DRV8832 Low-Voltage Motor Driver IC

1 Features

- H-Bridge Voltage-Controlled Motor Driver
  - Drives DC Motor, One Winding of a Stepper Motor, or Other Actuators/Loads
  - Efficient PWM Voltage Control for Constant Motor Speed With Varying Supply Voltages
  - Low MOSFET On-Resistance: HS + LS 450 mΩ
- 1-A Maximum DC/RMS or Peak Drive Current
- 2.75-V to 6.8-V Operating Supply Voltage Range
- 300-nA (Typical) Sleep Mode Current
- Reference Voltage Output
- Current Limit Circuit
- Fault Output
- Thermally-Enhanced Surface Mount Packages

2 Applications

- Battery-Powered:
  - Printers
  - Toys
  - Robotics
  - Cameras
  - Phones
- Small Actuators, Pumps, and so forth

3 Description

The DRV8832 provides an integrated motor driver solution for battery-powered toys, printers, and other low-voltage or battery-powered motion control applications. The device has one H-bridge driver, and can drive one DC motor or one winding of a stepper motor, as well as other loads like solenoids. The output driver block consists of N-channel and P-channel power MOSFETs configured as an H-bridge to drive the motor winding.

Provided with sufficient PCB heatsinking, the DRV8832 can supply up to 1 A of DC/RMS or peak output current. The device operates on power supply voltages from 2.75 V to 6.8 V.

To maintain constant motor speed over varying battery voltages while maintaining long battery life, a PWM voltage regulation method is provided. An input pin allows programming of the regulated voltage. A built-in voltage reference output is also provided.

Internal protection functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature protection.

The DRV8832 also provides a current limit function to regulate the motor current during conditions like motor start-up or stall, as well as a fault output pin to signal a host processor of a fault condition.

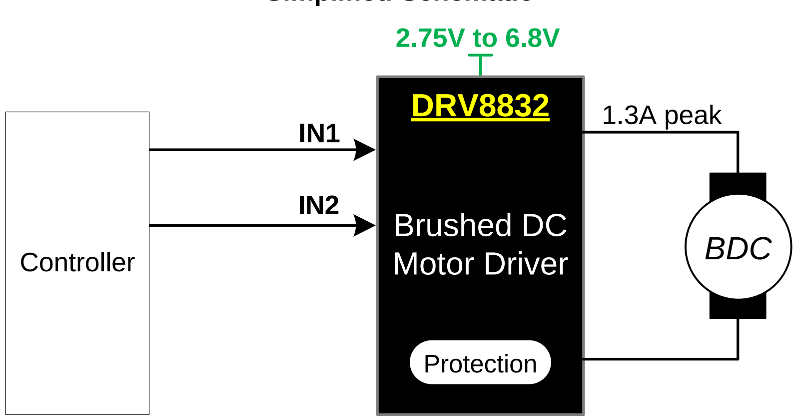
The DRV8832 is available in a tiny 3-mm × 3-mm 10-pin VSON package and MSOP PowerPAD™ package (Eco-friendly: RoHS & no Sb/Br).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8832	MSOP PowerPAD (10)	3.00 mm × 3.00 mm
	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

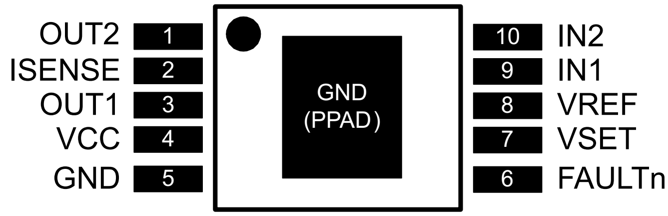
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (October 2013) to Revision I **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added V_{HYS} parameter row under the Logic-Level Inputs section in *Electrical Characteristics* ... 5
- Changed the paragraph describing the FAULT behavior in *Current Limit* ... 10
- Updated the paragraphs in *Power Dissipation* and added Equation 4 ... 16

5 Pin Configuration and Functions

DGQ and DRC Packages
10-Pin MSOP PowerPAD and VSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION	
NAME	NO.			
FAULTn	6	OD	Fault output	Open-drain output driven low if fault condition present
GND	5	—	Device ground	
IN1	9	I	Bridge A input 1	Logic high sets OUT1 high
IN2	10	I	Bridge A input 2	Logic high sets OUT2 high
ISENSE	2	IO	Current sense resistor	Connect current sense resistor to GND. Resistor value sets current limit level.
OUT1	3	O	Bridge output 1	Connect to motor winding
OUT2	1	O	Bridge output 2	Connect to motor winding
VCC	4	—	Device and motor supply	Bypass to GND with a 0.1-μF (minimum) ceramic capacitor.
VREF	8	O	Reference voltage output	Reference voltage output
VSET	7	I	Voltage set input	Input voltage sets output regulation voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
	Power supply voltage, VCC	–0.3	7	V
	Input pin voltage	–0.5	7	V
	Peak motor drive output current (3)	Internally limited		A
	Continuous motor drive output current (3)	–1	1	A
	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Motor power supply voltage	2.75		6.8	V
I_{OUT}	Continuous or peak H-bridge output current (1)	0		1	A

(1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC (1)		DRV8832		UNIT
		DGQ (MSOP PowerPAD)	DRC (VSON)	
		10 PINS	10 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	69.3	50.2	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	63.5	78.4	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	51.6	18.8	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	1.5	1.1	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	23.2	17.9	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	9.5	5.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{CC} = 2.75 V to 6.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VCC}	VCC operating supply current	V_{CC} = 5 V		1.4	2	mA
I_{VCCQ}	VCC sleep mode supply current	V_{CC} = 5 V, T_A = 25°C		0.3	1	μA
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising		2.575	2.75	V
		V_{CC} falling		2.47		
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage				0.25 × VCC	V
V_{HYS}	Input hysteresis			0.08 × Vcc		V
V_{IH}	Input high voltage		0.5 × VCC			V
I_{IL}	Input low current	V_{IN} = 0	–10		10	μA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	μA
LOGIC-LEVEL OUTPUTS (FAULTn)						
V_{OL}	Output low voltage	V_{CC} = 5 V, I_{OL} = 4 mA(1)		0.5		V
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_{CC} = 5 V, I_O = 0.8 A, T_J = 85°C		290	400	mΩ
		V_{CC} = 5 V, I_O = 0.8 A, T_J = 25°C		250		
$R_{DS(ON)}$	LS FET on resistance	V_{CC} = 5 V, I_O = 0.8 A, T_J = 85°C		230	320	mΩ
		V_{CC} = 5 V, I_O = 0.8 A, T_J = 25°C		200		
I_{OFF}	Off-state leakage current		–20		20	μA
MOTOR DRIVER						
t_R	Rise time	V_{CC} = 3 V, load = 4 Ω	50		300	ns
t_F	Fall time	V_{CC} = 3 V, load = 4 Ω	50		300	ns
f_{SW}	Internal PWM frequency			44.5		kHz
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.3		3	A
t_{OCP}	OCP deglitch time			2		μs
T_{TSD}	Thermal shutdown temperature	Die temperature(1)	150	160	180	°C
VOLTAGE CONTROL						
V_{REF}	Reference output voltage		1.235	1.285	1.335	V
ΔV_{LINE}	Line regulation	V_{CC} = 3.3 V to 6 V, V_{OUT} = 3 V(1) I_{OUT} = 500 mA		±1%		
ΔV_{LOAD}	Load regulation	V_{CC} = 5 V, V_{OUT} = 3 V I_{OUT} = 200 mA to 800 mA(1)		±1%		
CURRENT LIMIT						
V_{ILIM}	Current limit sense voltage		160	200	240	mV
t_{ILIM}	Current limit fault deglitch time			275		ms
R_{ISEN}	Current limit set resistance (external resistor value)		0		1	Ω

(1) Not production tested.

6.6 Typical Characteristics

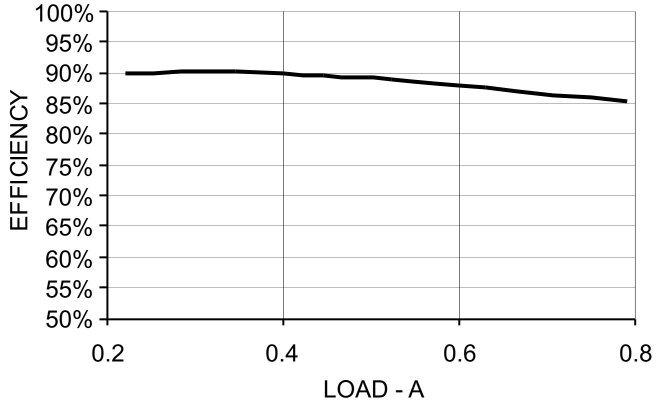


Figure 1. Efficiency vs Load Current (V_{IN} = 5 V, V_{OUT} = 3 V)

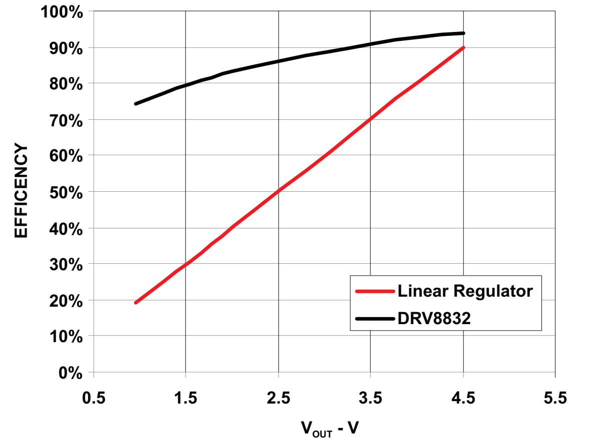


Figure 2. Efficiency vs Output Voltage (V_{IN} = 5 V, I_{OUT} = 500 mA)

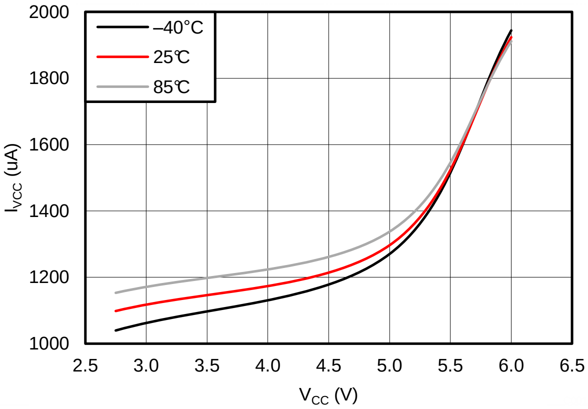


Figure 3. I_{VCC} vs V_{VCC}

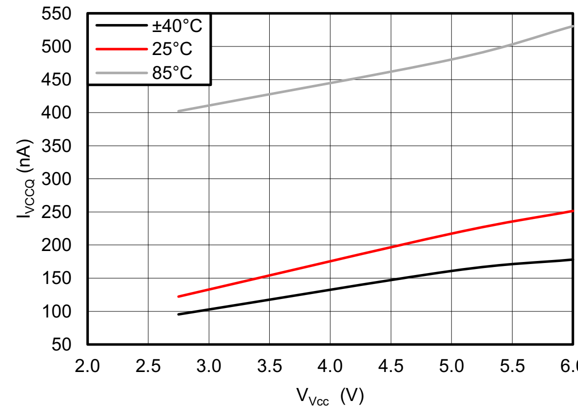


Figure 4. I_{VCCQ} vs V_{VCC}

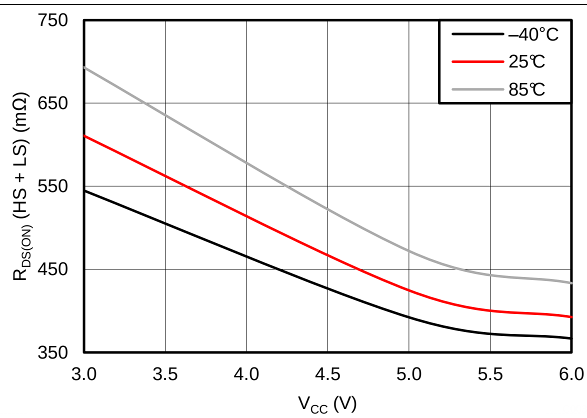


Figure 5. $R_{DS(ON)}$ vs V_{VCC}

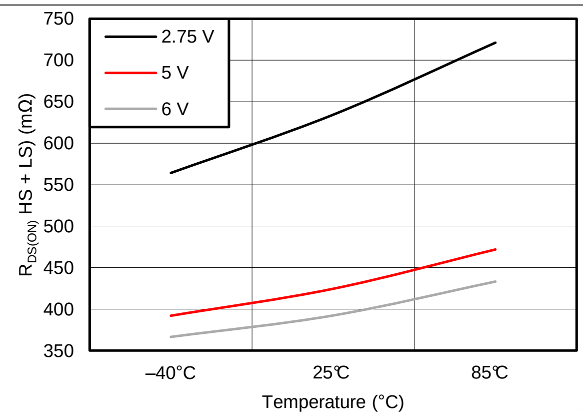


Figure 6. $R_{DS(ON)}$ HS + LS vs Temperature

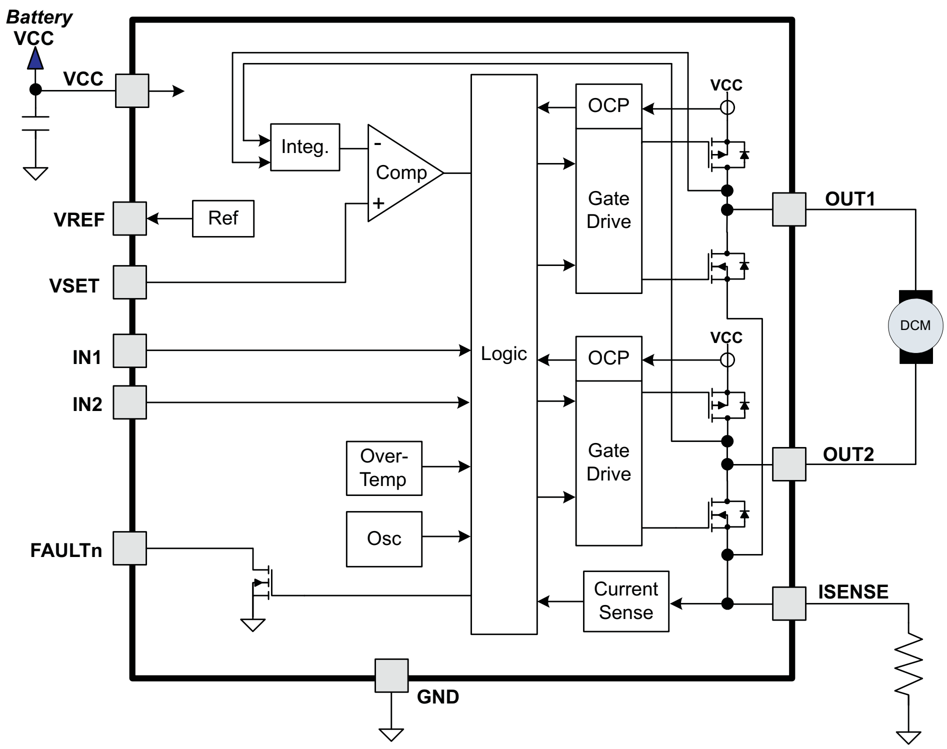
7 Detailed Description

7.1 Overview

The DRV8832 is an integrated motor driver solution used for brushed motor control. The device integrates one H-bridge, current regulation circuitry, and a PWM voltage regulation method.

Using the PWM voltage regulation allows the motor to maintain the desired speed as VCC changes. Battery operation is an example of using this feature. When the battery is new or fully charged VCC will be higher than when the battery is old or partially discharged. The speed of the motor will vary based on the voltage of the battery. By setting the desired voltage across the motor at a lower voltage, a fully charged battery will use less power and spin the motor at the same speed as a battery that has been partially discharged.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Motor Driver

The DRV8832 contains an H-bridge motor driver with PWM voltage-control circuitry with current limit circuitry. Figure 7 shows a block diagram of the motor control circuitry.

Feature Description (continued)

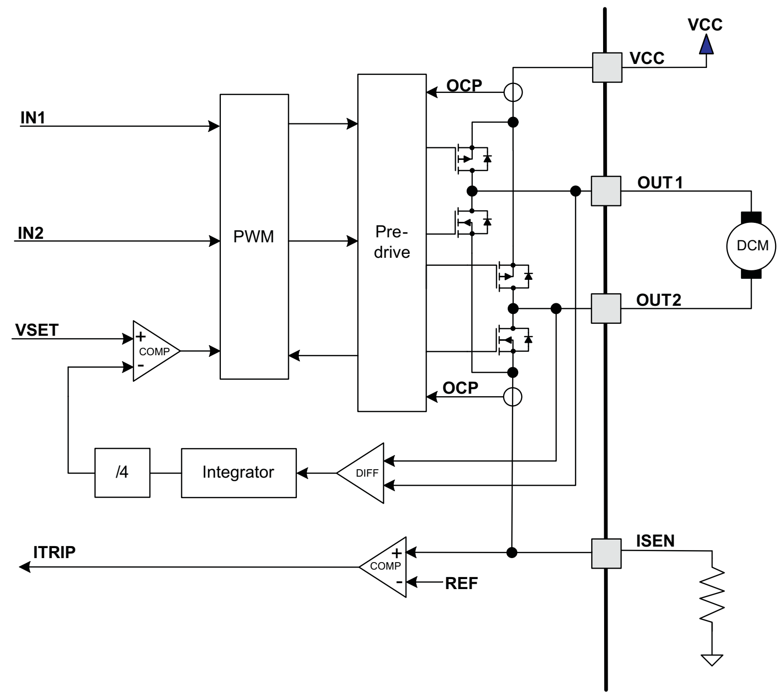


Figure 7. Motor Control Circuitry

7.3.2 Bridge Control

The IN1 and IN2 control pins enable the H-bridge outputs. Table 1 shows the logic:

Table 1. H-Bridge Logic

IN1	IN2	OUT1	OUT2	Function
0	0	Z	Z	Sleep/Coast
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	H	H	Brake

When both inputs are low, the output drivers are disabled and the device is placed into a low-power sleep state. The current limit fault condition (if present) is also cleared. Note that when transitioning from either brake or sleep mode to forward or reverse, the voltage control PWM starts at zero duty cycle. The duty cycle slowly ramps up to the commanded voltage. This can take up to 12 ms to go from sleep to 100% duty cycle. Because of this, high-speed PWM signals cannot be applied to the IN1 and IN2 pins. To control motor speed, use the VSET pin as described below.

Because of the sleep mode functionality described previously, when applying an external PWM to the DRV8832, hold one input logic high while applying a PWM signal to the other. If the logic input is held low instead, then the device will cycle in and out of sleep mode, causing the FAULTn pin to pulse low on every sleep mode exit.

7.3.3 Voltage Regulation

The DRV8832 provides the ability to regulate the voltage applied to the motor winding. This feature allows constant motor speed to be maintained even when operating from a varying supply voltage such as a discharging battery.

The DRV8832 uses a pulse-width modulation (PWM) technique instead of a linear circuit to minimize current consumption and maximize battery life.

The circuit monitors the voltage difference between the output pins and integrates it, to get an average DC voltage value. This voltage is divided by 4 and compared to the VSET pin voltage. If the averaged output voltage (divided by 4) is lower than VSET, the duty cycle of the PWM output is increased; if the averaged output voltage (divided by 4) is higher than VSET, the duty cycle is decreased.

During PWM regulation, the H-bridge is enabled to drive current through the motor winding during the PWM on time. This is shown in the diagram below as case 1. The current flow direction shown indicates the state when IN1 is high and IN2 is low.

Note that if the programmed output voltage is greater than the supply voltage, the device will operate at 100% duty cycle and the voltage regulation feature will be disabled. In this mode the device behaves as a conventional H-bridge driver.

During the PWM off time, winding current is recirculated by enabling both of the high-side FETs in the bridge as shown in Figure 8.

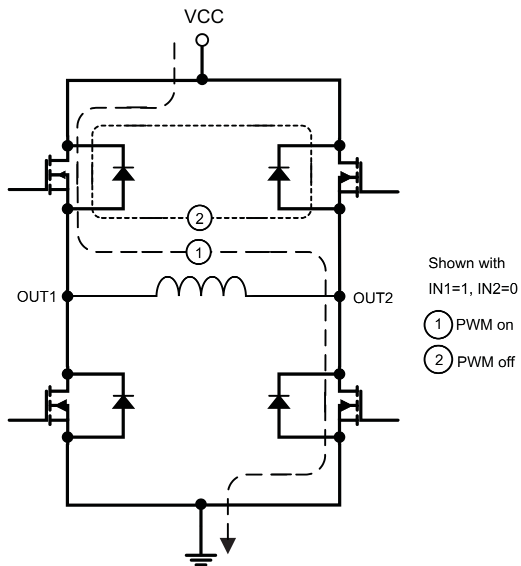


Figure 8. Voltage Regulation

7.3.4 Reference Output

The DRV8832 includes a reference voltage output that can be used to set the motor voltage. Typically for a constant-speed application, VSET is driven from VREF through a resistor divider to provide a voltage equal to 1/4 the desired motor drive voltage.

For example, if VREF is connected directly to VSET, the voltage will be regulated at 5.14 V. If the desired motor voltage is 3 V, VREF should be 0.75 V. This can be obtained with a voltage divider using 53 kΩ from VREF to VSET, and 75 kΩ from VSET to GND.

7.3.5 Current Limit

A current limit circuit is provided to protect the system in the event of an overcurrent condition, such as what would be encountered if driving a DC motor at start-up or with an abnormal mechanical load (stall condition).

The motor current is sensed by monitoring the voltage across an external sense resistor. When the voltage exceeds a reference voltage of 200 mV for more than approximately 3 µs, the PWM duty cycle is reduced to limit the current through the motor to this value. This current limit allows for starting the motor while controlling the current.

If the current limit condition persists for some time, it is likely that a fault condition has been encountered, such as the motor being run into a stop or a stalled condition. An overcurrent event must persist for approximately 275 ms before the fault is registered. After approximately 275 ms, a fault signaled to the host by driving the FAULTn signal low. Operation of the motor driver will continue.

The current limit fault condition is self-clearing and will be released when the abnormal load (stall condition) is removed.

The resistor used to set the current limit must be less than 1 Ω. Its value may be calculated using Equation 1:

$$R_{ISENSE} = \frac{200\ mV}{I_{LIMIT}}$$

where

- R_{ISENSE} is the current sense resistor value
- I_{LIMIT} is the desired current limit (in mA) (1)

If the current limit feature is not needed, the ISENSE pin may be directly connected to ground.

7.3.6 Protection Circuits

The DRV8832 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.6.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled, and the FAULTn signal will be driven low. The device will remain disabled until VCC is removed and re-applied.

Overcurrent conditions are sensed independently on both high and low side devices. A short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that OCP is independent of the current limit function, which is typically set to engage at a lower current level; the OCP function is intended to prevent damage to the device under abnormal (for example, short-circuit) conditions.

7.3.6.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the FAULTn signal will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

7.3.6.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, the FAULTn signal will be driven low, and internal logic will be reset. Operation will resume when VCC rises above the UVLO threshold.

Table 2. Device Protection

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VCC undervoltage (UVLO)	VCC < V_{UVLO}	FAULTn	Disabled	Disabled	VCC > V_{UVLO}
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	FAULTn	Disabled	Operating	Power Cycle VCC
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	FAULTn	Disabled	Operating	$T_J < T_{TSD} – T_{HYS}$

7.4 Device Functional Modes

The DRV8832 is active when either IN1 or IN2 are set to a logic high. Sleep mode is entered when both IN1 and IN2 are set to a logic low. When in sleep mode, the H-bridge FETs are disabled (Hi-Z).

Table 3. Modes of Operation

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Operating	IN1 or IN2 high	Operating	Operating
Sleep mode	IN1 and IN2 low	Disabled	Disabled
Fault encountered	Any fault condition met	Disabled	See Table 2

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8832 is used in brushed DC applications to provide a constant motor speed over varying voltages. The following design procedure can be used to configure the DRV8832 for a system with a VCC variance of 4 V to 6 V.

8.2 Typical Application

Figure 9 shows a common application of the DRV8832.

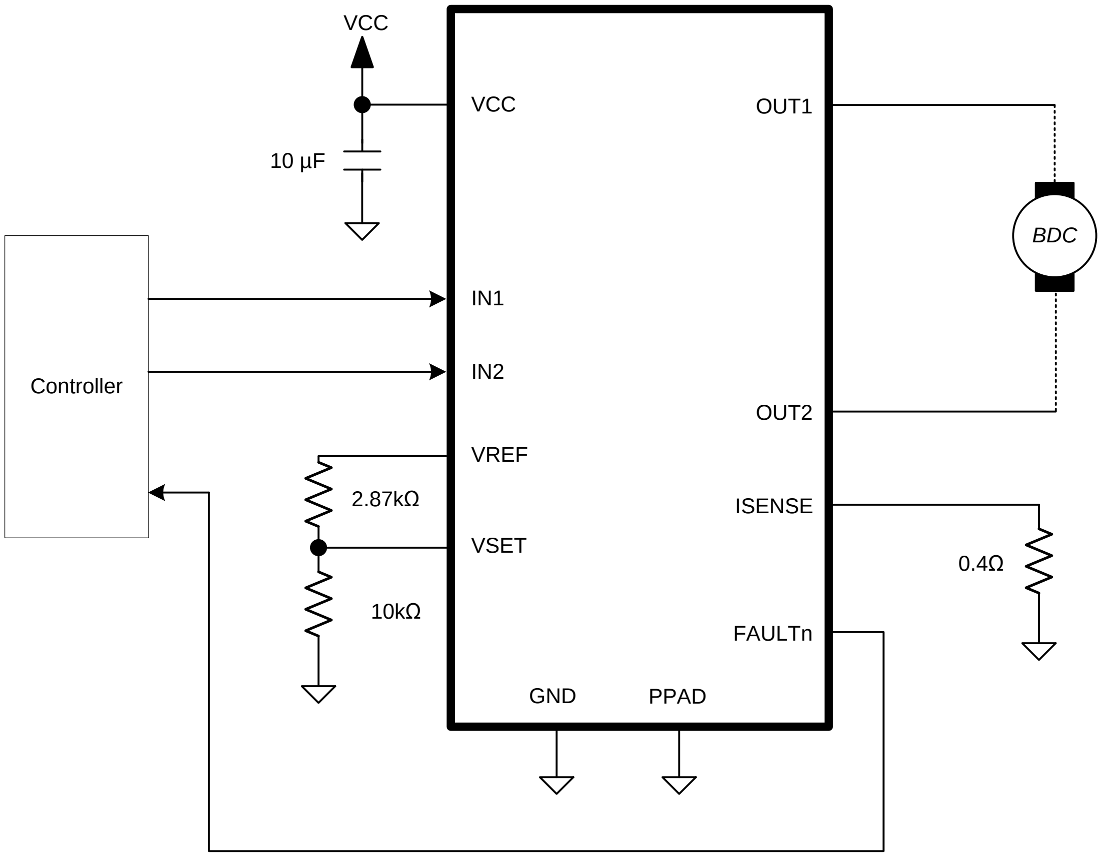


Figure 9. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 4 lists the design parameters for this application.

Table 4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_{CC}	4 V
Motor RMS current	I_{RMS}	0.3 A
Motor start-up current	I_{START}	0.6 A
Motor current trip point	IL_{IMIT}	0.5 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

For the DRV8832, TI recommends setting a motor voltage at the lowest system VCC. This will maintain a constant RPM across varying VCC conditions.

For example if the VCC voltage can vary from 4.5 V to 5.5 V, setting the VSET voltage to 1.125 V will compensate for power supply variation. The DRV8832 will set the motor voltage at 4.5 V, even if VCC is 5.5 V.

8.2.2.2 Motor Current Trip Point

When the voltage on pin ISENSE exceeds V_{ILIM} (0.2 V), overcurrent is detected. The R_{SENSE} resistor should be sized to set the desired I_{LIMIT} level.

$$R_{ISENSE} = 0.2\ V\ /\ I_{LIMIT} \tag{2}$$

To set I_{LIMIT} to 5 A, R_{ISENSE} = 0.2 V / 0.5 A = 0.4 Ω.

To prevent false trips, I_{LIMIT} must be higher than regular operating current. Motor current during start-up is typically much higher than steady-state spinning, because the initial load torque is higher, and the absence of back-EMF causes a higher voltage and extra current across the motor windings.

It can be beneficial to limit start-up current by using series inductors on the DRV8832 output, as that allows I_{LIMIT} to be lower, and it may decrease the system's required bulk capacitance. Start-up current can also be limited by ramping the forward drive duty cycle.

8.2.2.3 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}^2 \times R$. For example, if peak motor current is 1 A, RMS motor current is 0.7 A, and a 0.4-Ω sense resistor is used, the resistor will dissipate 0.7 $A^2 \times$ 0.4 Ω = 0.2 W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

8.2.2.4 Low Power Operation

Under normal operation, using sleep mode to minimize supply current should be sufficient.

If desired, power can be removed to the DRV8832 to further decrease supply current. TI recommends removing power to the FAULTn pullup resistor when removing power to the DRV8832. Removing power from the FAULTn pullup resistor will eliminate a current path from the FAULTn pin through an ESD protection diode to VCC. TI also recommends setting both IN1 and IN2 as a logic low when power is removed.

8.2.3 Application Curves

The following scope captures show how the output duty cycle changes to as VCC increases. This allows the motor to spin at a constant speed as VCC changes. At VCC=3.9V, the output duty cycle is 100% on. As the VCC voltage increases to greater than 4 V, the output duty cycle begins to decrease. The output duty cycle is shown at VCC=4.5 V, VCC=5 V and VCC=5.5 V.

- Channel 1 – OUT1: IN1 – Logic Low
- Channel 2 – OUT2: IN2 – Logic High
- Channel 4 – Motor current: VSET – 1 V
- Motor used: NMB Technologies Corporation, PPN7PA12C1

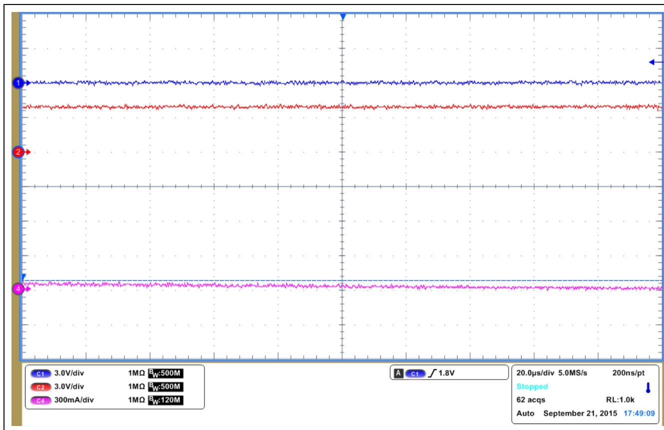


Figure 10. Output Pulse Width Modulating at VCC = 3.9 V

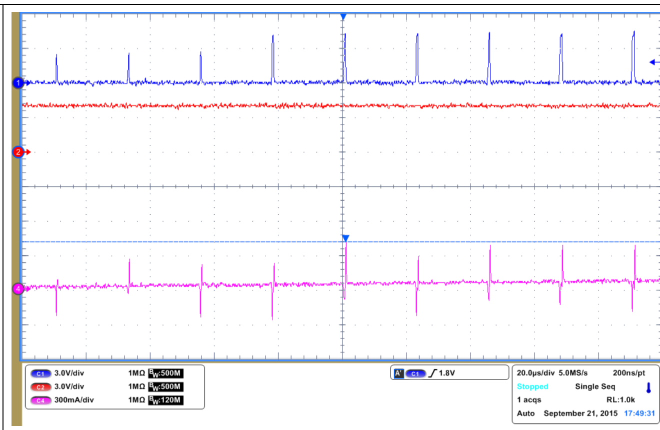


Figure 11. Output Pulse Width Modulating at VCC = 4 V

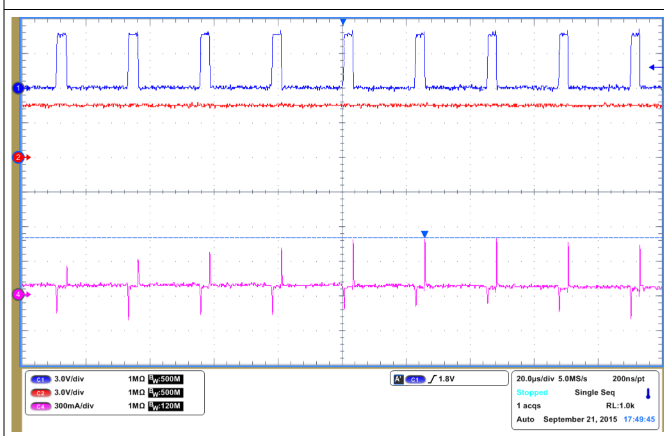


Figure 12. Output Pulse Width Modulating at VCC = 4.5 V

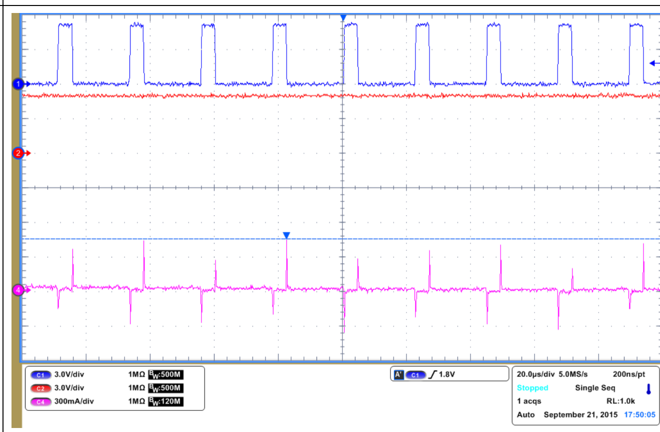


Figure 13. Output Pulse Width Modulating at VCC = 5 V

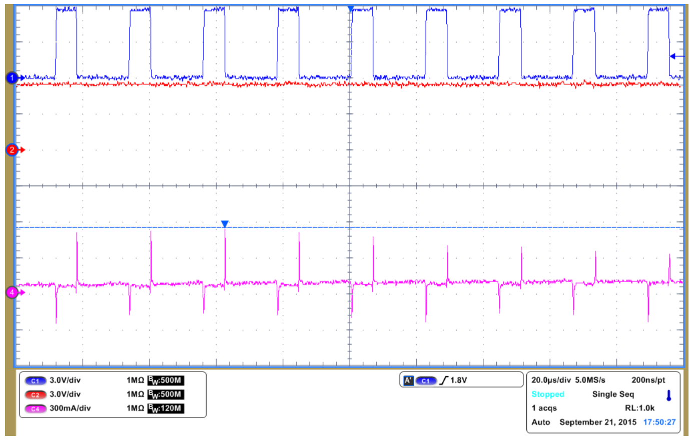


Figure 14. Output Pulse Width Modulating at VCC = 5.5 V

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

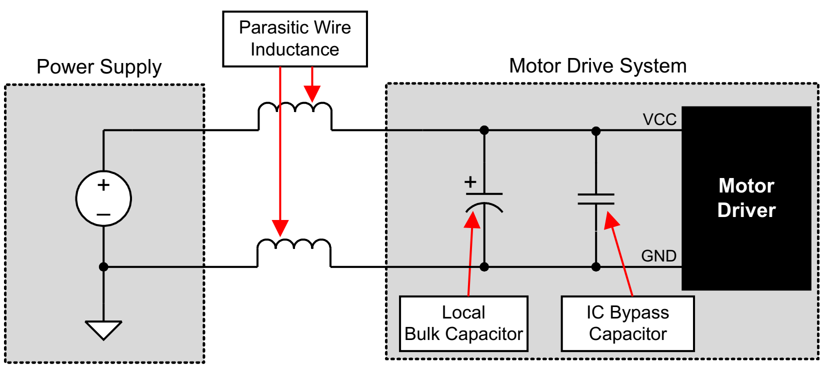


Figure 15. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

9.2 Power Supervisor

The DRV8832 is capable of entering a low-power sleep mode by bringing both of the INx control inputs logic low. The outputs will be disabled Hi-Z.

To exit the sleep mode, bring either or both of the INx inputs logic high. This will enable the H-bridges. When exiting the sleep mode, the FAULTn pin will pulse low.

10 Layout

10.1 Layout Guidelines

The VCC pin should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1-µF rated for VCC. This capacitor should be placed as close to the VCC pin as possible with a thick trace or ground plane connection to the device GND pin.

The VCC pin must be bypassed to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8832.

10.2 Layout Example

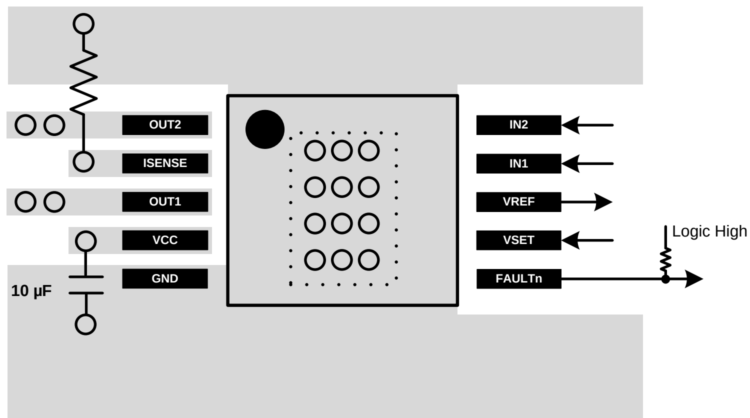


Figure 16. Recommended Layout

10.3 Thermal Considerations

The DRV8832 has thermal shutdown (TSD) as described *Thermal Shutdown (TSD)*. If the die temperature exceeds approximately 160°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

The power dissipation of the DRV8832 is a function of RMS motor current and the each output's FET resistance ($R_{DS(ON)}$).

$$\text{Power} \approx I_{RMS}^2 \times (\text{High-Side } R_{DS(ON)} + \text{Low-Side } R_{DS(ON)}) \quad (3)$$

For this example, the ambient temperature is 35°C, and the junction temperature reaches 65°C. At 65°C, the sum of $R_{DS(ON)}$ is about 1 Ω. With an example motor current of 0.8 A, the dissipated power in the form of heat will be 0.8 A^2 × 1 Ω = 0.64 W.

The temperature that the DRV8832 reaches will depend on the thermal resistance to the air and PCB. It is important to solder the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, dissipate heat into the PCB and reduce the device temperature. In the example used here, the DRV8832 had an effective thermal resistance RθJA of 47°C/W, and:

$$T_J = T_A + (P_O \times R_{\theta JA}) = 35°C + (0.64\ W \times 47°C/W) = 65°C \quad (4)$$

10.3.2 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

Thermal Considerations (continued)

For details about how to design the PCB, refer to TI application report SLMA002, *PowerPAD™ Thermally Enhanced Package* and TI application brief SLMA004, *PowerPAD™ Made Easy*, available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Thermally Enhanced Package* SLMA002
- *PowerPAD™ Made Easy* SLMA004

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8832DGQ	Obsolete	Production	HVSSOP (DGQ) | 10	-	-	Call TI	Call TI	-40 to 85	8832
DRV8832DGQR	Active	Production	HVSSOP (DGQ) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	8832
DRV8832DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	8832
DRV8832DRCT	Obsolete	Production	VSON (DRC) | 10	-	-	Call TI	Call TI	-40 to 85	8832

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DRV8832 :

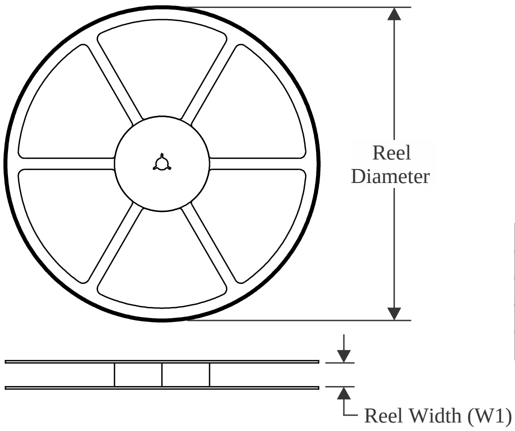
- Automotive : DRV8832-Q1

NOTE: Qualified Version Definitions:

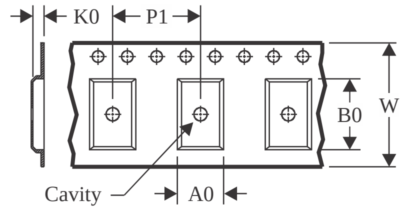
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

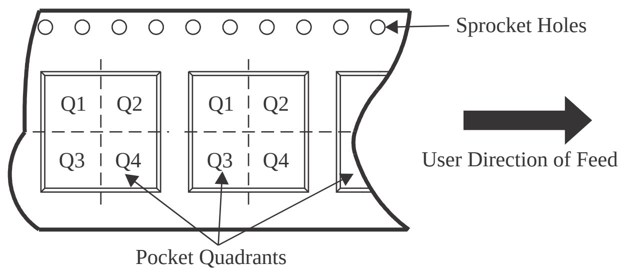


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

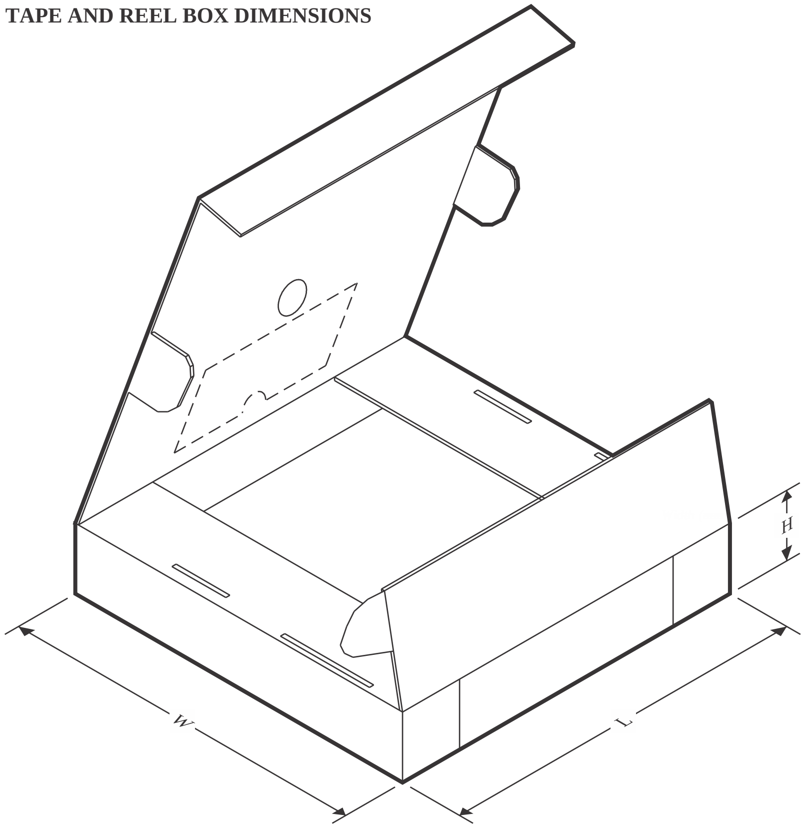
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8832DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DRV8832DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

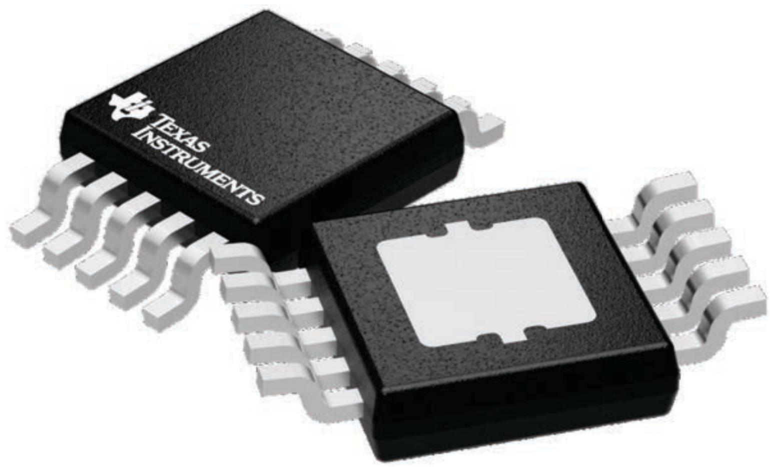
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8832DGQR	HVSSOP	DGQ	10	2500	356.0	356.0	35.0
DRV8832DRCR	VSON	DRC	10	3000	335.0	335.0	25.0

DGQ 10

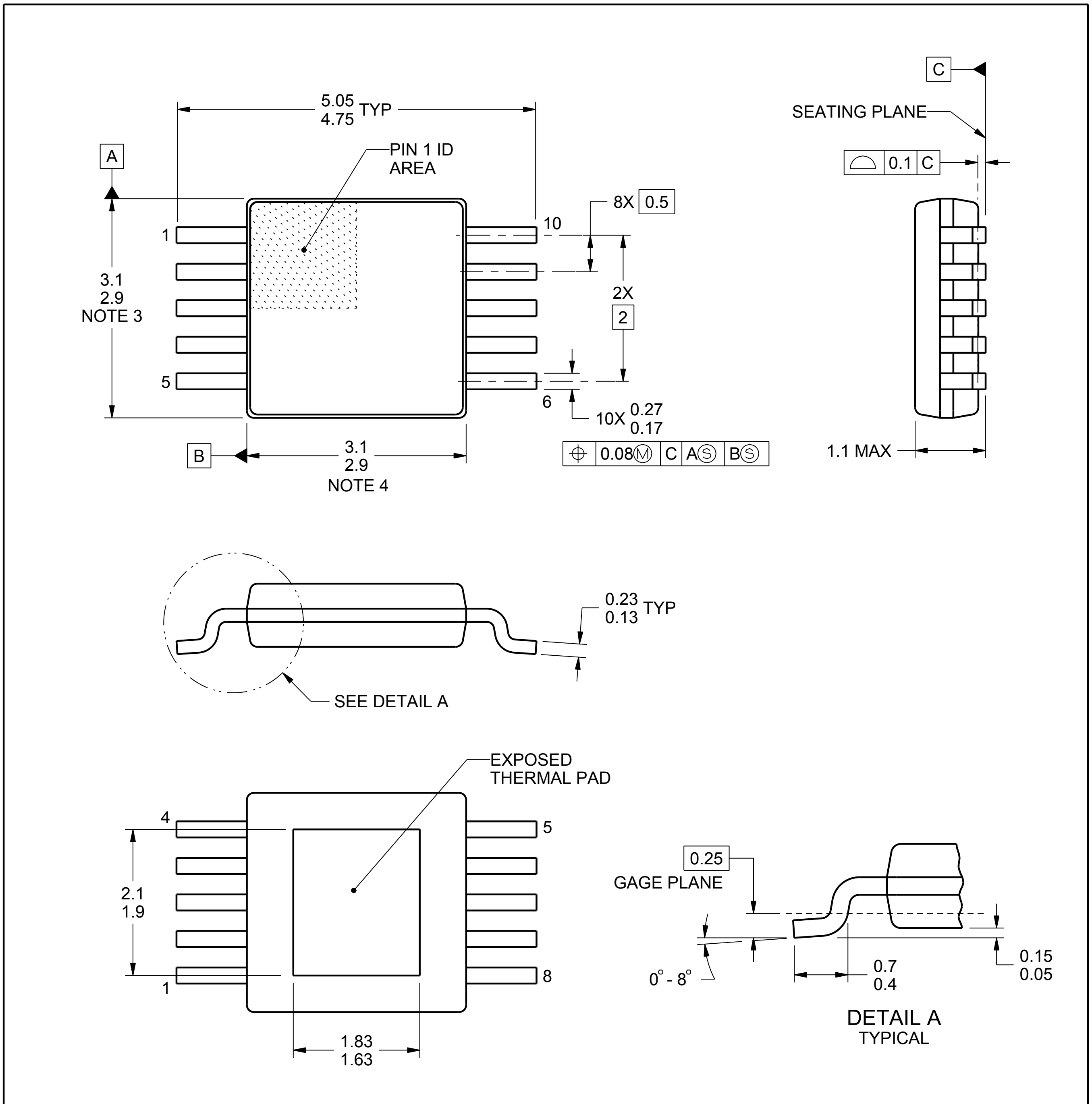
PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

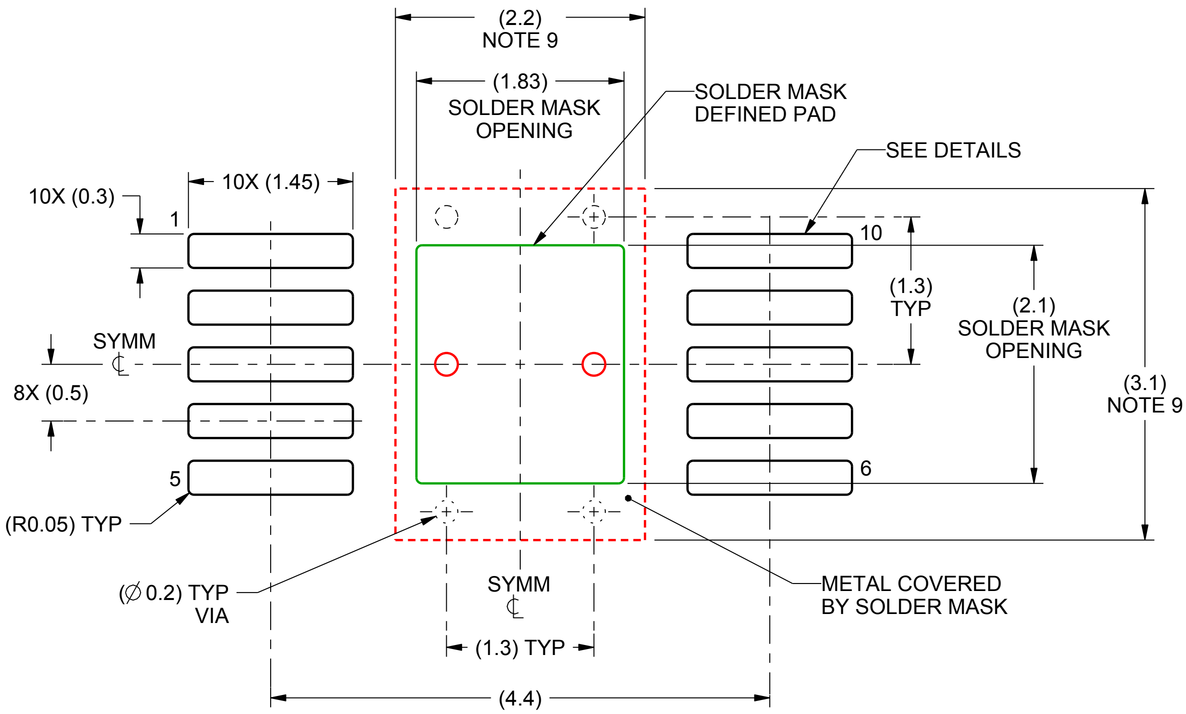


4221816/A 08/2015

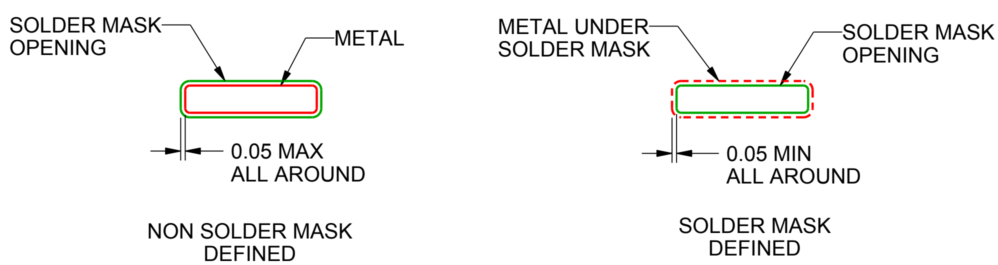
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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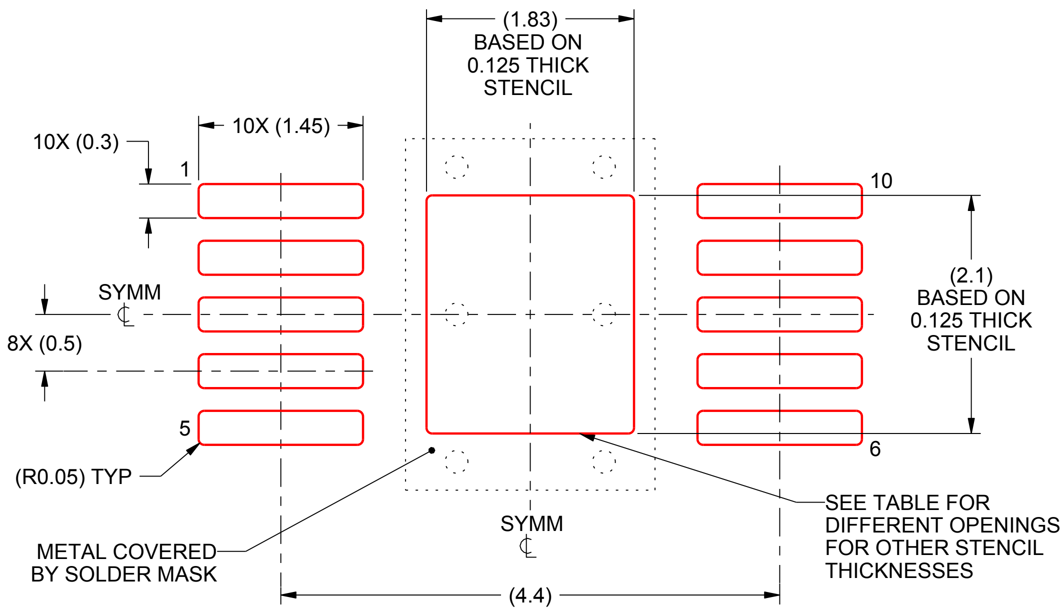
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.35
0.125	1.83 X 2.1 (SHOWN)
0.150	1.67 X 1.92
0.175	1.55 X 1.77

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

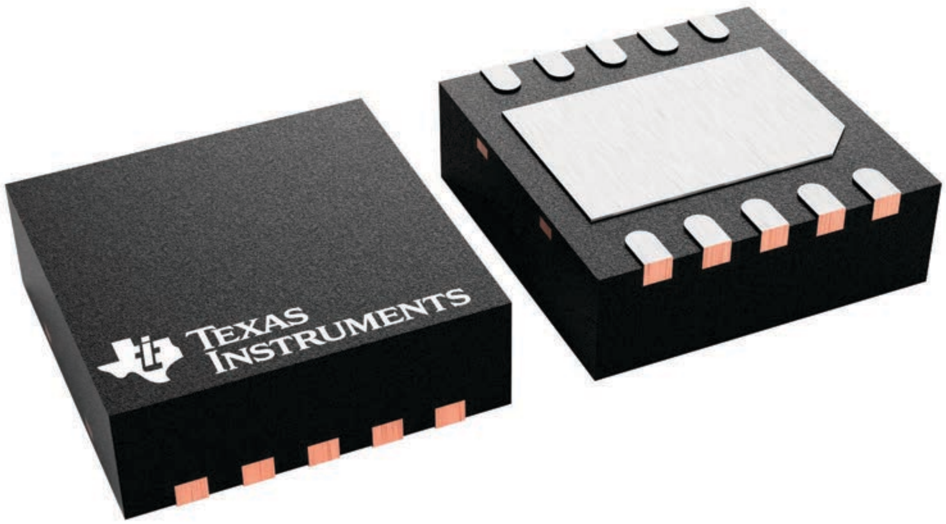
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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