

SN5430, SN54LS30, SN54S30 SN7430, SN74LS30, SN74S30 8-INPUT POSITIVE-NAND GATES

SDLS099 - DECEMBER 1983 - REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

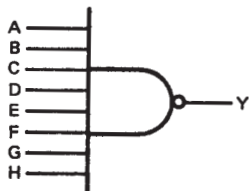
These devices contain a single 8-input NAND gate.

The SN5430, SN54LS30, and SN54S30 are characterized for operation over the full military range of -55°C to 125°C. The SN7430, SN74LS30, and SN74S30 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic diagram

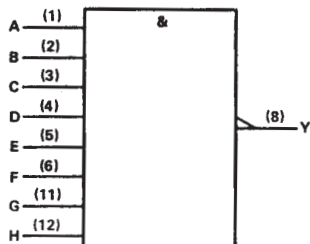


positive logic

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \quad \text{or}$$

$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

logic symbol†

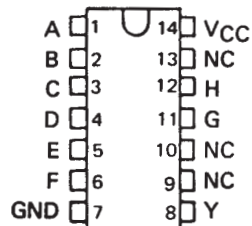


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

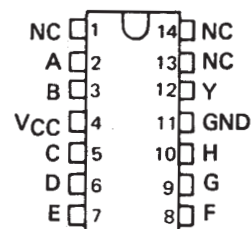
SN5430 . . . J PACKAGE
SN54LS30, SN54S30 . . . J OR W PACKAGE
SN7430 . . . N PACKAGE
SN74LS30, SN74S30 . . . D OR N PACKAGE

(TOP VIEW)



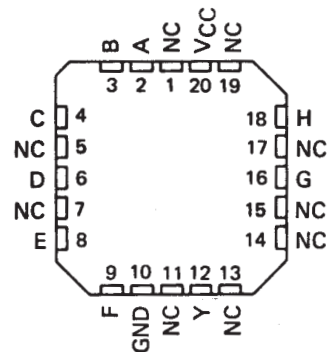
SN5430 . . . W PACKAGE

(TOP VIEW)



SN54LS30, SN54S30 . . . FK PACKAGE

(TOP VIEW)

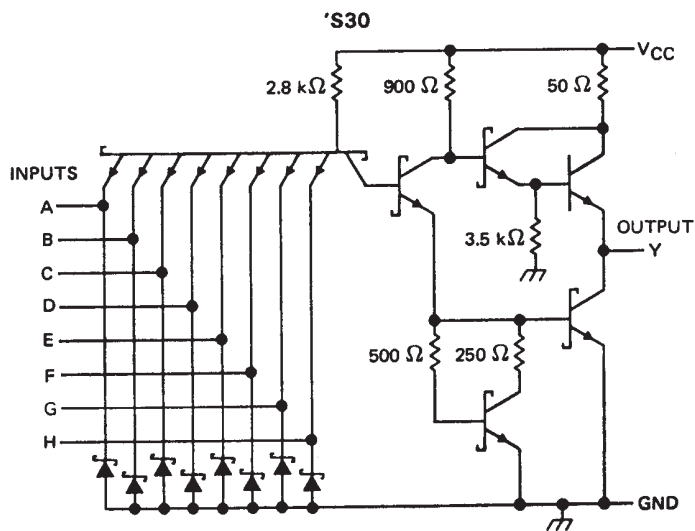
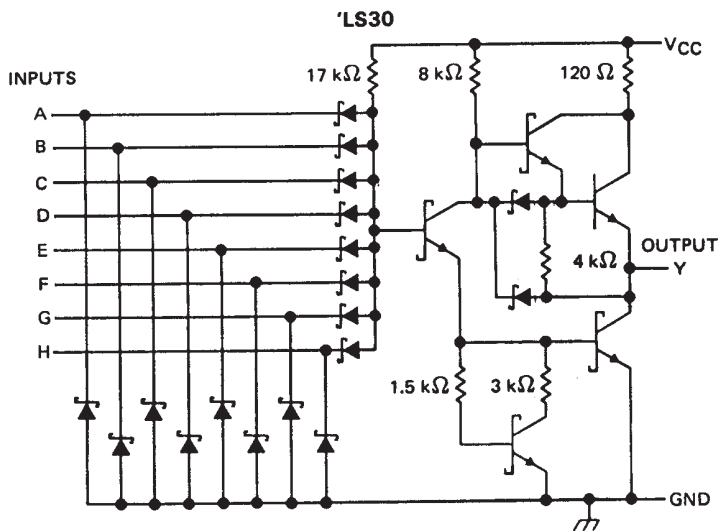
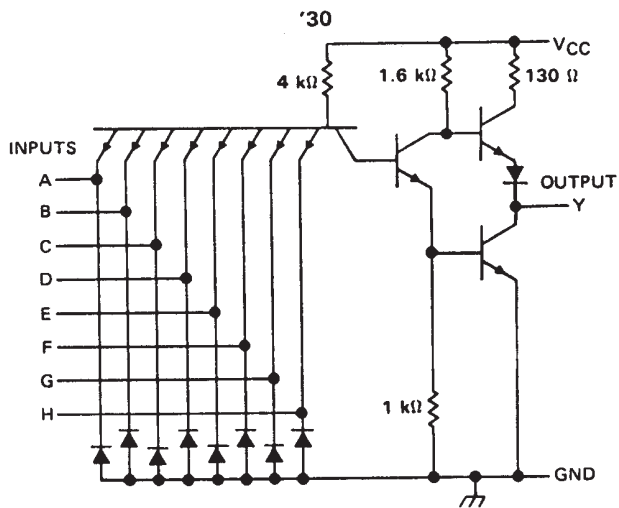


NC - No internal connection

**SN5430, SN54LS30, SN54S30
SN7430, SN74LS30, SN74S30
8-INPUT POSITIVE-NAND GATES**

SDLS099 – DECEMBER 1983 – REVISED MARCH 1988

schematics (each gate)



Resistor values shown are nominal.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN5430, SN54LS30, SN54S30
SN7430, SN74LS30, SN74S30
8-INPUT POSITIVE-NAND GATES
SDLS099 – DECEMBER 1983 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN5430	–55 °C to 125 °C
SN7430	0 °C to 70 °C
Storage temperature range	–65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5430			SN7430			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			–0.4			–0.4	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5430			SN7430			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			–1.5			–1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–1.6			–1.6	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	–20		–55	–18		–55	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0$		1	2		1	2	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		3	6		3	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 400 \Omega, C_L = 15 \text{ pF}$		13	22	ns
t_{PHL}					8	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



**SN5430, SN54LS30, SN54S30
SN7430, SN74LS30, SN74S30
8-INPUT POSITIVE-NAND GATES**

SDLS099 – DECEMBER 1983 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS30	-55°C to 125°C
SN74LS30	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS30			SN74LS30			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			-0.4			-0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS30			SN74LS30			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25	0.4				0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$				0.25	0.5		
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0$		0.35	0.5		0.35	0.5	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		0.6	1.1		0.6	1.1	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		8	15	ns
t_{PHL}					13	20	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



SN5430, SN54LS30, SN54S30
SN7430, SN74LS30, SN74S30
8-INPUT POSITIVE-NAND GATES
SDLS099 – DECEMBER 1983 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S30	–55 °C to 125 °C
SN74S30	0 °C to 70 °C
Storage temperature range	–65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S30			SN74S30			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			–1			–1	mA
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S30			SN74S30			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			–1.2			–1.2	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			–2			–2	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	–40		–100	–40		–100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0$		3	5		3	5	mA
I_{CCL}	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		5.5	10		5.5	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$		4	6	ns
t_{PHL}					4.5	7	ns
t_{PLH}			$R_L = 280 \Omega, C_L = 50 \text{ pF}$		5.5		ns
t_{PHL}					6.5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9679201QCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9679201QC A SNJ54S30J
5962-9679201QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9679201QD A SNJ54S30W
5962-9679201QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9679201QD A SNJ54S30W
JM38510/30009B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30009B2A
JM38510/30009B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30009B2A
JM38510/30009BCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30009BCA
JM38510/30009BCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30009BCA
JM38510/30009BDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30009BDA
JM38510/30009BDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30009BDA
SN5430J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN5430J
SN5430J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN5430J
SN54LS30J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS30J
SN54LS30J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS30J
SN54S30J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S30J
SN54S30J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S30J
SN74LS30D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	LS30
SN74LS30D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	LS30
SN74LS30DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS30
SN74LS30DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS30
SN74LS30N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS30N

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS30N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS30N
SN74LS30NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS30
SN74LS30NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS30
SNJ5430J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ5430J
SNJ5430J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ5430J
SNJ5430W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ5430W
SNJ5430W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ5430W
SNJ54LS30FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS30FK
SNJ54LS30FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS30FK
SNJ54LS30J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS30J
SNJ54LS30J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS30J
SNJ54LS30W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS30W
SNJ54LS30W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS30W
SNJ54S30J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9679201QC A SNJ54S30J
SNJ54S30J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9679201QC A SNJ54S30J
SNJ54S30W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9679201QD A SNJ54S30W
SNJ54S30W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9679201QD A SNJ54S30W

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54LS30, SN74LS30 :

- Catalog : [SN74LS30](#)
- Military : [SN54LS30](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

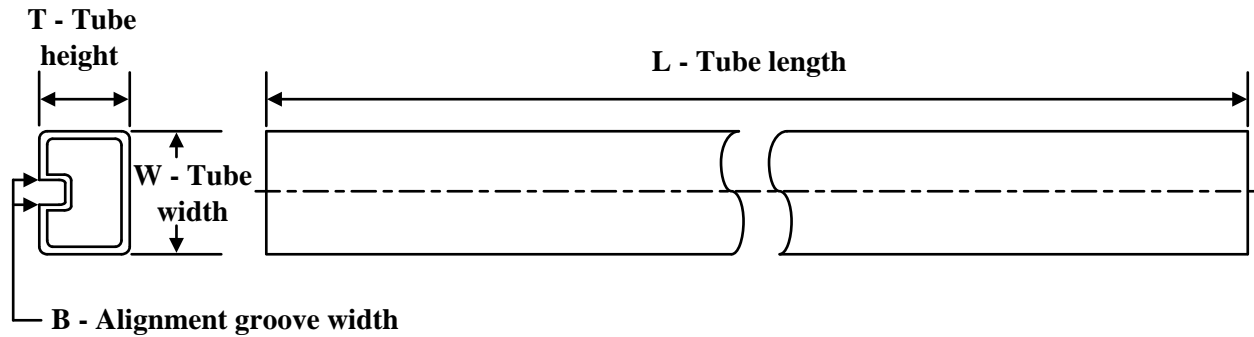

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS30DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS30NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS30DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS30NSR	SOP	NS	14	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9679201QDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/30009B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/30009BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/30009B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/30009BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS30N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS30N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS30NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS30NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ5430W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54LS30FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS30W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54S30W	W	CFP	14	25	506.98	26.16	6220	NA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

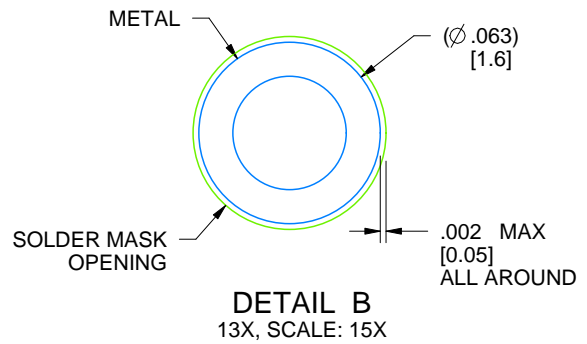
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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