SN74CB3Q3305 双路 FET 总线开关 2.5V 或 3.3V 低压高带宽总线开关

1 特性

- 高带宽数据路径（高达 500MHz）[1]
- 可耐受 5V 电压并支持器件上电或断电的 I/O
- 在运行范围内具有平缓的低通态电阻 (r_{on}) 特性（r_{on} 典型值 = 3Ω）
- 数据 I/O 端口支持超出电源电压范围的输入电压
  - 3.3V V_{CC} 时，开关范围为 0 至 5V
  - 2.5V V_{CC} 时，开关范围为 0 至 3.3V
- 具有接近零传播延迟的双向数据流
- 低输入和输出电容可更大程度减小负载和信号失真（$C_{io(OFF)}$ 典型值 = 3.5pF）
- 快速开关频率（f_{OE} 最大值 = 20MHz）
- 数据与控制输入提供下冲钳位二极管
- 低功耗（I_{CC} 典型值 = 0.25mA）
- V_{CC} 工作范围为 2.3V 至 3.6V
- 数据 I/O 支持 0 至 5V 信号电平（0.8V、1.2V、1.5V、1.8V、2.5V、3.3V 和 5V）
- 控制输入可由 TTL 或 5V/3.3V CMOS 输出驱动
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范

2 应用

- IP 电话：有线和无线
- 光学模块
- 光纤网络：光纤和 EPON 视频
- 专用分支交换机 (PBX)
- WiMAX 和无线基础设施设备
- USB、差分信号接口
- 总线隔离

3 描述

SN74CB3Q3305 器件是一款高带宽 FET 总线开关，此开关利用一个电荷泵来提升通道晶体管的栅极电压，从而提供一个平缓的低通态电阻 (r_{on})。平缓的低通态电阻可实现非常短的传播延迟，并且支持在数据输入/输出 (I/O) 端口上开关超出电源电压范围的输入电压。该器件还具有低的数据 I/O 电容，以更大限度地减少数据总线上的容性负载和信号失真。SN74CB3Q3305 器件专为支持高带宽应用而设计，提供优化的接口解决方案，非常适合宽带通信、网络和数据密集型计算系统。

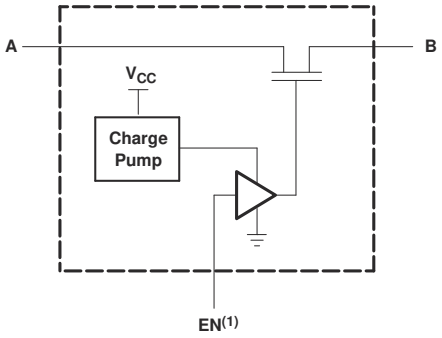
该器件完全符合使用 I_{off} 的部分断电应用的规范要求。I_{off} 电路可防止在器件断电时电流回流对器件造成损坏。该器件可在关闭时提供隔离。

为确保在加电或断电期间处于高阻抗状态，应将 OE 通过下拉电阻器接地；该电阻器的最小值取决于驱动器的拉电流能力。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN74CB3Q3305	VSSOP (8)	2.00 mm × 3.10 mm
	TSSOP (8)	3.00 mm × 6.10 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



(1) EN is the internal enable signal applied to the switch.

每个 FET 开关 (SW) 的简化版原理图)

[1] 有关 CB3Q 系列器件性能特性的更多信息，请参阅 TI 应用报告《*CBT-C、CB3T 和 CB3Q 信号开关系列*》，SCDA008。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (October 2015) to Revision D (September 2021) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.....1
- 更新了数据表以包含丰富的术语.....1

Changes from Revision B (October 2009) to Revision C (October 2015) **Page**

- 添加了 *引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分.....1

5 Pin Configuration and Functions

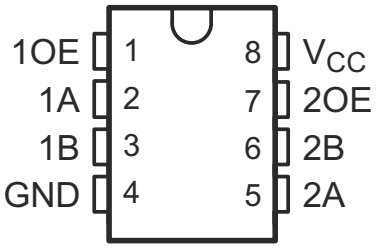


图 5-1. PW Package
8-Pin TSSOP
Top View

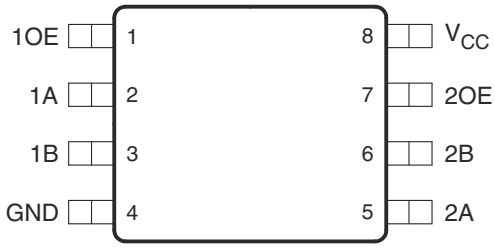


图 5-2. DCU Package
8-Pin VSSOP
Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	2	I/O	Channel 1 A port
1B	3	I/O	Channel 1 B port
1OE	1	I	Output Enable for switch 1
2A	5	I/O	Channel 2 A port
2B	6	I/O	Channel 2 B port
2OE	7	I	Output Enable for switch 2
GND	4	P	Ground
V_{cc}	8	P	Power supply

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_{IN}	Control input voltage(2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(6)			88	°C/W
T_j	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		SN74CB3Q3305 DCU (VSSOP) 8 PINS	SN74CB3Q3305 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	183	190.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.2	74.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.5	119.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.3	120.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.1	117.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = –18 mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	µA
I_{OZ} [3]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.25	0.7	mA
ΔI_{CC} [4]	Control inputs	V_{CC} = 3.6 V, One input at 3 V, Other inputs at V_{CC} or GND					25	µA
I_{CCD} [5]	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,			0.040	0.045	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		8	10.5	pF
r_{on} [6]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0, I_O = 30 mA			3	8	Ω
			V_I = 1.7 V, I_O = –15 mA			3.5	9	
		V_{CC} = 3 V	V_I = 0, I_O = 30 mA			3	6	
			V_I = 2.4 V, I_O = –15 mA			3.5	8	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see 图 9-2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{OE} (1)	OE	A or B	V_{CC} = 2.5 V ± 0.2 V		10	MHz
			V_{CC} = 3.3 V ± 0.3 V		20	
t_{pd} (2)	A or B	B or A	V_{CC} = 2.5 V ± 0.2 V		0.09	ns
			V_{CC} = 3.3 V ± 0.3 V		0.15	
t_{en}	OE	A or B	V_{CC} = 2.5 V ± 0.2 V	1	5	ns
			V_{CC} = 3.3 V ± 0.3 V	1	4.5	
t_{dis}	OE	A or B	V_{CC} = 2.5 V ± 0.2 V	1	4.5	ns
			V_{CC} = 3.3 V ± 0.3 V	1	5	

(1) Maximum switching frequency for control input (V_O > V_{CC}, V_I = 5 V, R_L ⩾ 1 MΩ, C_L = 0).
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.7 Typical Characteristics

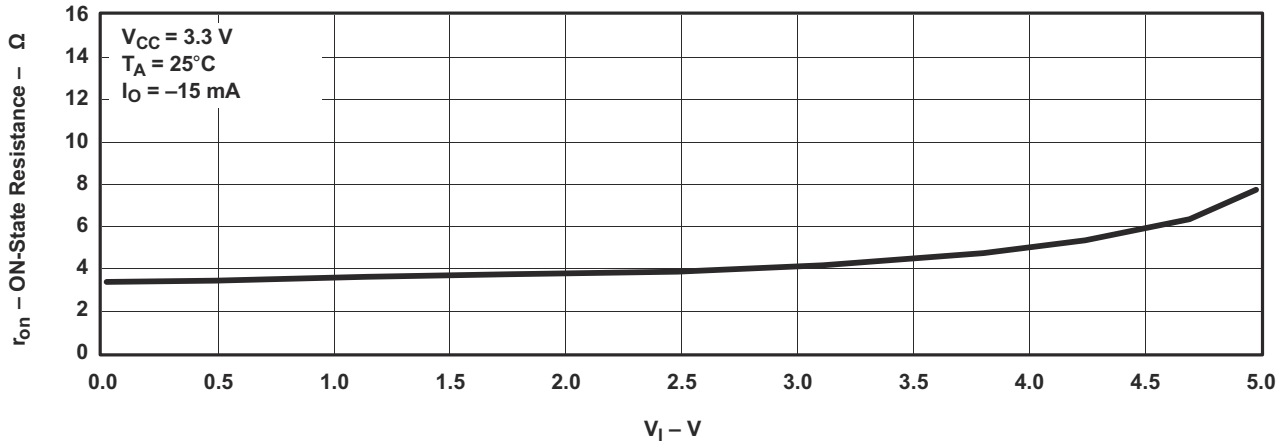
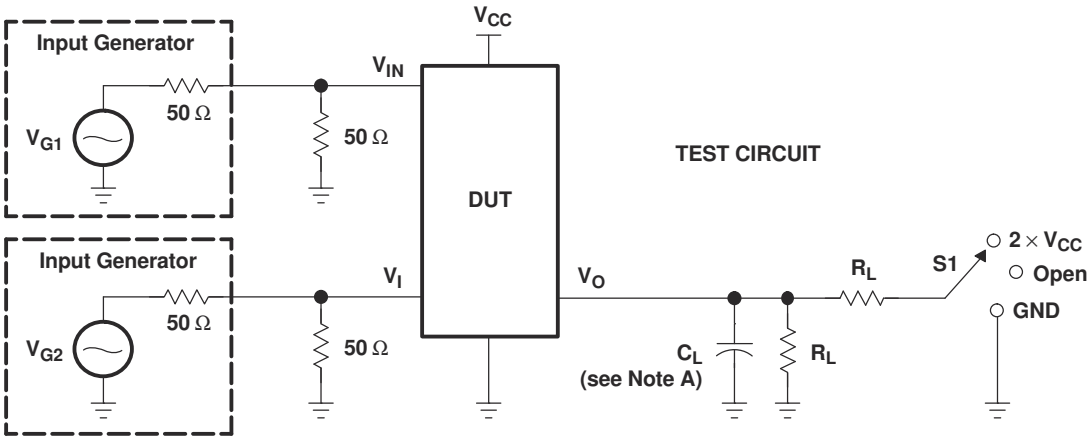
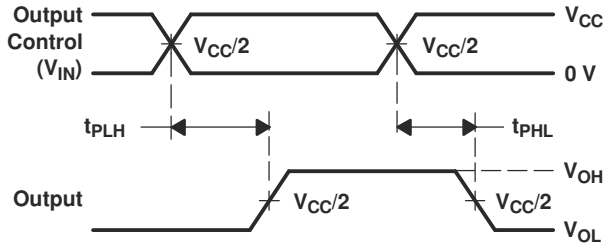


图 6-1. Typical r_{on} vs V_I

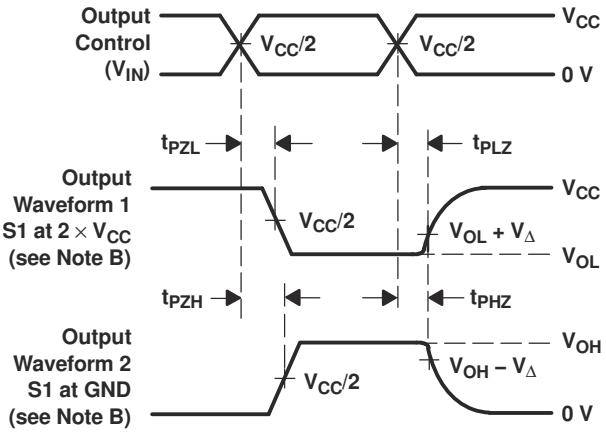
7 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

图 7-1. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74CB3Q3305 device is organized as two 1-bit switches with separate output-enable (1OE and 2OE) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When OE is high, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low, the associated 1-bit bus switch is OFF and a high-impedance state exists between the A and B ports.

8.2 Functional Block Diagram

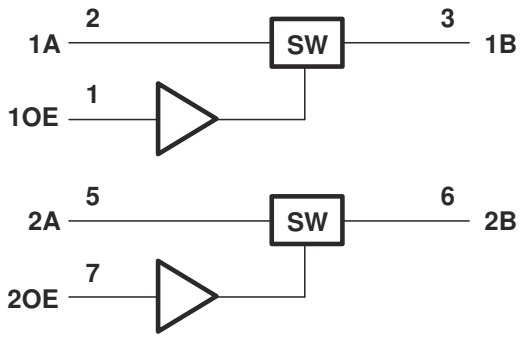


图 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The device supports High-Bandwidth data path up to 500 MHz. The I/O ports are 5 V tolerant when powered up or powered down due to I_{OFF}. The charge pump creates low and flat ON-state resistance characteristics over the whole operating temperature range.

Switching input voltage beyond the supply is supported on data I/O ports: 0 V to 5 V with 3.3 V V_{CC} or 0 V to 3.3 V with 2.5 V V_{CC}.

The data flow is bidirectional with near-zero propagation delay. Reduced input/output capacitance for higher speed applications. OE can be toggled at the high speeds of 20 MHz for fast switching applications.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74CB3Q3305.

表 8-1. Function Table (Each Bus Switch)

INPUT OE	INPUT/OUTPUT A	FUNCTION
H	B	A port = B port
L	Z	Disconnect

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

图 9-1 shows that the SN74CB3Q3305 can be used as bidirectional switch. The controller operates at 5 V and the peripheral can accept 5 V. Even with a V_{CC} of 3 V on the SN74CB3Q3305, the two ports can be connected to pass the 5 V signal. The controller uses the OE pin control the switch. This is a very generic example and could apply to many situations. For applications that require only 1 bit (for example, one channel), tie the unused OE low and tie the unused ports A and B to either high or low (not shown).

9.2 Typical Application

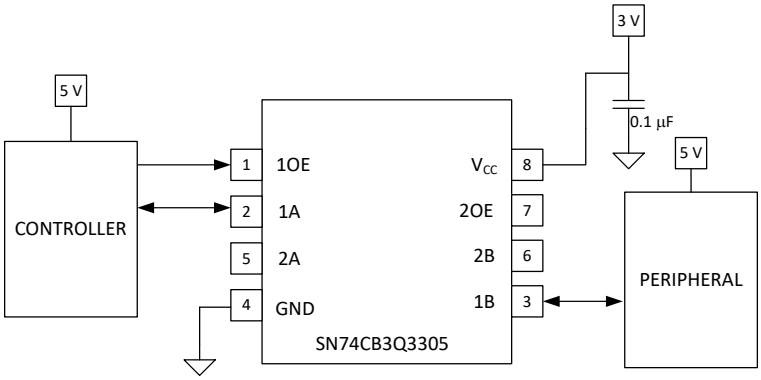


图 9-1. Typical Application of the SN74CB3Q3305

9.2.1 Design Requirements

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in 节 6.3.
   - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Absolute Maximum Conditions:
   - I/O currents should not exceed ±64 mA per channel.
   - Continuos current through GND or V_{CC} should not exceed ±100 mA.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 500 MHz.
   - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in 节 11.

9.2.2 Detailed Design Procedure

The 0.1 µF capacitor should be placed as close as possible to the device.

9.2.3 Application Curve

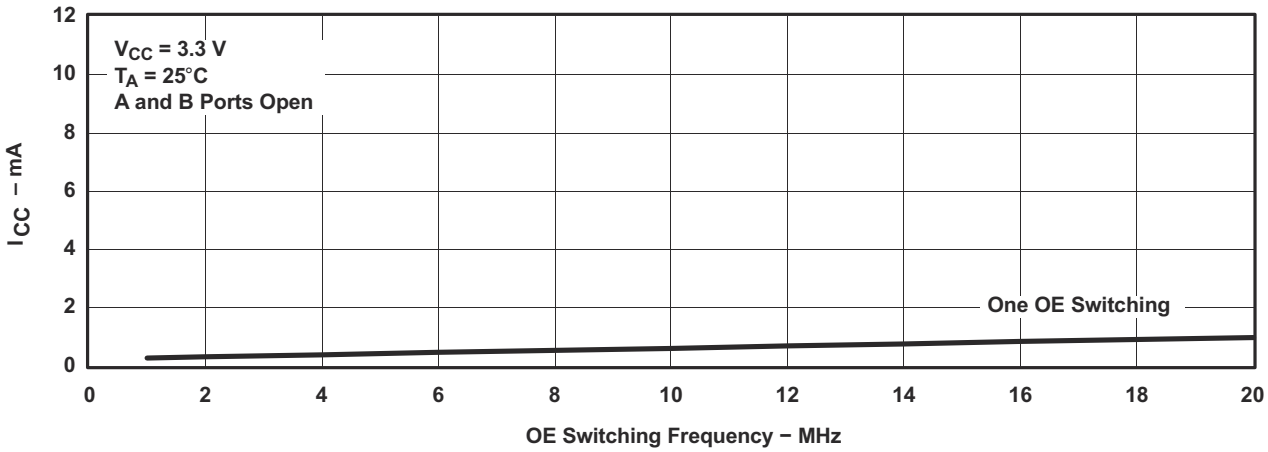


图 9-2. Typical I_{CC} vs OE Switching Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in 节 6.1 table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01 μF or 0.022 μF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1 μF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self‐inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

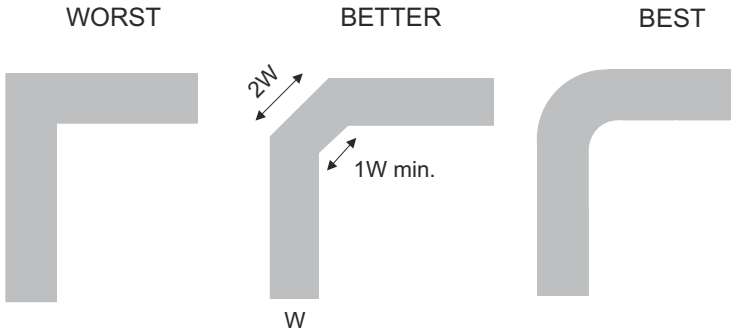


图 11-1. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *CBT-C, CB3T, and CB3Q Signal-Switch Families* application report
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Selecting the Right Texas Instruments Signal Switch* application report

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74CB3Q3305DCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GARR
SN74CB3Q3305DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(GARQ, GARR)
SN74CB3Q3305PW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	BU305
SN74CB3Q3305PWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	BU305
SN74CB3Q3305PWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

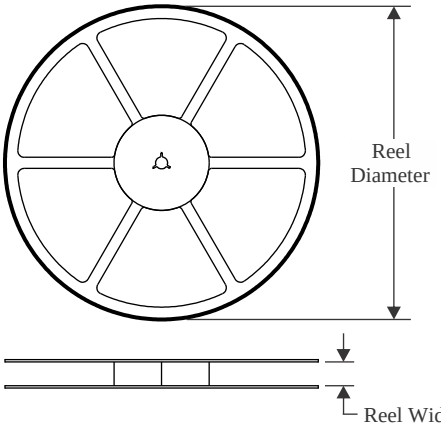
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

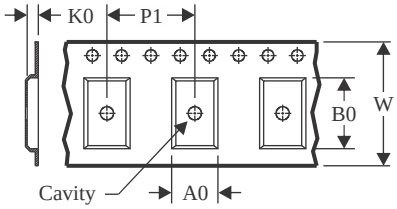
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

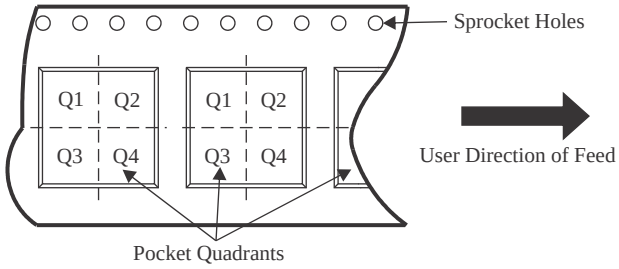


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

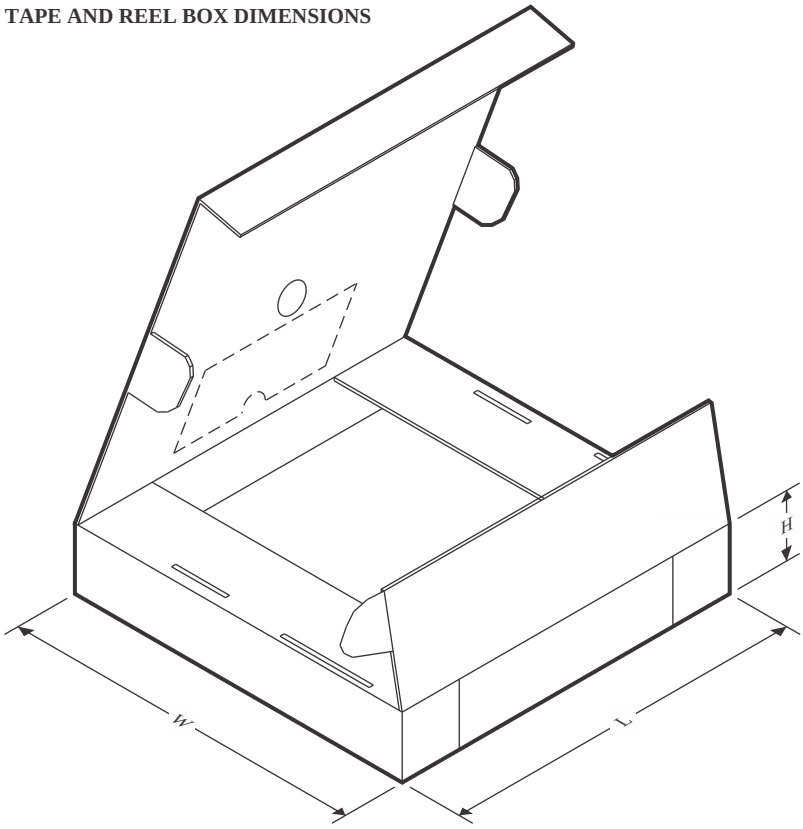
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CB3Q3305DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3305DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3305PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN74CB3Q3305PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

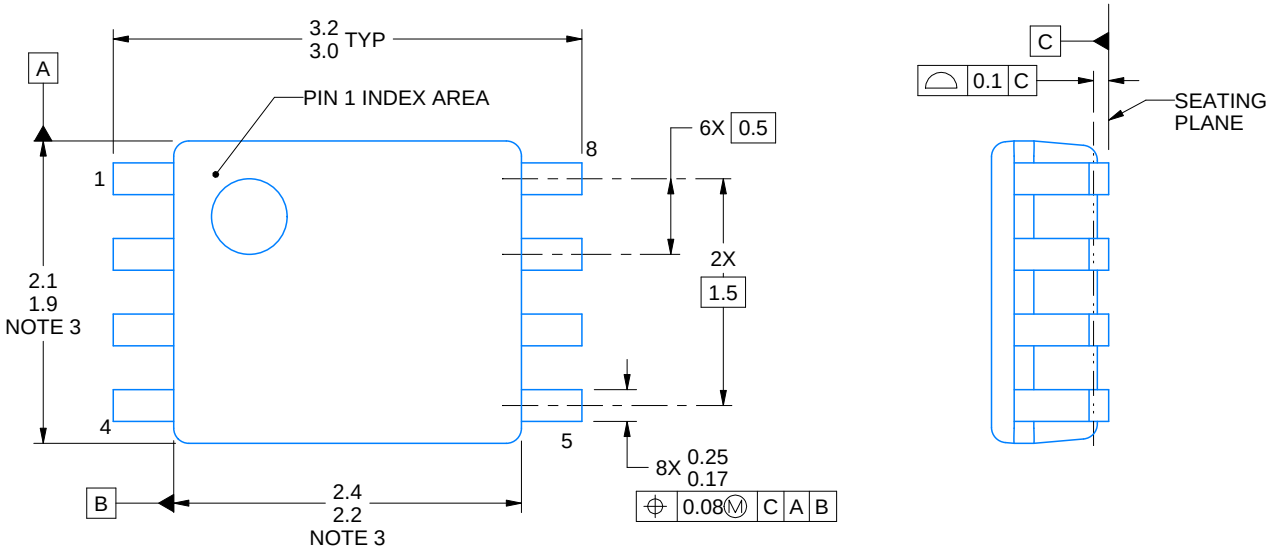
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CB3Q3305DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3305DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74CB3Q3305PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
SN74CB3Q3305PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0

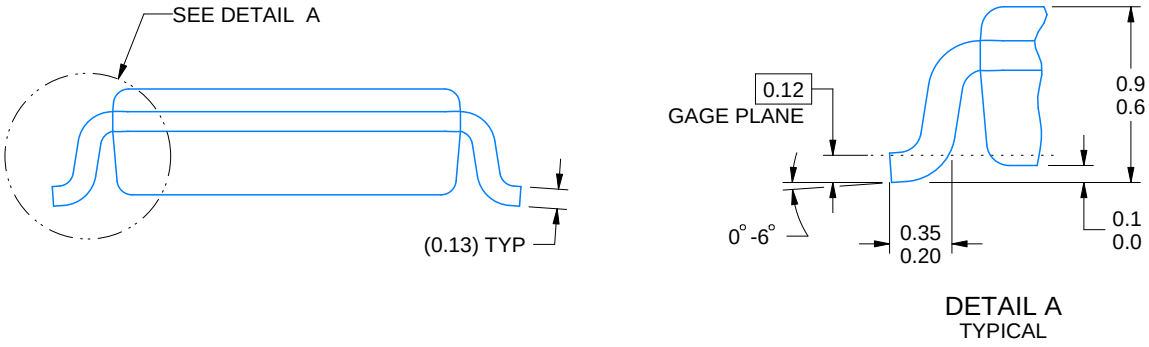
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

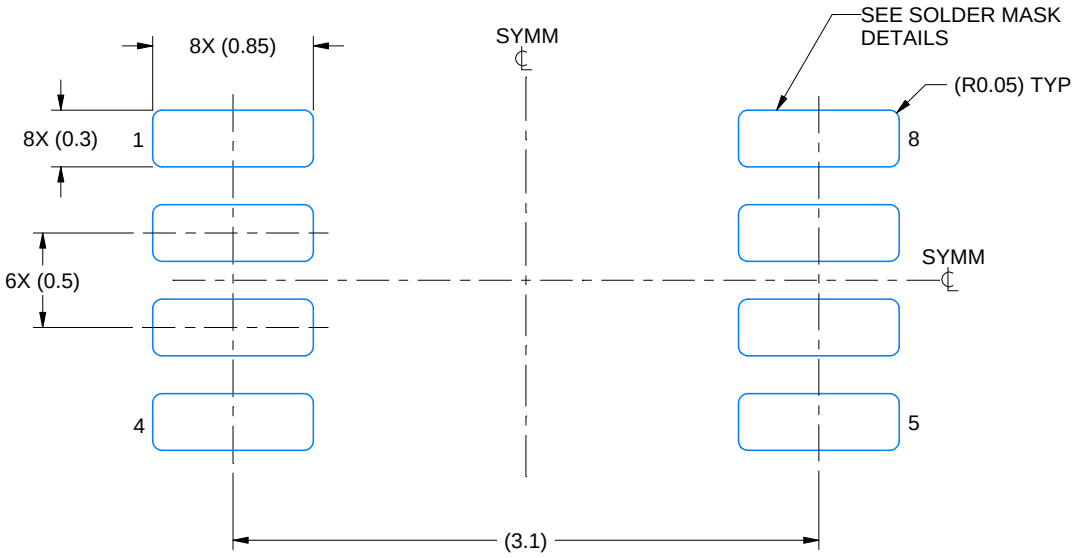




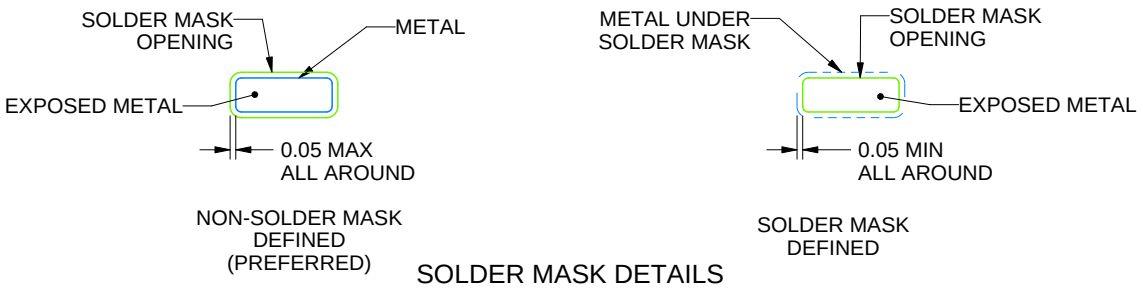
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

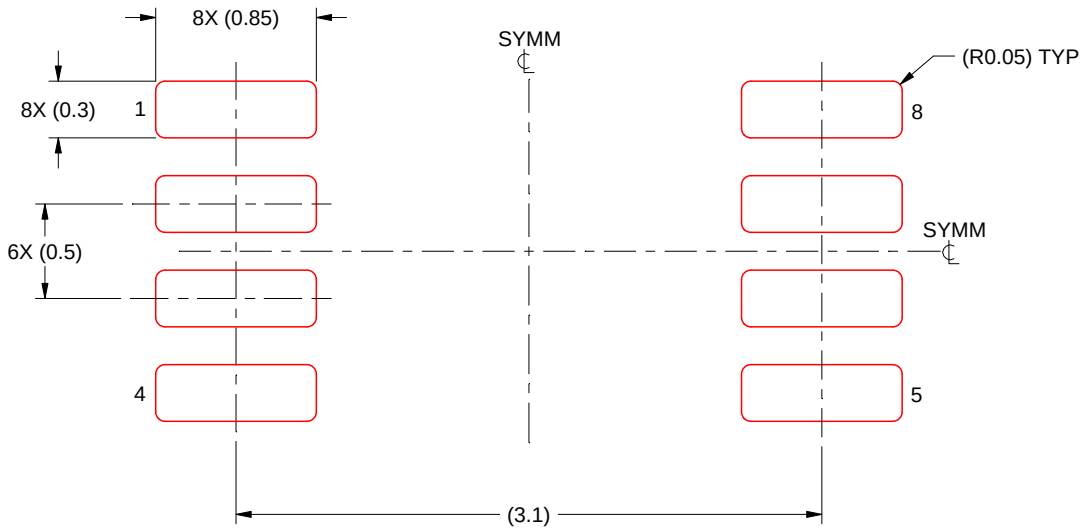


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

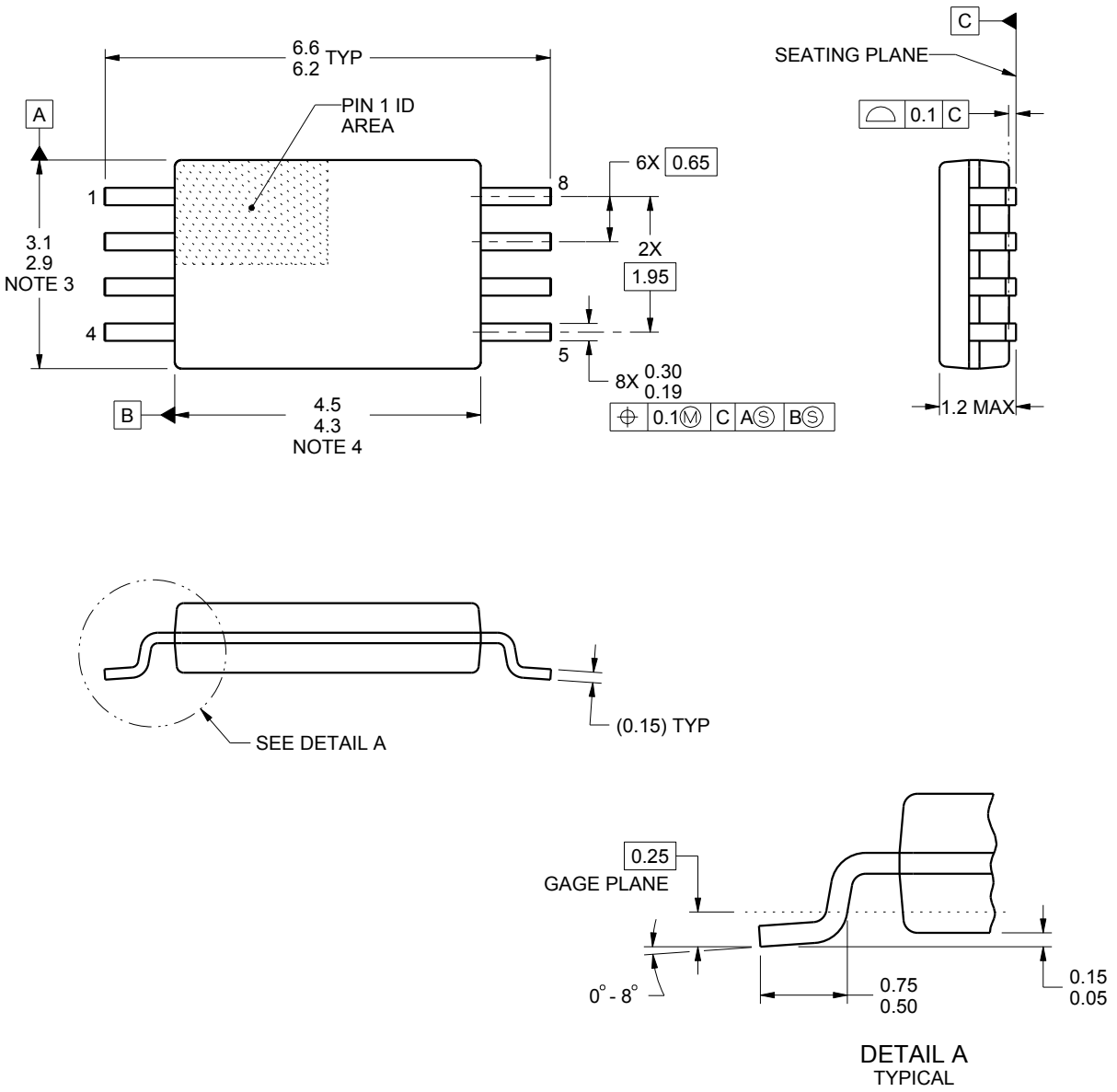
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

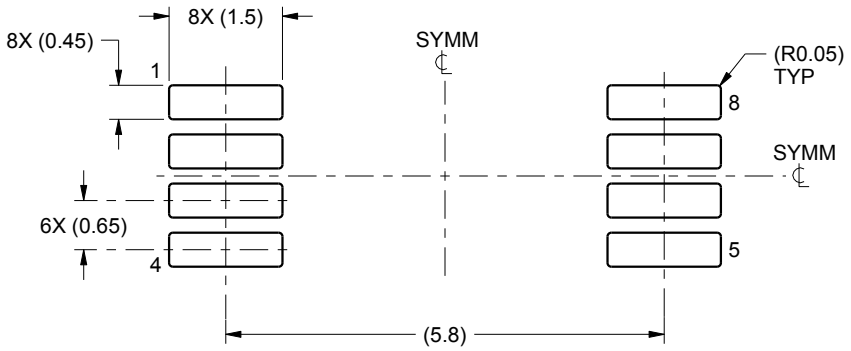
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

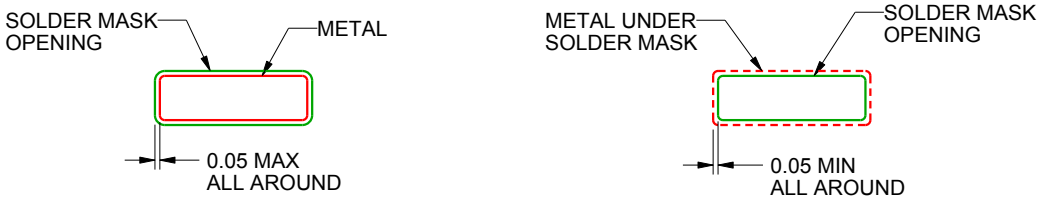


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

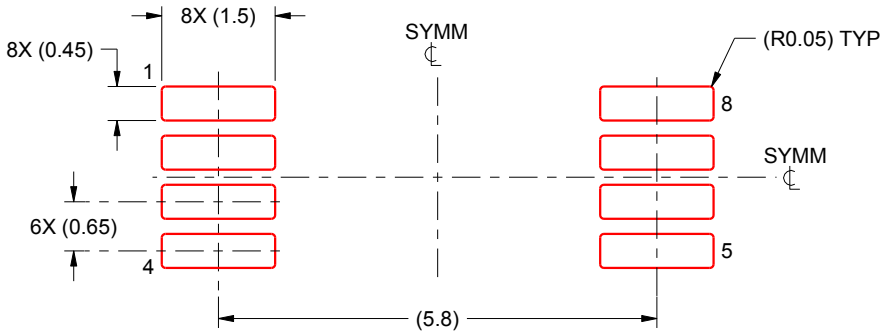


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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