LMV796/LMV796Q/LMV797 17 MHz, Low Noise, CMOS Input, 1.8V Operational Amplifiers

Check for Samples: LMV796, LMV797

FEATURES

(Typical 5V Supply, Unless Otherwise Noted)

- **Input Referred Voltage Noise 5.8 nV/√Hz**
- **Input Bias Current 100 fA**
- **Unity Gain Bandwidth 17 MHz**
- **Supply Current per Channel**
  - **LMV796/LMV796Q 1.15 mA**
  - **LMV797 1.30 mA**
- **Rail-to-Rail Output Swing**
  - **@ 10 kΩ Load 25 mV from Rail**
  - **@ 2 kΩ Load 45 mV from Rail**
- **Guaranteed 2.5V and 5.0V Performance**
- **Total Harmonic Distortion 0.01% @ 1kHz, 600Ω**
- **Temperature Range −40°C to 125°C**
- **LMV796Q is an Automotive Grade Product that is AEC-Q100 Grade 1 Qualified and is Manufactured on an Automotive Grade Flow.**

APPLICATIONS

- **Photodiode Amplifiers**
- **Active Filters and Buffers**
- **Low Noise Signal Processing**
- **Medical Instrumentation**
- **Sensor Interface Applications**
- **Automotive**

DESCRIPTION

The LMV796/LMV796Q (Single) and the LMV797 (Dual) low noise, CMOS input operational amplifiers offer a low input voltage noise density of 5.8 nV/√Hz while consuming only 1.15 mA (LMV796/LMV796Q) of quiescent current. The LMV796/LMV796Q and LMV797 are unity gain stable op amps and have gain bandwidth of 17 MHz. The LMV796/LMV796Q/ LMV797 have a supply voltage range of 1.8V to 5.5V and can operate from a single supply. The LMV796/LMV796Q/LMV797 each feature a rail-to-rail output stage capable of driving a 600Ω load and sourcing as much as 60 mA of current.

The LMV796/LMV796Q family provides optimal performance in low voltage and low noise systems. A CMOS input stage, with typical input bias currents in the range of a few femtoAmperes, and an input common mode voltage range, which includes ground, make the LMV796/LMV796Q and the LMV797 ideal for low power sensor applications.

The LMV796/LMV796Q/LMV797 are manufactured using TI's advanced VIP50 process. The LMV796/ LMV796Q are offered in 5–pin SOT-23 package. The LMV797 is offered in 8–pin VSSOP package.

Typical Application

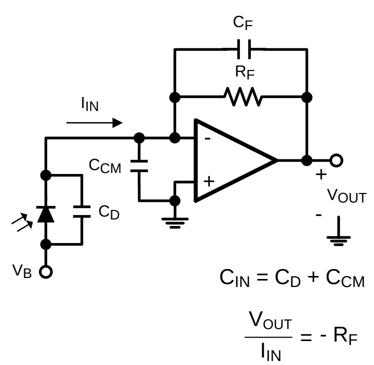


Figure 1. Photodiode Transimpedance Amplifier

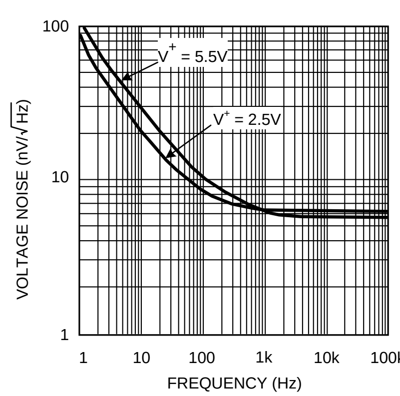


Figure 2. Input Referred Voltage Noise vs. Frequency

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	Human Body Model	2000V
	Machine Model	200V
	Charge-Device Model	1000V
V_{IN} Differential		±0.3V
Supply Voltage ($V^+ - V^-$)		6.0V
Input/Output Pin Voltage		V^+ +0.3V, V^- −0.3V
Storage Temperature Range		−65°C to 150°C
Junction Temperature (4)		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temperature (10 sec)	260°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics* tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model is 1.5kΩ in series with 100pF. Machine Model is 0Ω in series with 200pF.
(4) The maximum power dissipation is a function of T_{JMAX}, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{JMAX} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings (1)

Temperature Range (2)		−40°C to 125°C
Supply Voltage ($V^+ - V^-$)	$-40°C \le T_A \le 125°C$	2.0V to 5.5V
	$0°C \le T_A \le 125°C$	1.8V to 5.5V
Package Thermal Resistance (θ_{JA}) (2)	5-Pin SOT-23	180°C/W
	8-Pin VSSOP	236°C/W

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics* tables.
(2) The maximum power dissipation is a function of T_{JMAX}, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{JMAX} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

2.5V Electrical Characteristics

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.5V, V^- = 0V, $V_{CM} = V^+/2 = V_O$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage				0.1	±1.35 **±1.65**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	LMV796/LMV796Q (3)			−1.0		μV/°C
		LMV797 (3)			−1.8		
I_B	Input Bias Current	V_{CM} = 1.0V (4) (5)	$-40°C \le T_A \le 85°C$		0.05	1 **25**	pA
			$-40°C \le T_A \le 125°C$		0.05	1 **100**	
I_{OS}	Input Offset Current	V_{CM} = 1.0V (5)			10		fA

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the statistical quality control (SQC) method.
(2) Typical values represent the parametric norm at the time of characterization.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} by temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) This parameter is specified by design and/or characterization and is not tested in production.

2.5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.4V	80 **75**	94		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V, V_{CM} = 0V	80 **75**	100		dB
		1.8V ≤ V^+ ≤ 5.5V, V_{CM} = 0V	80	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 60 dB CMRR ≥ 55 dB	−0.3 **-0.3**		1.5 **1.5**	V
A_{VOL}	Open Loop Voltage Gain	V_{OUT} = 0.15V to 2.2V, R_{LOAD} = 2 kΩ to $V^+/2$; LMV796/LMV796Q	85 **80**	98		dB
		V_{OUT} = 0.15V to 2.2V, R_{LOAD} = 2 kΩ to $V^+/2$; LMV797	82 **78**	92		
		V_{OUT} = 0.15V to 2.2V, R_{LOAD} = 10 kΩ to $V^+/2$	88 **84**	110		
V_{OUT}	Output Voltage Swing High	R_{LOAD} = 2 kΩ to $V^+/2$		25	75 **82**	mV from either rail
		R_{LOAD} = 10 kΩ to $V^+/2$		20	65 **71**	
	Output Voltage Swing Low	R_{LOAD} = 2 kΩ to $V^+/2$		30	75 **78**	
		R_{LOAD} = 10 kΩ to $V^+/2$		15	65 **67**	
I_{OUT}	Output Current	Sourcing to V^- V_{IN} = 200 mV (6)	35 **28**	47		mA
		Sinking to V^+ V_{IN} = –200 mV (6)	7 **5**	15		
I_S	Supply Current per Amplifier	LMV796/LMV796Q		0.95	1.30 **1.65**	mA
		LMV797 per channel		1.1	1.50 **1.85**	
SR	Slew Rate	A_V = +1, Rising (10% to 90%)		8.5		V/µs
		A_V = +1, Falling (90% to 10%)		10.5		
GBW	Gain Bandwidth			14		MHz
e_n	Input Referred Voltage Noise Density	f = 1 kHz		6.2		nV/$\sqrt{Hz}$
i_n	Input Referred Current Noise Density	f = 1 kHz		0.01		pA/$\sqrt{Hz}$
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_{LOAD} = 600Ω		0.01		%

(6) The short circuit test is a momentary test, the short circuit duration is 1.5ms.

5V Electrical Characteristics

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			0.1	±1.35 **±1.65**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	LMV796/LMV796Q (3)		−1.0		µV/°C
		LMV797 (3)		−1.8		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the statistical quality control (SQC) method.
(2) Typical values represent the parametric norm at the time of characterization.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} by temperature change.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes.

I_B	Input Bias Current	V_{CM} = 2.0V (4) (5)	−40°C ≤ T_A ≤ 85°C		0.1	1 **25**	pA
			−40°C ≤ T_A ≤ 125°C		0.1	1 **100**	
I_{OS}	Input Offset Current	V_{CM} = 2.0V (5)			10		fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.7V		80 **75**	100		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		80 **75**	100		dB
		1.8V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		80	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 60 dB CMRR ≥ 55 dB		−0.3 **-0.3**		4 **4**	V
A_{VOL}	Open Loop Voltage Gain	V_{OUT} = 0.3V to 4.7V, R_{LOAD} = 2 kΩ to $V^+/2$	LMV796/LMV796Q	85 **80**	97		dB
			LMV797	82 **78**	89		
		V_{OUT} = 0.3V to 4.7V, R_{LOAD} = 10 kΩ to $V^+/2$		88 **84**	110		
V_{OUT}	Output Voltage Swing High	R_{LOAD} = 2 kΩ to $V^+/2$			35	75 **82**	mV from either rail
		R_{LOAD} = 10 kΩ to $V^+/2$			25	65 **71**	
	Output Voltage Swing Low	R_{LOAD} = 2 kΩ to $V^+/2$	LMV796/LM796Q		42	75 **78**	
			LMV797		45	80 **83**	
		R_{LOAD} = 10 kΩ to $V^+/2$			20	65 **67**	
I_{OUT}	Output Current	Sourcing to V^- V_{IN} = 200 mV (6)		45 **37**	60		mA
		Sinking to V^+ V_{IN} = –200 mV (6)		10 **6**	21		
I_S	Supply Current per Amplifier	LMV796/LMV796Q			1.15	1.40 **1.75**	mA
		LMV797per channel			1.30	1.70 **2.05**	
SR	Slew Rate	A_V = +1, Rising (10% to 90%)		6.0	9.5		V/μs
		A_V = +1, Falling (90% to 10%)		7.5	11.5		
GBW	Gain Bandwidth				17		MHz
e_n	Input Referred Voltage Noise Density	f = 1 kHz			5.8		$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise Density	f = 1 kHz			0.01		$pA/\sqrt{Hz}$
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_{LOAD} = 600Ω			0.01		%

(4) Positive current corresponds to current flowing into the device.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) The short circuit test is a momentary test, the short circuit duration is 1.5ms.

Connection Diagram

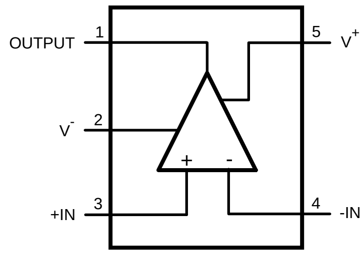


Figure 3. 5-Pin SOT-23 Top View

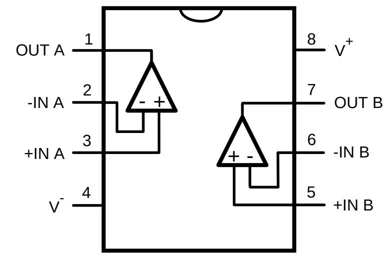


Figure 4. 8-Pin VSSOP Top View

Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = $V^+/2$.

Supply Current vs. Supply Voltage (LMV796/LMV796Q)

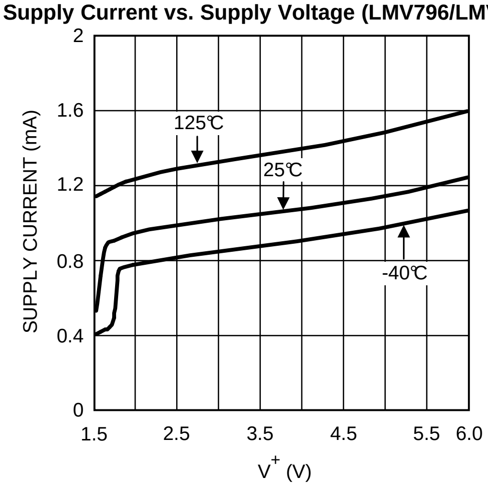


Figure 5.

Supply Current vs. Supply Voltage (LMV797)

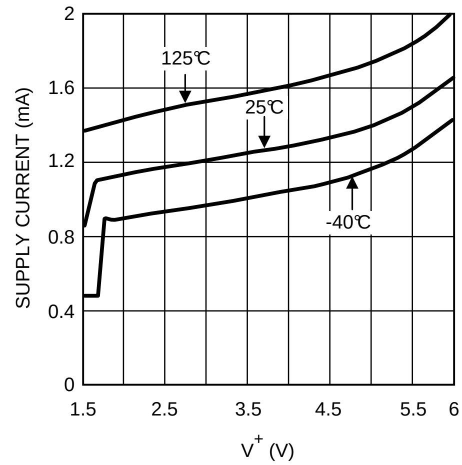


Figure 6.

V_{OS} vs. V_{CM}

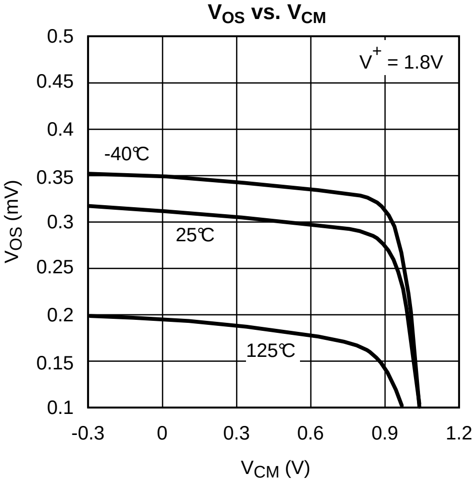


Figure 7.

V_{OS} vs. V_{CM}

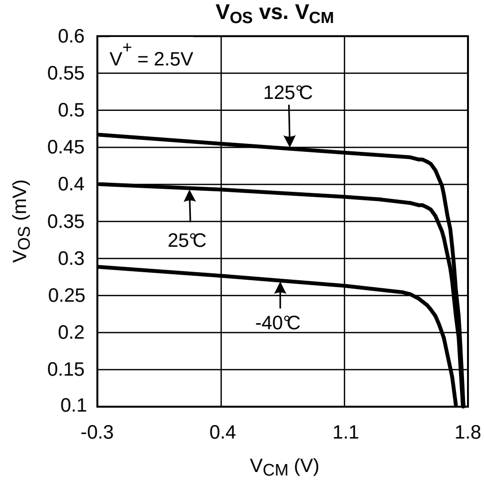


Figure 8.

V_{OS} vs. V_{CM}

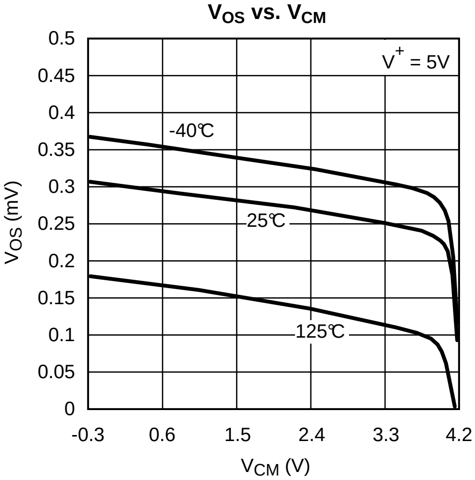


Figure 9.

V_{OS} vs. Supply Voltage

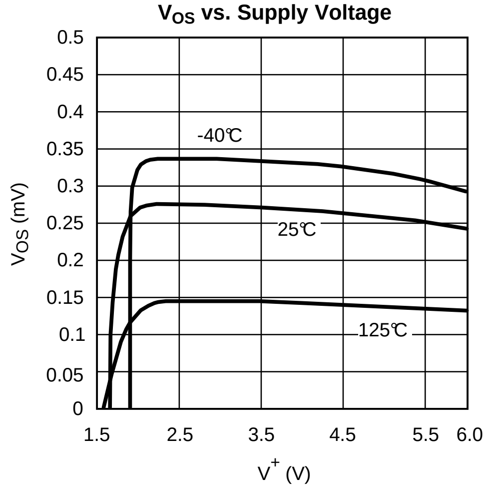


Figure 10.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.

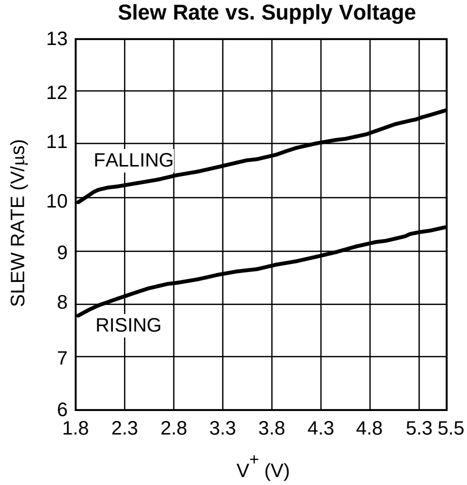
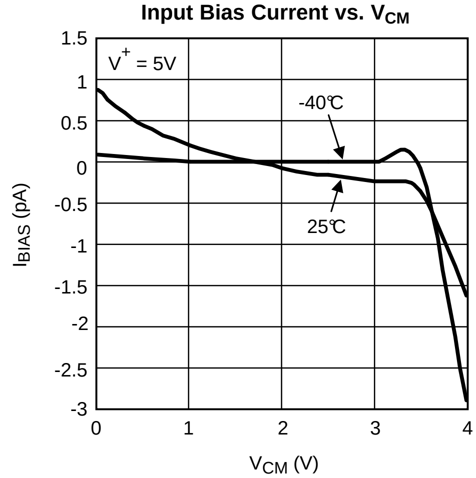


Figure 11.



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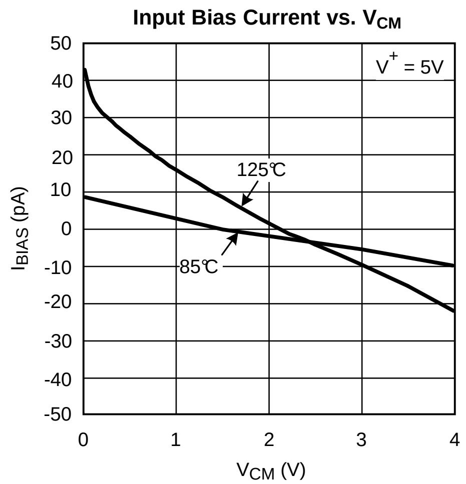

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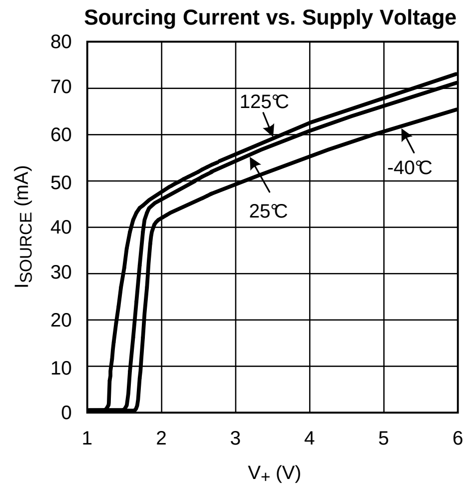

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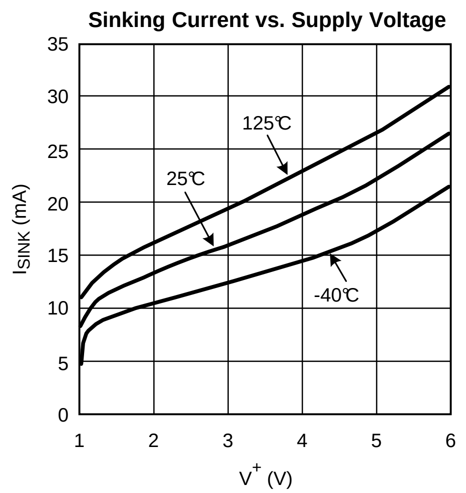

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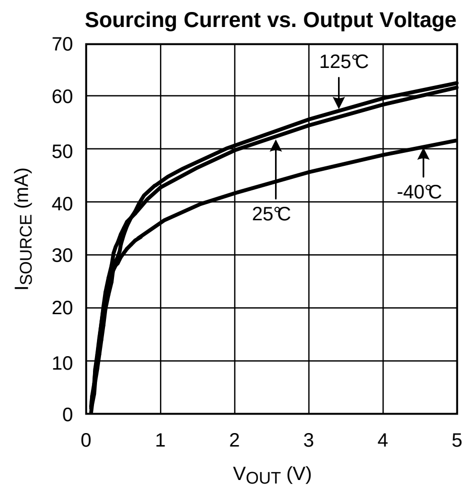
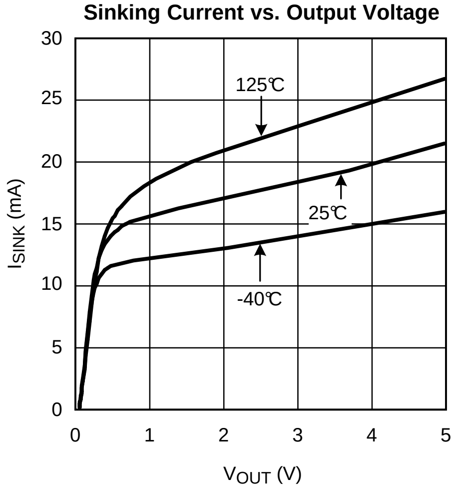


Figure 16.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.



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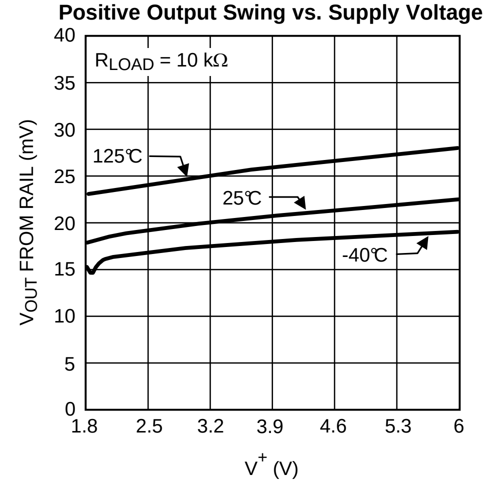


Figure 18.

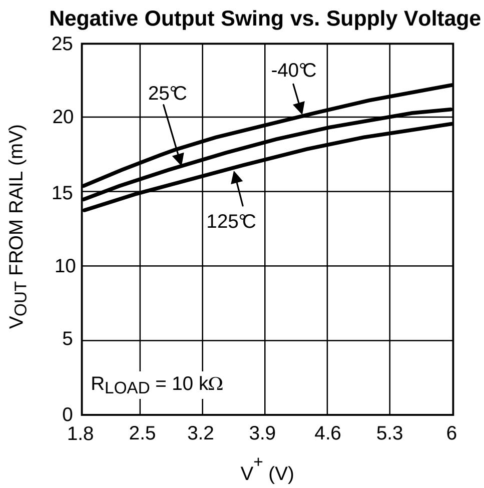
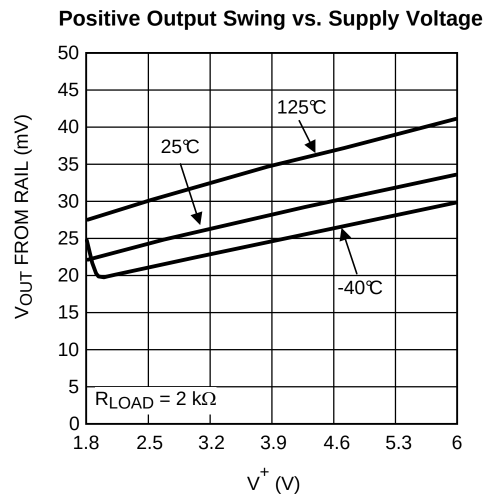


Figure 19.



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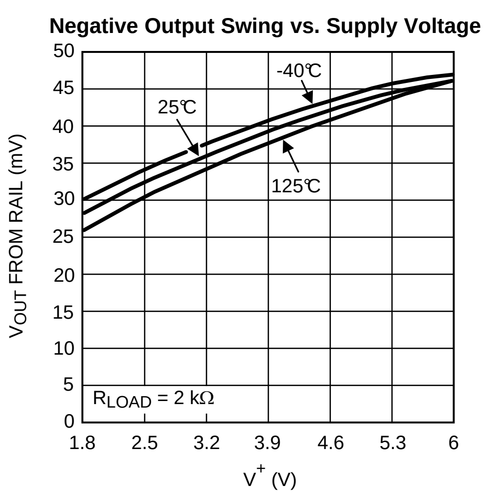

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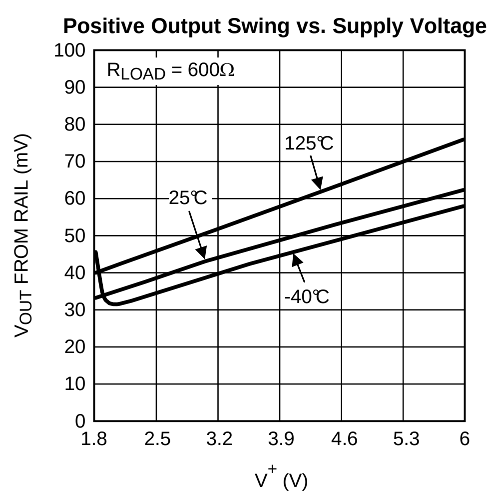


Figure 22.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.

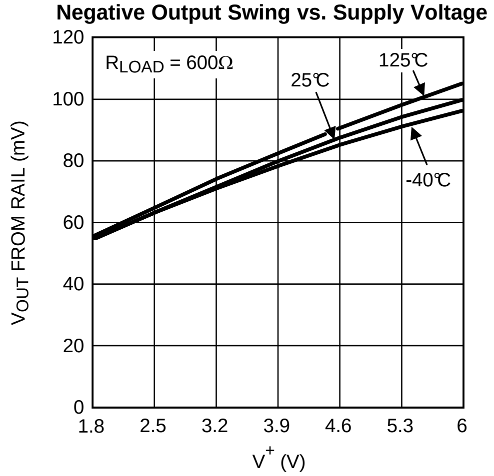
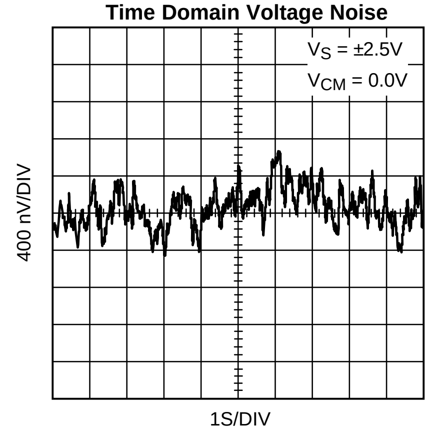


Figure 23.



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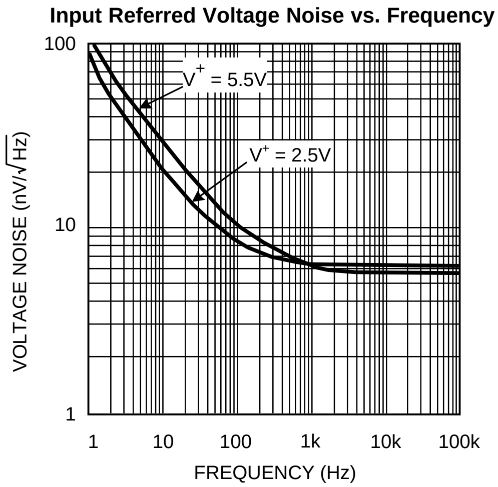

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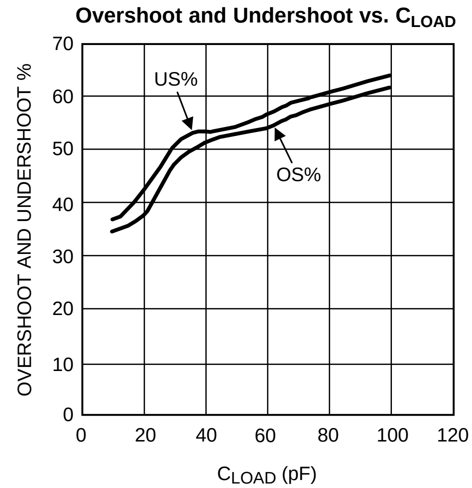

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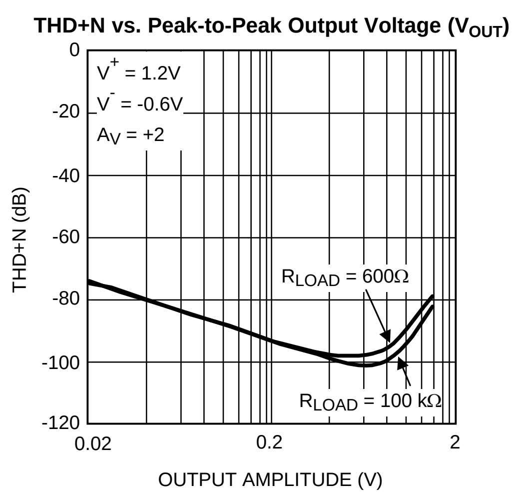

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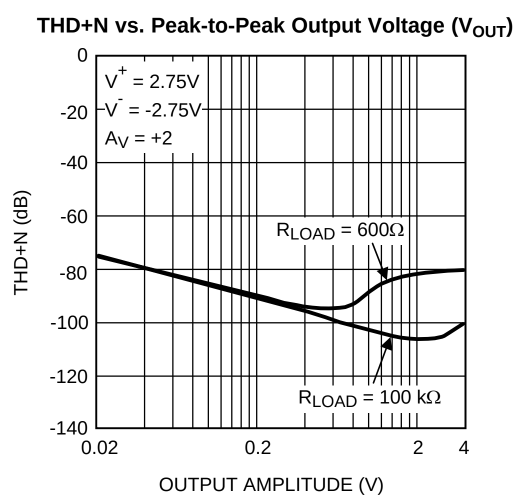
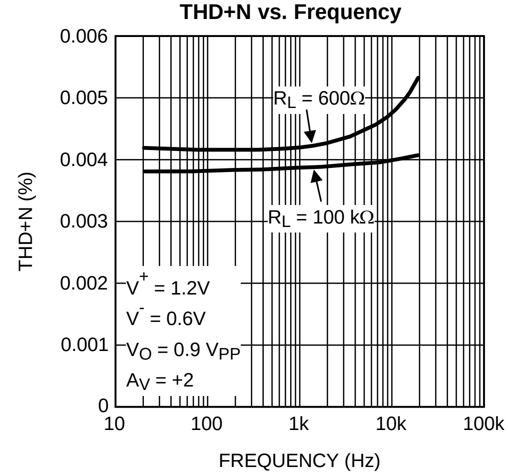


Figure 28.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.



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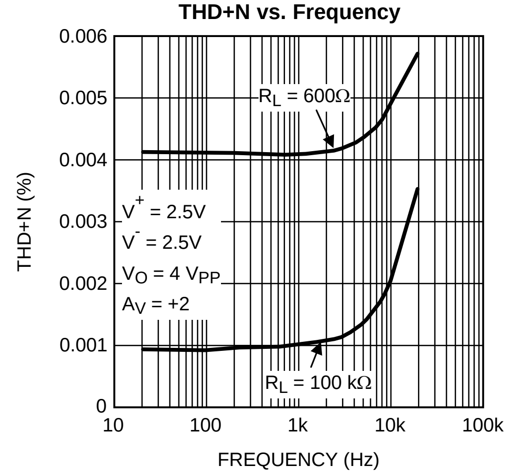
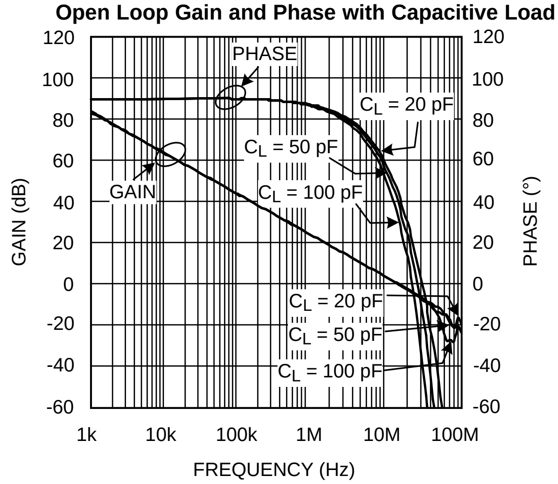


Figure 30.



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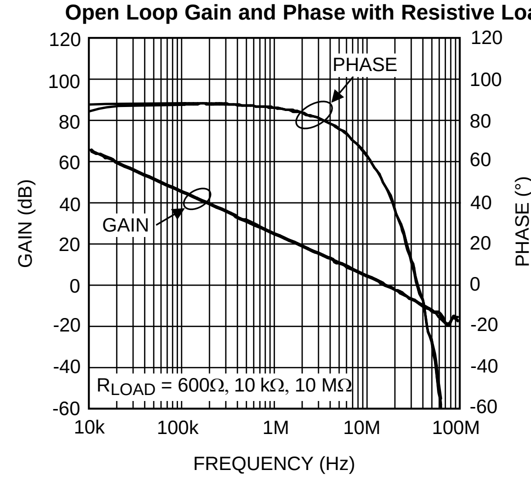


Figure 32.

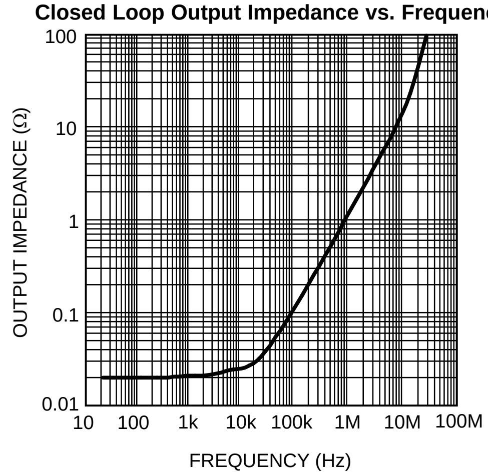


Figure 33.

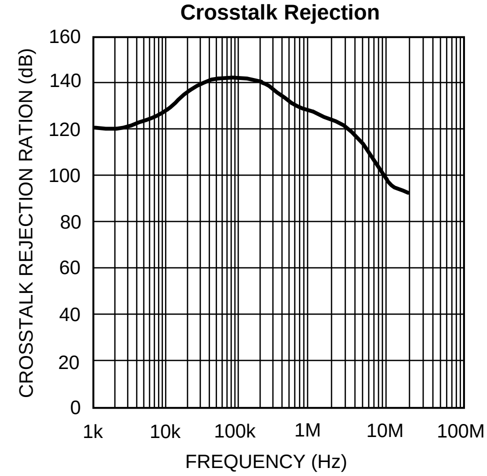


Figure 34.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.

Small Signal Transient Response, A_V = +1

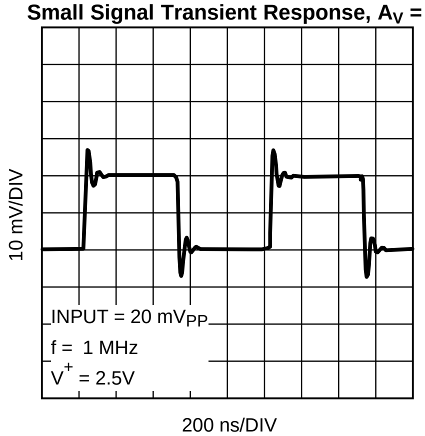


Figure 35.

Large Signal Transient Response, A_V = +1

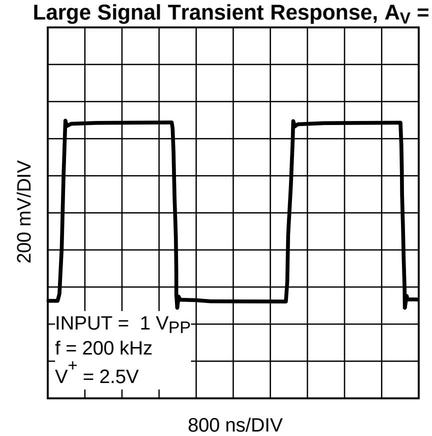


Figure 36.

Small Signal Transient Response, A_V = +1

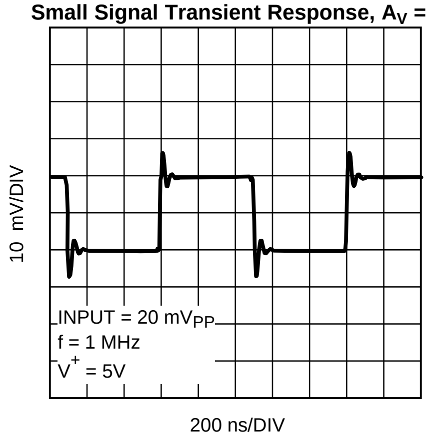


Figure 37.

Large Signal Transient Response, A_V = +1

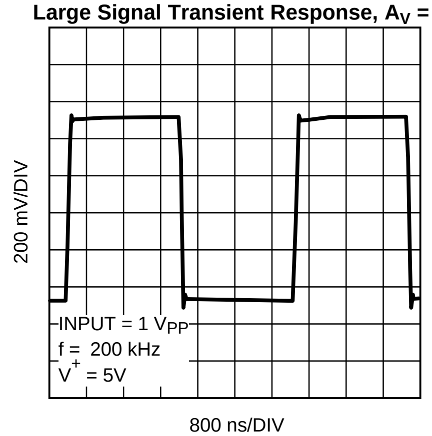


Figure 38.

Phase Margin vs. Capacitive Load (Stability)

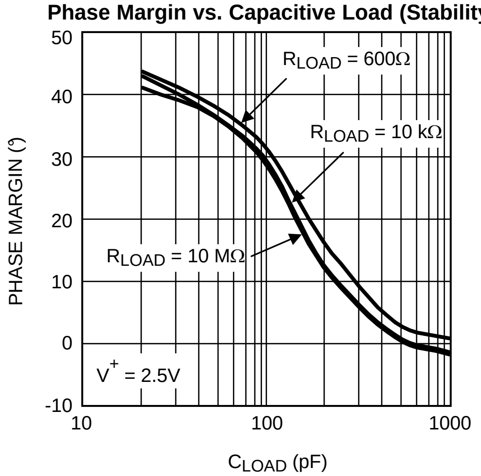


Figure 39.

Phase Margin vs. Capacitive Load (Stability)

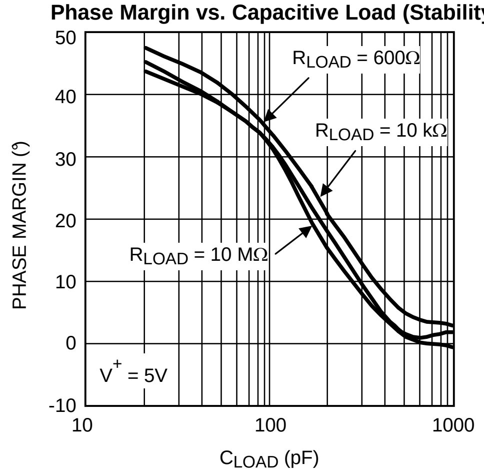


Figure 40.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.

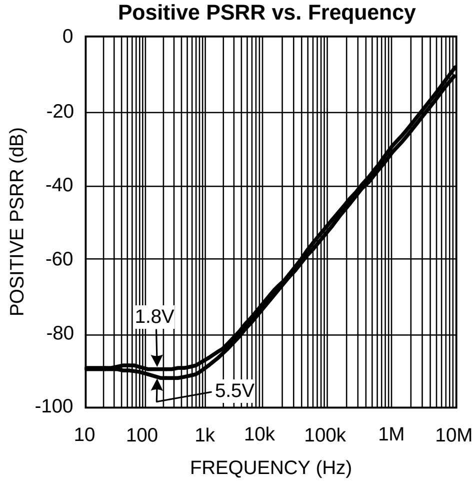


Figure 41.

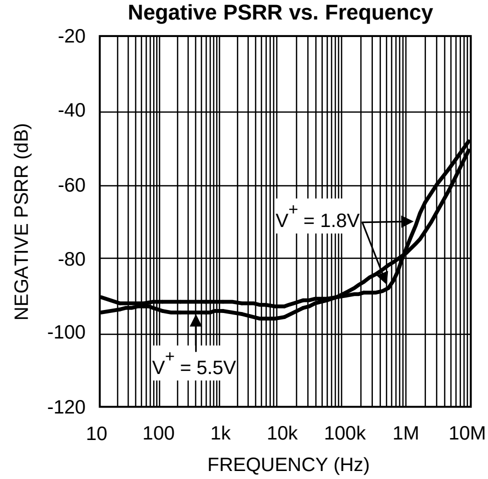


Figure 42.

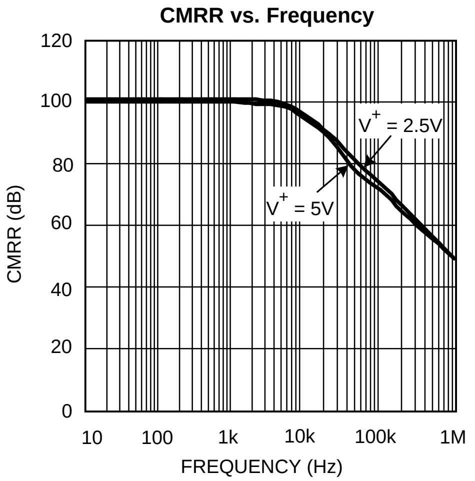


Figure 43.

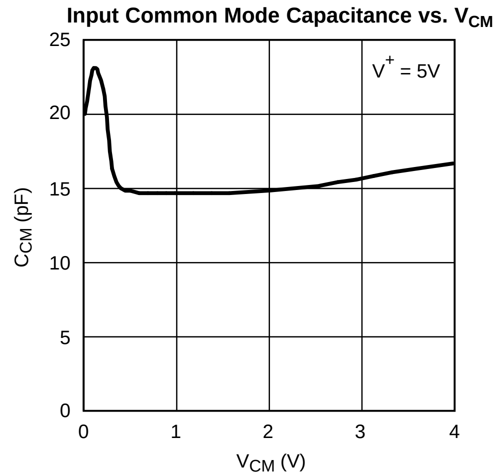


Figure 44.

APPLICATION INFORMATION

ADVANTAGES OF THE LMV796/LMV797

Wide Bandwidth at Low Supply Current

The LMV796 and LMV797 are high performance op amps that provide a unity gain bandwidth of 17 MHz while drawing a low supply current of 1.15 mA. This makes them ideal for providing wideband amplification in portable applications.

Low Input Referred Noise and Low Input Bias Current

The LMV796/LMV797 have a very low input referred voltage noise density (5.8 nV/$\sqrt{\text{Hz}}$ at 1 kHz). A CMOS input stage ensures a small input bias current (100 fA) and low input referred current noise (0.01 pA/$\sqrt{\text{Hz}}$). This is very helpful in maintaining signal fidelity, and makes the LMV796 and LMV797 ideal for audio and sensor based applications.

Low Supply Voltage

The LMV796 and the LMV797 have performance specified at 2.5V and 5V supply. The LMV796 family is specified to be operational at all supply voltages between 2.0V and 5.5V, for ambient temperatures ranging from −40°C to 125°C, thus utilizing the entire battery lifetime. The LMV796 and LMV797 are also specified to be operational at 1.8V supply voltage, for temperatures between 0°C and 125°C. This makes the LMV796 family ideal for usage in low-voltage commercial applications.

RRO and Ground Sensing

Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating at low supply voltages. An innovative positive feedback scheme is used to boost the current drive capability of the output stage. This allows the LMV796 and the LMV797 to source more than 40 mA of current at 1.8V supply. This also limits the performance of the LMV796 family as comparators, and hence the usage of the LMV796 and the LMV797 in an open-loop configuration is not recommended. The input common-mode range includes the negative supply rail which allows direct sensing at ground in single supply operation.

Small Size

The small footprint of the LMV796 and the LMV797 package saves space on printed circuit boards, and enables the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. Long traces between the signal source and the op amp make the signal path susceptible to noise. By using the physically smaller LMV796 or LMV797 package, the op amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

CAPACITIVE LOAD TOLERANCE

The LMV796 and LMV797 can directly drive 120 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, the circuit in Figure 45 can be used.

In Figure 45, the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Increased R_{ISO} would, however, result in a reduced output swing and short circuit current.

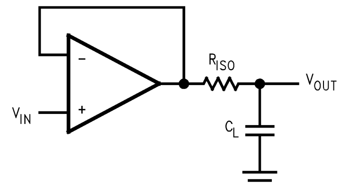
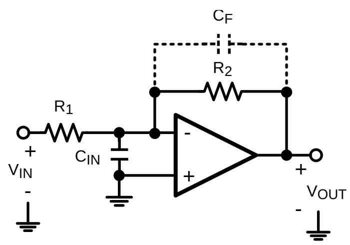


Figure 45. Isolation of C_L to Improve Stability

INPUT CAPACITANCE AND FEEDBACK CIRCUIT ELEMENTS

The LMV796 family has a very low input bias current (100 fA) and a low 1/f noise corner frequency (400 Hz), which makes it ideal for sensor applications. However, to obtain this performance a large CMOS input stage is used, which adds to the input capacitance of the op amp, C_{IN}. Though this does not affect the DC and low frequency performance, at higher frequencies the input capacitance interacts with the input and the feedback impedances to create a pole, which results in lower phase margin and gain peaking. This can be controlled by being selective in the use of feedback resistors, as well as, by using a feedback capacitance, C_F. For example, in the inverting amplifier shown in Figure 46, if C_{IN} and C_F are ignored and the open loop gain of the op amp is considered infinite then the gain of the circuit is $-R_2/R_1$. An op amp, however, usually has a dominant pole, which causes its gain to drop with frequency. Hence, this gain is only valid for DC and low frequency. To understand the effect of the input capacitance coupled with the non-ideal gain of the op amp, the circuit needs to be analyzed in the frequency domain using a Laplace transform.



$$A_V = -\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}$$

Figure 46. Inverting Amplifier

For simplicity, the op amp is modeled as an ideal integrator with a unity gain frequency of A_0 . Hence, its transfer function (or gain) in the frequency domain is A_0/s. Solving the circuit equations in the frequency domain, ignoring C_F for the moment, results in an expression for the gain shown in Equation 1.

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}\right]} \tag{1}$$

It can be inferred from the denominator of the transfer function that it has two poles, whose expressions can be obtained by solving for the roots of the denominator and are shown in Equation 2.

$$P_{1,2} = \frac{-1}{2C_{IN}}\left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4 A_0 C_{IN}}{R_2}}\right] \tag{2}$$

Equation 2 shows that as the values of R_1 and R_2 are increased, the magnitude of the poles, and hence the bandwidth of the amplifier, is reduced. This theory is verified by using different values of R_1 and R_2 in the circuit shown in Figure 45 and by comparing their frequency responses. In Figure 47 the frequency responses for three different values of R_1 and R_2 are shown. When both R_1 and R_2 are 1 kΩ, the response is flattest and widest; whereas, it narrows and peaks significantly when both their values are changed to 10 kΩ or 30 kΩ. So it is advisable to use lower values of R_1 and R_2 to obtain a wider and flatter response. Lower resistances also help in high sensitivity circuits since they add less noise.

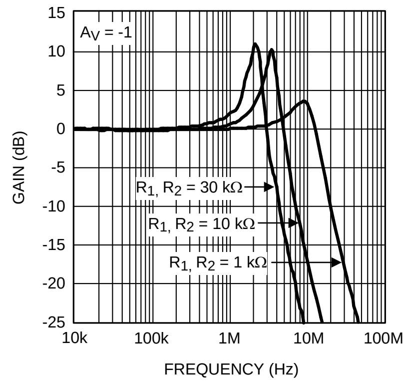


Figure 47. Gain Peaking Caused by Large R_1, R_2

A way of reducing the gain peaking is by adding a feedback capacitance C_F in parallel with R_2. This introduces another pole in the system and prevents the formation of pairs of complex conjugate poles which cause the gain to peak. Figure 48 shows the effect of C_F on the frequency response of the circuit. Adding a capacitance of 2 pF removes the peak, while a capacitance of 5 pF creates a much lower pole and reduces the bandwidth excessively.

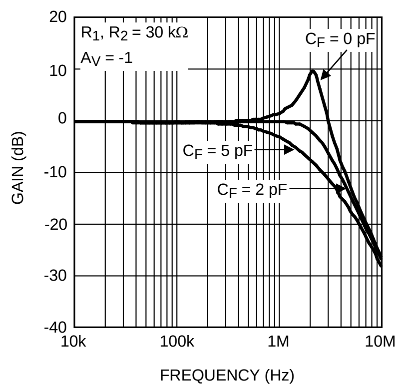


Figure 48. Gain Peaking Eliminated by C_F

AUDIO PREAMPLIFIER WITH BAND PASS FILTERING

With low input referred voltage noise, low supply voltage and current, and a low harmonic distortion, the LMV796 family is ideal for audio applications. Its wide unity gain bandwidth allows it to provide large gain for a wide range of frequencies and it can be used to design a preamplifier to drive a load of as low as 600Ω with less than 0.01% distortion. Two amplifier circuits are shown in Figure 49 and Figure 50. Figure 49 is an inverting amplifier, with a 10 kΩ feedback resistor, R_2, and a 1kΩ input resistor, R_1, and hence provides a gain of −10. Figure 50 is a non-inverting amplifier, using the same values of $R_1$and R_2, and provides a gain of 11. In either of these circuits, the coupling capacitor C_{C1} decides the lower frequency at which the circuit starts providing gain, while the feedback capacitor C_F decides the frequency at which the gain starts dropping off. Figure 51 shows the frequency response of the inverting amplifier with different values of C_F.

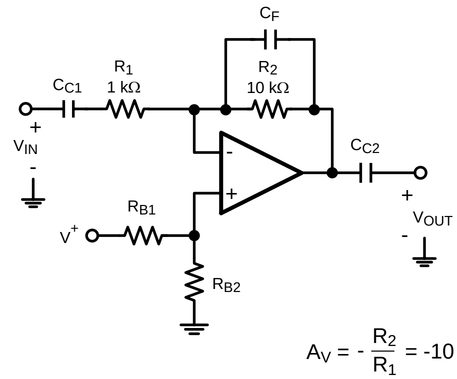


Figure 49. Inverting Audio Preamplifier

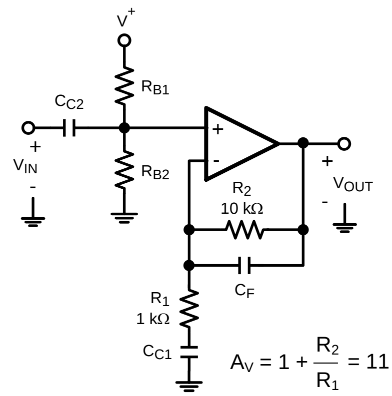


Figure 50. Non-inverting Audio Preamplifier

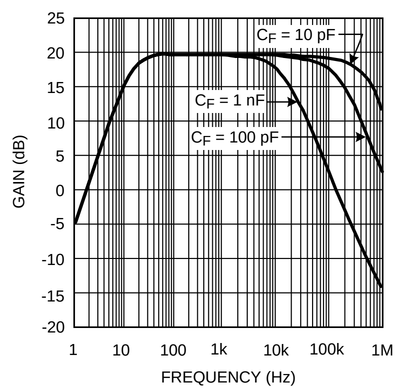


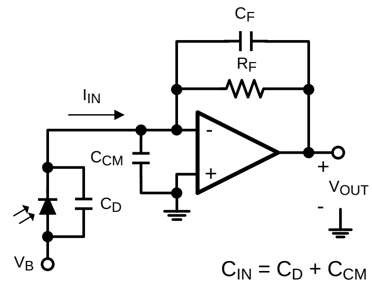
Figure 51. Frequency Response of the Inverting Audio Preamplifier

TRANSIMPEDANCE AMPLIFIER

CMOS input op amps are often used in transimpedance applications as they have an extremely high input impedance. A transimpedance amplifier converts a small input current into a voltage. This current is usually generated by a photodiode. The transimpedance gain, measured as the ratio of the output voltage to the input current, is expected to be large and wide-band. Since the circuit deals with currents in the range of a few nA, low noise performance is essential. The LMV796/LMV797 are CMOS input op amps providing wide bandwidth and low noise performance, and are hence ideal for transimpedance applications.

Usually, a transimpedance amplifier is designed on the basis of the current source driving the input. A photodiode is a very common capacitive current source, which requires transimpedance gain for transforming its miniscule current into easily detectable voltages. The photodiode and the amplifier's gain are selected with respect to the speed and accuracy required of the circuit. A faster circuit would require a photodiode with lesser capacitance and a faster amplifier. A more sensitive circuit would require a sensitive photodiode and a high gain. A typical transimpedance amplifier is shown in Figure 52. The output voltage of the amplifier is given by the equation $V_{OUT} = −I_{IN}R_F$. Since the output swing of the amplifier is limited, R_F should be selected such that all possible values of I_{IN} can be detected.

The LMV796/LMV797 have a large gain-bandwidth product (17 MHz), which enables high gains at wide bandwidths. A rail-to-rail output swing at 5.5V supply allows detection and amplification of a wide range of input currents. A CMOS input stage with negligible input current noise and low input voltage noise allows the LMV796/LMV797 to provide high fidelity amplification for wide bandwidths. These properties make the LMV796/LMV797 ideal for systems requiring wide-band transimpedance amplification.



$$C_{IN} = C_D + C_{CM}$$

$$\frac{V_{OUT}}{I_{IN}} = -R_F$$

Figure 52. Photodiode Transimpedance Amplifier

As mentioned earlier, the following parameters are used to design a transimpedance amplifier: the amplifier gain-bandwidth product, A_0; the amplifier input capacitance, C_{CM}; the photodiode capacitance, C_D; the transimpedance gain required, R_F; and the amplifier output swing. Once a feasible R_F is selected using the amplifier output swing, these numbers can be used to design an amplifier with the desired transimpedance gain and a maximally flat frequency response.

An essential component for obtaining a maximally flat response is the feedback capacitor, C_F. The capacitance seen at the input of the amplifier, C_{IN}, combined with the feedback capacitor, R_F, generate a phase lag which causes gain-peaking and can destabilize the circuit. C_{IN} is usually just the sum of C_D and C_{CM}. The feedback capacitor C_F creates a pole, f_P in the noise gain of the circuit, which neutralizes the zero in the noise gain, f_Z, created by the combination of R_F and C_{IN}. If properly positioned, the noise gain pole created by C_F can ensure that the slope of the gain remains at 20 dB/decade till the unity gain frequency of the amplifier is reached, thus ensuring stability. As shown in Figure 53, f_P is positioned such that it coincides with the point where the noise gain intersects the op amp's open loop gain. In this case, f_P is also the overall −3 dB frequency of the transimpedance amplifier. The value of C_F needed to make it so is given by Equation 3. A larger value of C_F causes excessive reduction of bandwidth, while a smaller value fails to prevent gain peaking and instability.

$$C_F = \frac{1 + \sqrt{1 + 4\pi R_F C_{IN} A_0}}{2\pi R_F A_0} \tag{3}$$

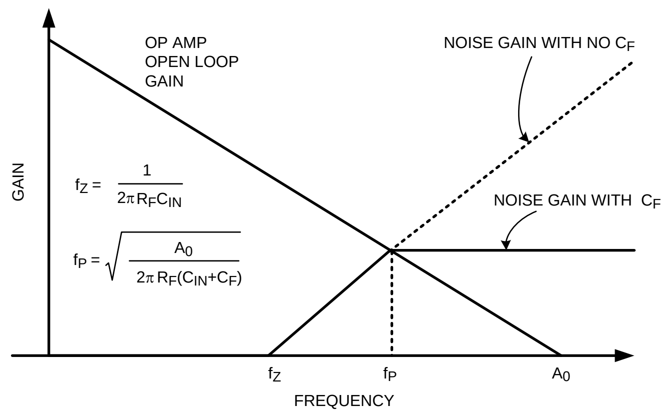
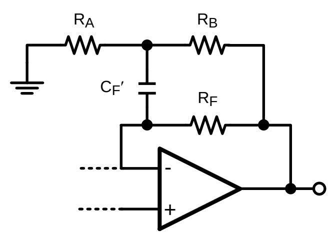


Figure 53. C_F Selection for Stability

Calculating C_F from Equation 3 can sometimes return unreasonably small values (<1 pF), especially for high speed applications. In these cases, it is often more practical to use the circuit shown in Figure 54 in order to allow more reasonable values. In this circuit, the capacitance C_F' is (1+ R_B/R_A) times the effective feedback capacitance, C_F. A larger capacitor can now be used in this circuit to obtain a smaller effective capacitance.

For example, if a C_F of 0.5 pF is needed, while only a 5 pF capacitor is available, R_B and R_A can be selected such that R_B/R_A = 9. This would convert a C_F' of 5 pF into a C_F of 0.5 pF. This relationship holds as long as R_A << R_F.



IF $R_A << R_F$

$$C_F' = \left(1 + \frac{R_B}{R_A}\right) C_F$$

Figure 54. Obtaining Small C_F from Large C_F'

LMV796 AS A TRANSIMPEDANCE AMPLIFIER

The LMV796 was used in the designs for a number of amplifiers with varying transimpedance gains and source capacitances. The gains, bandwidths and feedback capacitances of the circuits created are summarized in Table 1. The frequency responses are presented in Figure 55 and Figure 56. The feedback capacitances are slightly different from the formula in Equation 3, since the parasitic capacitance of the board and the feedback resistor R_F had to be accounted for.

Table 1.

Transimpedance, A_{TI}	C_{IN}	C_F	−3 dB Frequency
470000	50 pF	1.5 pF	350 kHz
470000	100 pF	2.0 pF	250 kHz
470000	200 pF	3.0 pF	150 kHz
47000	50 pF	4.5 pF	1.5 MHz
47000	100 pF	6.0 pF	1 MHz
47000	200 pF	9.0 pF	700 kHz

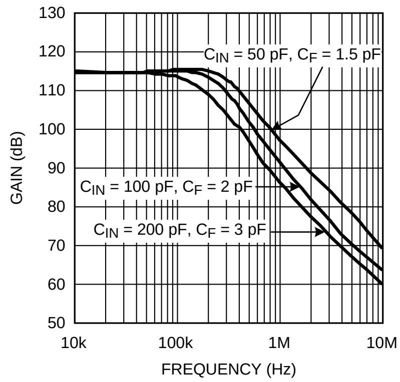


Figure 55. Frequency Response for A_{TI} = 470000

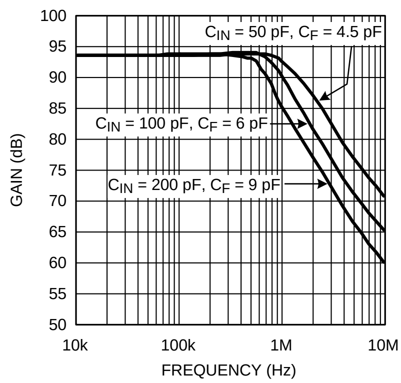
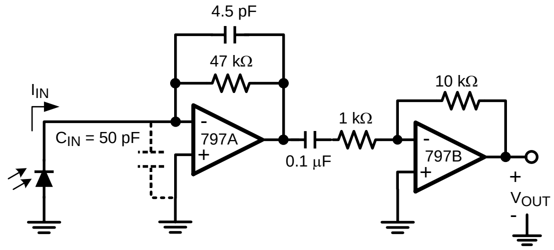


Figure 56. Frequency Response for A_{TI} = 47000

HIGH GAIN WIDEBAND TRANSIMPEDANCE AMPLIFIER USING THE LMV797

The LMV797 dual, low noise, wide bandwidth, CMOS input op amp IC can be used for compact, robust and integrated solutions for sensing and amplifying wide-band signals obtained from sensitive photodiodes. One of the two op amps available can be used to obtain transimpedance gain while the other can be used for amplifying the output voltage to further enhance the transimpedance gain. The wide bandwidth of the op amps (17 MHz) ensures that they are capable of providing high gain for a wide range of frequencies. The low input referred noise (5.8 nV/$\sqrt{Hz}$) allows the amplifier to deliver an output with a high SNR (signal to noise ratio). The small 8-pin VSSOP footprint saves space on printed circuit boards and allows ease of design in portable products.

The circuit shown in Figure 57, has the first op amp acting as a transimpedance amplifier with a gain of 47000, while the second stage provides a voltage gain of 10. This provides a total transimpedance gain of 470000 with a −3 dB bandwidth of about 1.5 MHz, for a total input capacitance of 50 pF. The frequency response for the circuit is shown in Figure 58



$$A_{TI} = \frac{V_{OUT}}{I_{IN}} = 470{,}000$$

Figure 57. 1.5 MHz Transimpedance Amplifier with A_{TI} = 470000

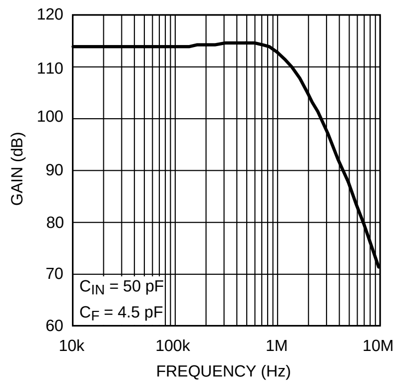
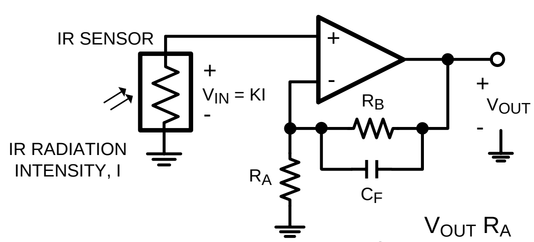


Figure 58. 1.5 MHz Transimpedance Amplifier Frequency Response

SENSOR INTERFACES

The low input bias current and low input referred noise of the LMV796 and LMV797 make them ideal for sensor interfaces. These circuits are required to sense voltages of the order of a few µV and currents amounting to less than a nA hence, the op amp needs to have low voltage noise and low input bias current. Typical applications include infra-red (IR) thermometry, thermocouple amplifiers and pH electrode buffers. Figure 59 is an example of a typical circuit used for measuring IR radiation intensity, often used for estimating the temperature of an object from a distance. The IR sensor generates a voltage proportional to I, which is the intensity of the IR radiation falling on it. As shown in Figure 59, K is the constant of proportionality relating the voltage across the IR sensor (V_{IN}) to the radiation intensity, I. The resistances R_A and R_B are selected to provide a high gain to amplify this voltage, while C_F is added to filter out the high frequency noise.



$$I = \frac{V_{OUT}\,R_A}{K(R_A + R_B)}$$

Figure 59. IR Radiation Sensor

REVISION HISTORY

Changes from Revision C (March 2013) to Revision C	Page

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV796MF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	AT3A
LMV796MFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	AT3A
LMV796QMF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AD7A
LMV796QMFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AD7A
LMV797MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AU3A
LMV797MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AU3A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV796, LMV796-Q1 :

- Catalog : LMV796

- Automotive : LMV796-Q1

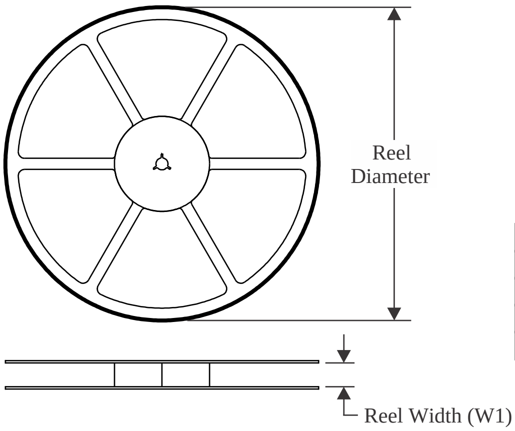
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

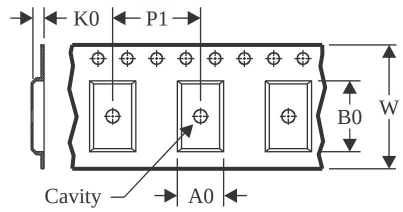
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

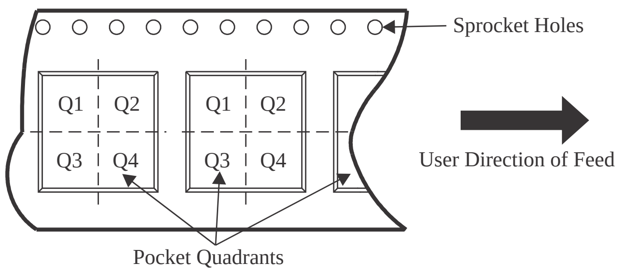


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

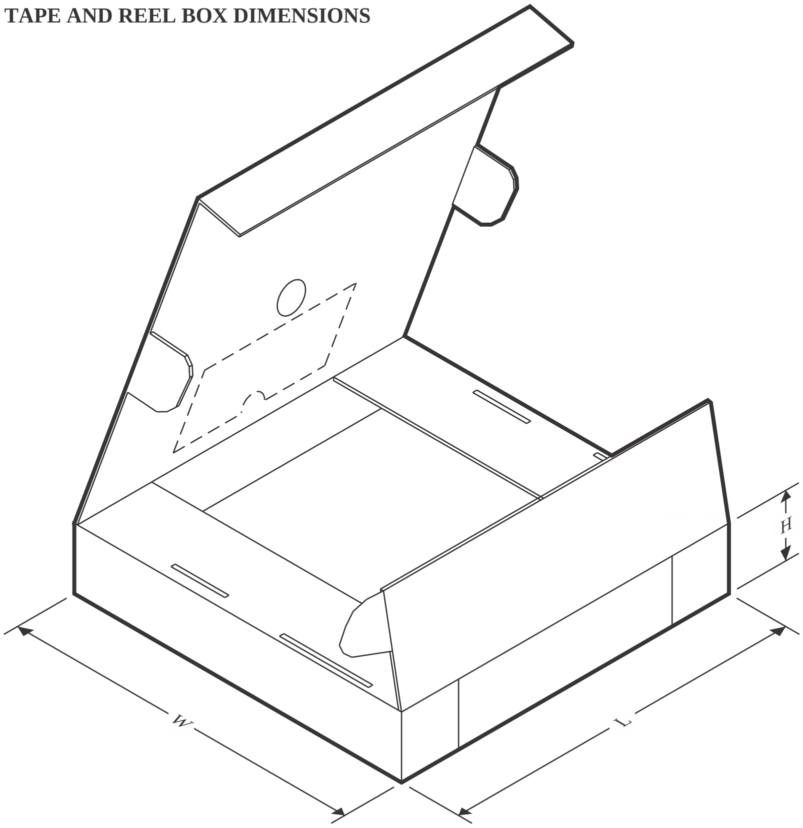
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

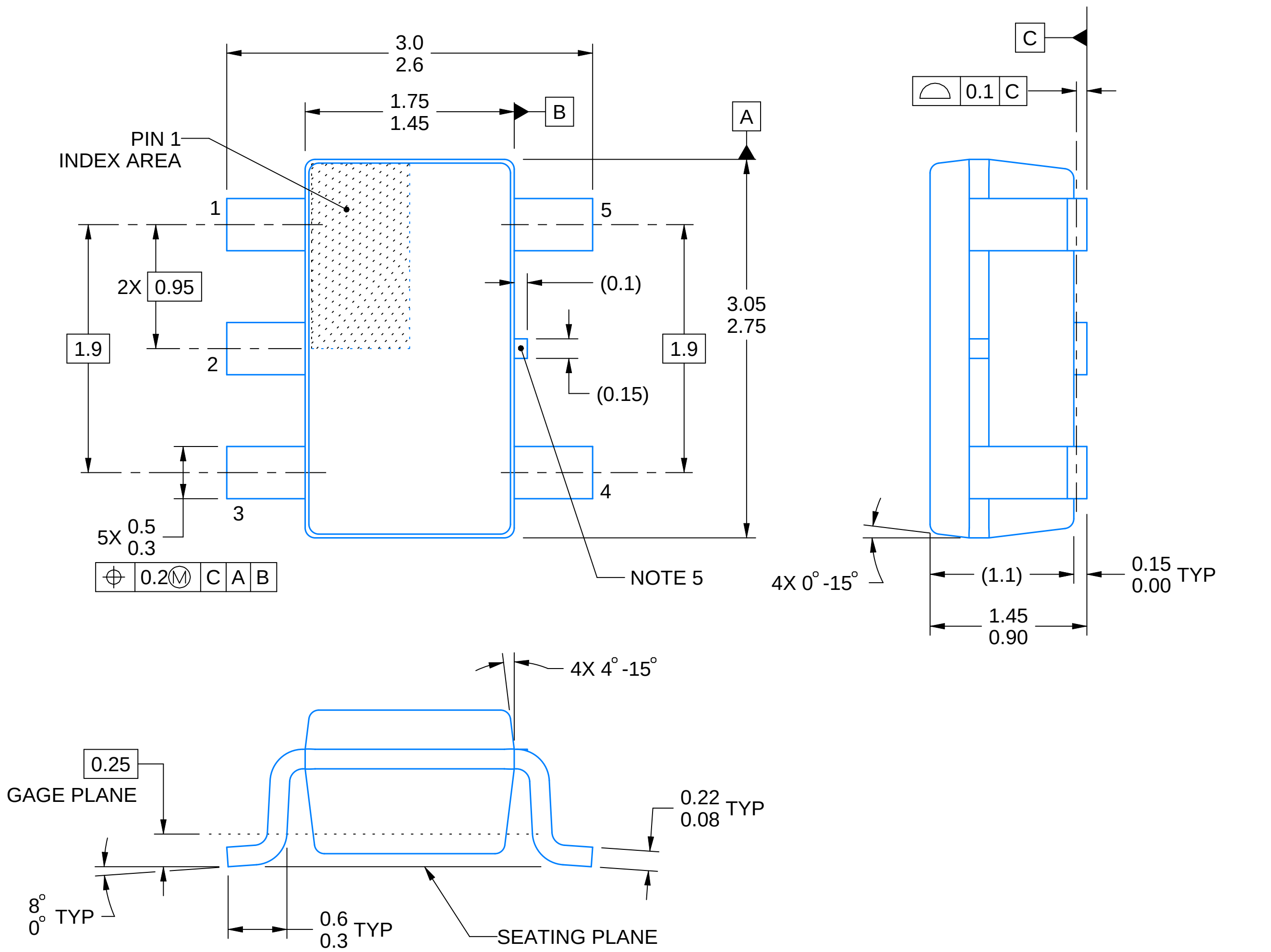
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV796MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV796MF/NOPB	SOT-23	DBV	5	1000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV796MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV796QMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV796QMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV797MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV797MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV796MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV796MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV796MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV796QMF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV796QMFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV797MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV797MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0



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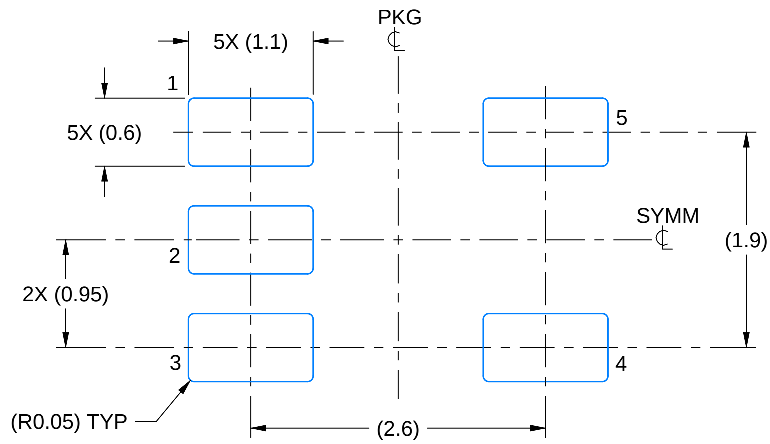
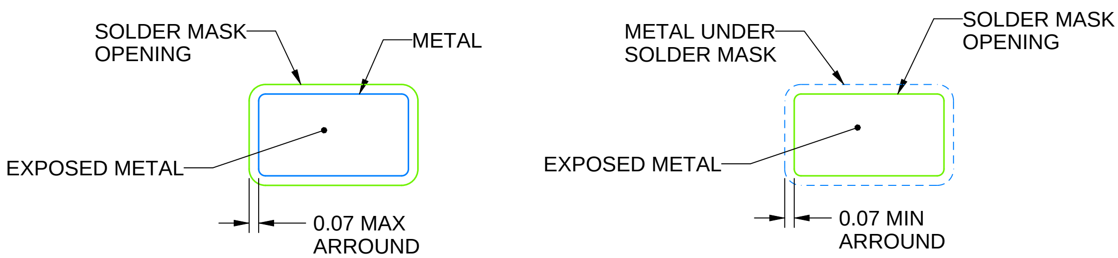
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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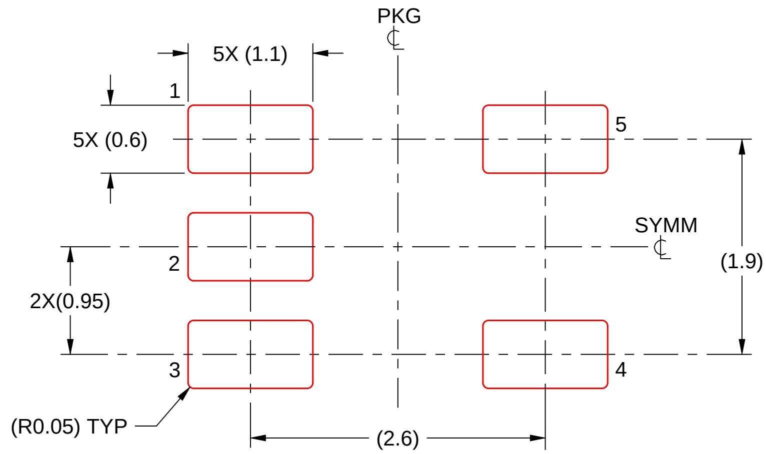
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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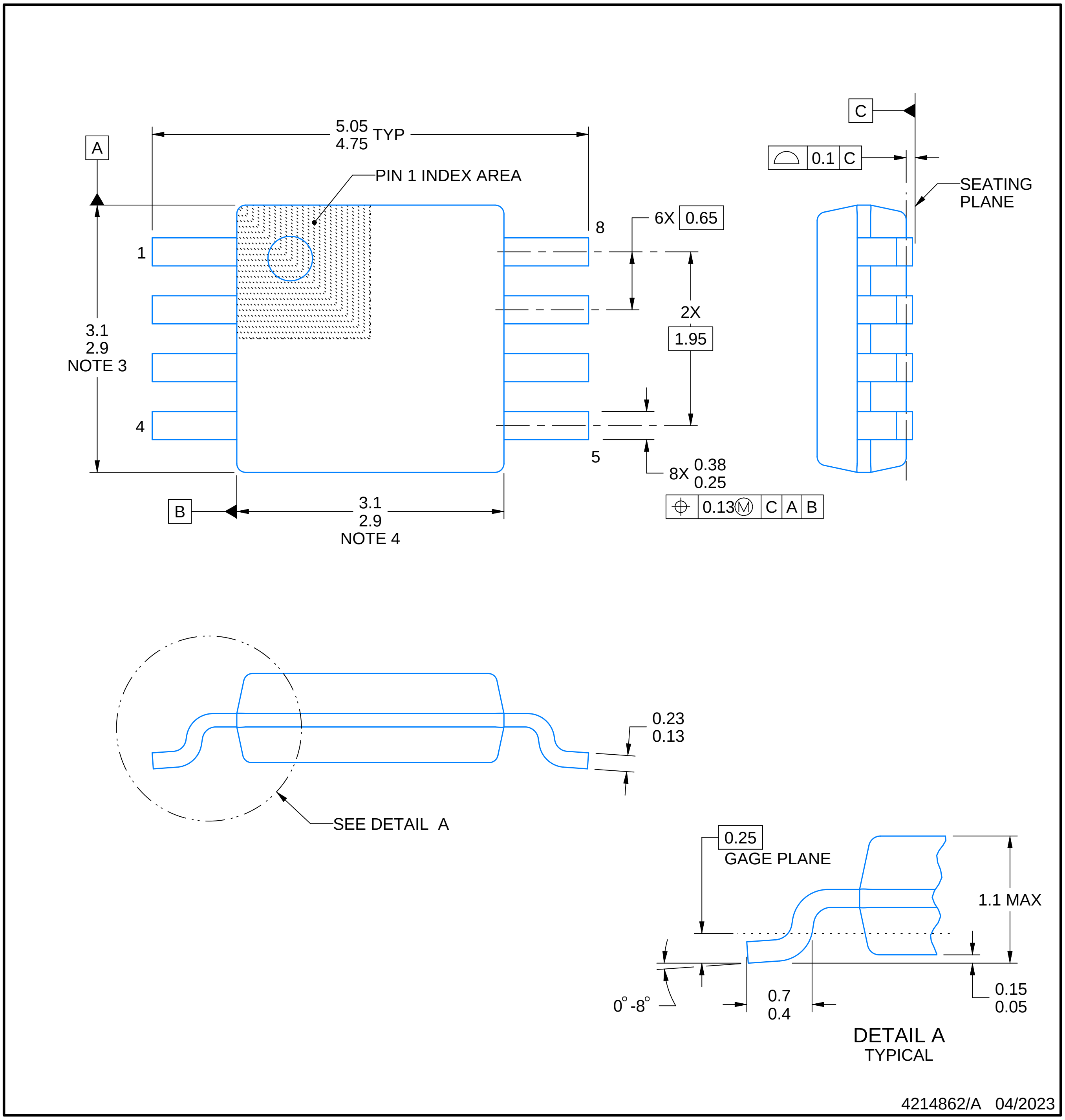
NOTES: (continued)

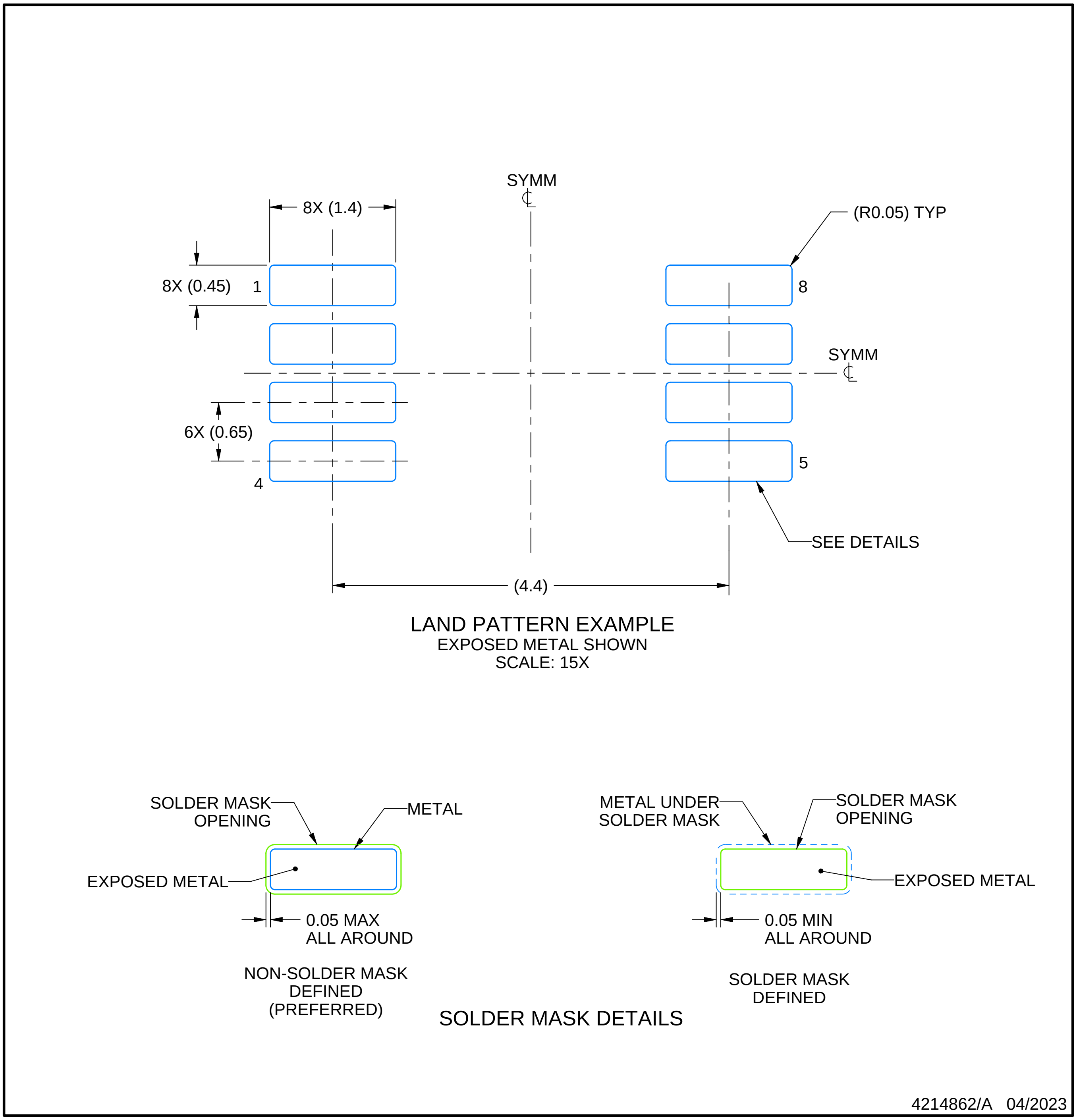
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PowerPAD is a trademark of Texas Instruments.

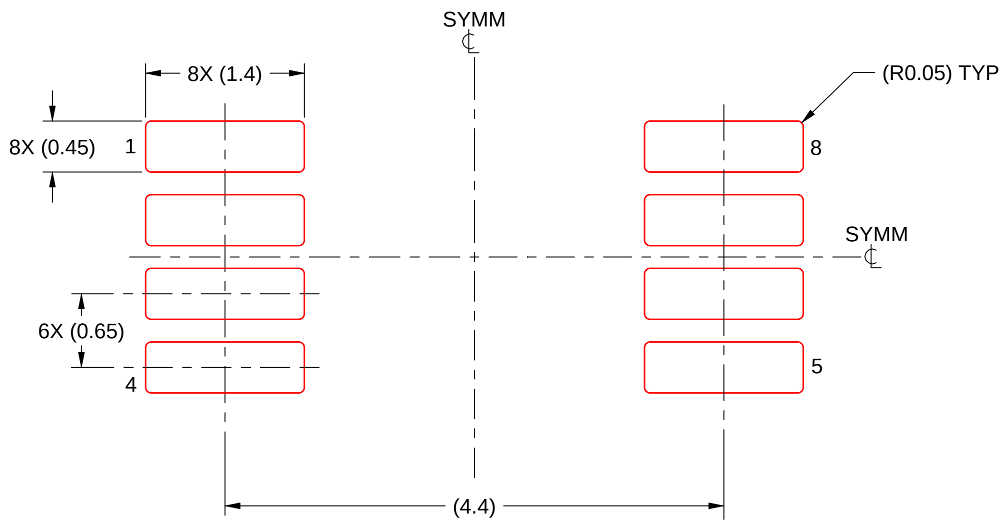
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.