CSD18512Q5B 40V N 通道 NexFET™ 功率 MOSFET

1 特性

- 低 $R_{DS(ON)}$
- 低热阻
- 雪崩级
- 逻辑电平
- 无铅端子镀层
- 符合 RoHS
- 无卤素
- SON 5mm x 6mm 塑料封装

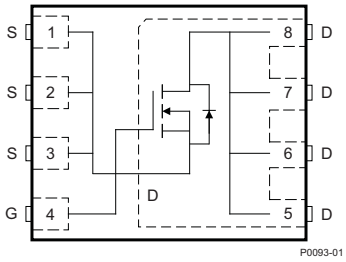
2 应用

- 直流/直流转换
- 次级侧同步整流器
- 电机控制

3 说明

这款 40V、1.3mΩ、5mm × 6mmNexFET™功率 MOSFET 旨在用于最大程度降低功率转换应用中的 损耗。

俯视图



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	40		V
Q_g	栅极电荷总量 (10V)	75		nC
Q_{gd}	栅漏栅极电荷	13.3		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	1.8	mΩ
		V_{GS} = 10V	1.3	mΩ
$V_{GS(th)}$	阈值电压	1.6		V

订购信息(1)

器件	数量	包装介质	封装	配送
CSD18512Q5B	2500	13 英寸卷带	SON 5mm × 6mm 塑料封装	卷带封装
CSD18512Q5BT	250	7 英寸卷带		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

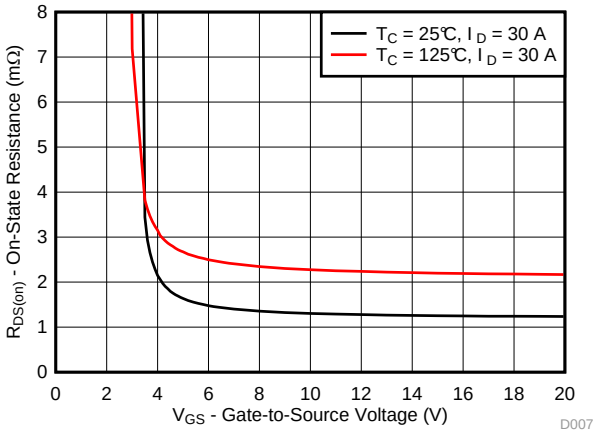
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	40	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	100	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	211	
	持续漏极电流(1)	32	
I_{DM}	脉冲漏极电流(2)	400	A
P_D	功耗(1)	3.1	W
	功耗，T_C = 25°C	139	
T_J、T_{stg}	工作结温、贮存温度	–55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 64A，L = 0.1mH，R_G = 25Ω	205	mJ

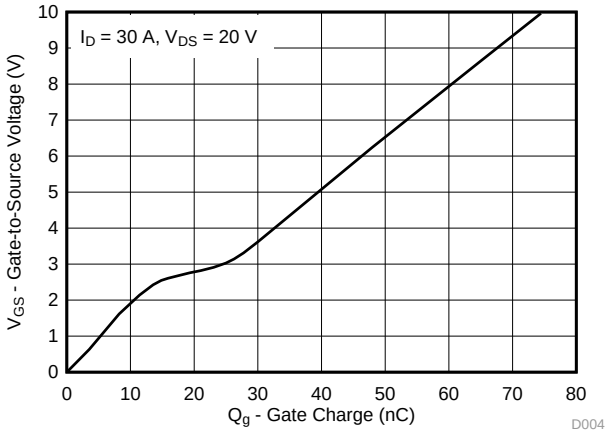
(1) $R_{\theta JA}$ = 40°C/W，这是在厚度为 0.06 英寸的环氧板 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2 2 盎司的铜焊盘上测得的典型值。

(2) 最大 $R_{\theta JC}$ = 0.9°C/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%

$R_{DS(on)}$ 与 V_{GS} 对比



栅极电荷



目录

4 修订历史记录

Changes from Original (December 2016) to Revision A	Page
• Corrected the SOA in Figure 10	5

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

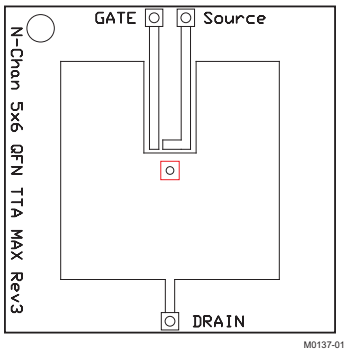
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain to source voltage	V_{GS} = 0 V, I_D = 250 μA	40			V
I_{DSS}	Drain to source leakage current	V_{GS} = 0 V, V_{DS} = 32 V			1	μA
I_{GSS}	Gate to source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate to source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.3	1.6	2.2	V
$R_{DS(on)}$	Drain to source on resistance	V_{GS} = 4.5 V, I_D = 30 A		1.8	2.3	mΩ
		V_{GS} = 10 V, I_D = 30 A		1.3	1.6	mΩ
g_{fs}	Transconductance	V_{DS} = 20 V, I_D = 30 A		136		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz		5480	7120	pF
C_{oss}	Output capacitance			537	699	pF
C_{rss}	Reverse transfer capacitance			256	333	pF
R_G	Series gate resistance			1.0	2.0	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 20 V, I_D = 30 A		37	48	nC
Q_g	Gate charge total (10 V)			75	98	nC
Q_{gd}	Gate charge gate to drain			13.3		nC
Q_{gs}	Gate charge gate to source			15.1		nC
$Q_{g(th)}$	Gate charge at V_{th}			8.2		nC
Q_{oss}	Output charge	V_{DS} = 20 V, V_{GS} = 0 V		23		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 20 V, V_{GS} = 10 V, I_{DS} = 30 A, R_G = 0 Ω		7		ns
t_r	Rise time			16		ns
$t_{d(off)}$	Turn off delay time			31		ns
t_f	Fall time			7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 30 A, V_{GS} = 0 V		0.75	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= 20 V, I_F = 30 A, di/dt = 300 A/μs		22		nC
t_{rr}	Reverse recovery time			17		ns

5.2 Thermal Information

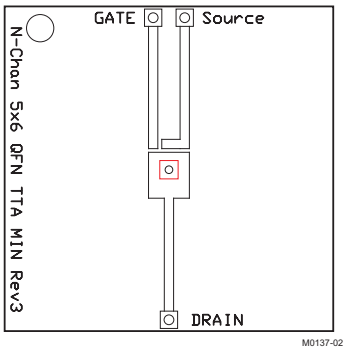
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case (top of package) thermal resistance (1)			0.9	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

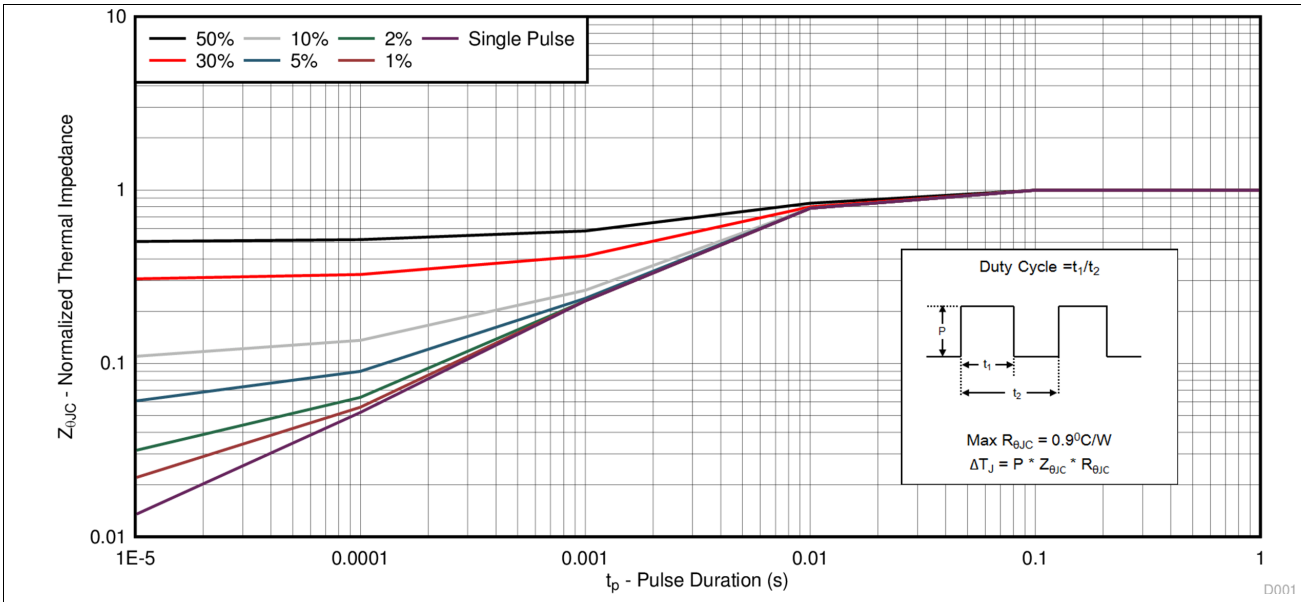


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

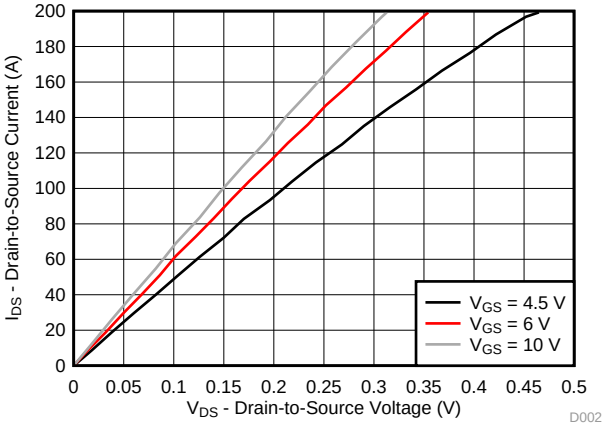


Figure 2. Saturation Characteristics

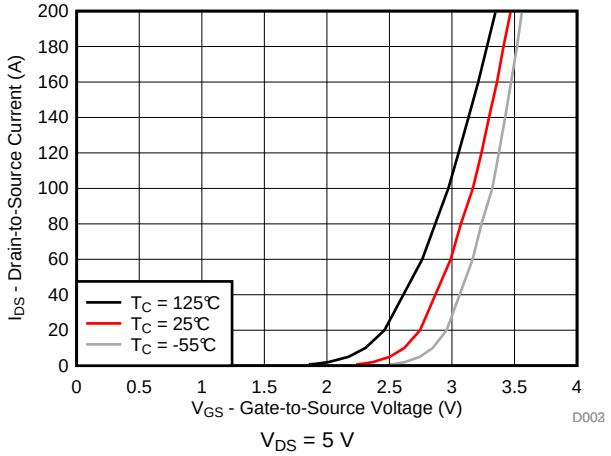


Figure 3. Transfer Characteristics

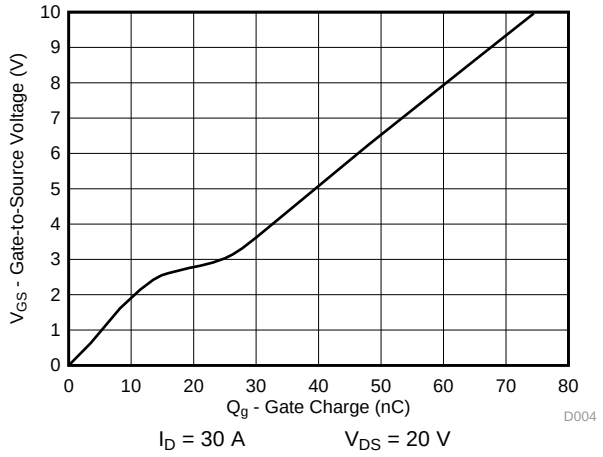


Figure 4. Gate Charge

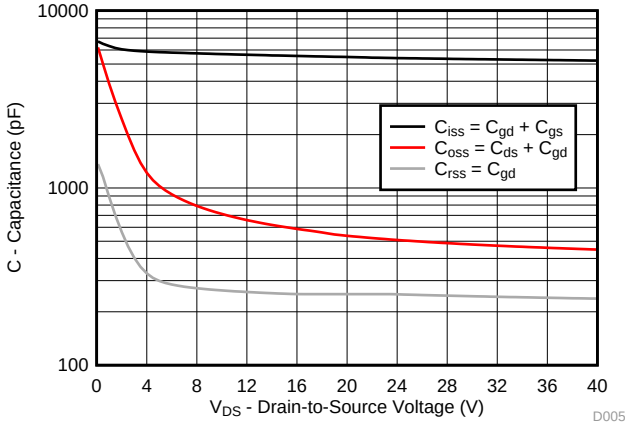


Figure 5. Capacitance

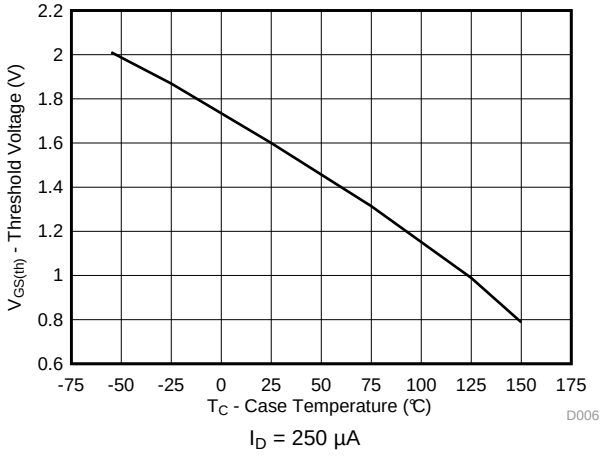


Figure 6. Threshold Voltage vs Temperature

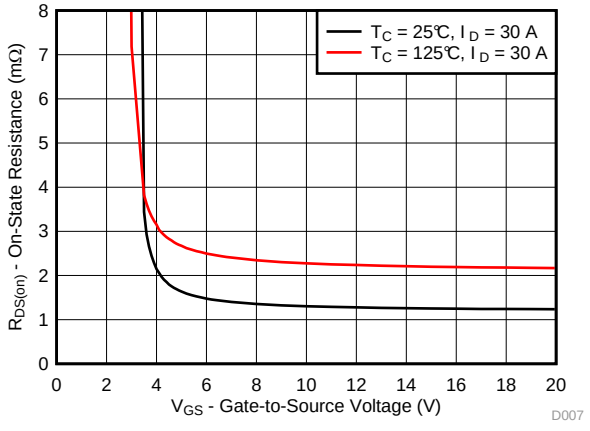


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

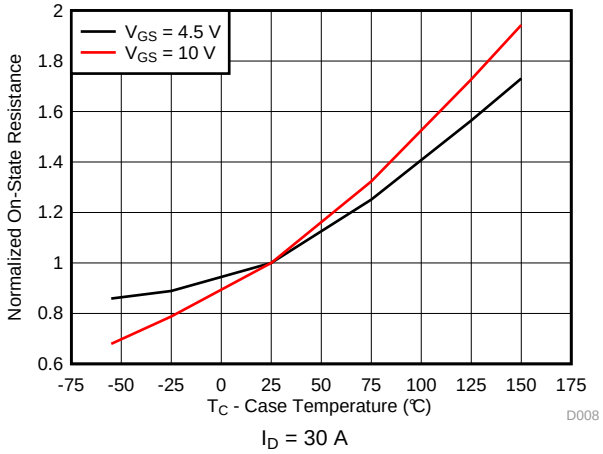


Figure 8. Normalized On-State Resistance vs Temperature

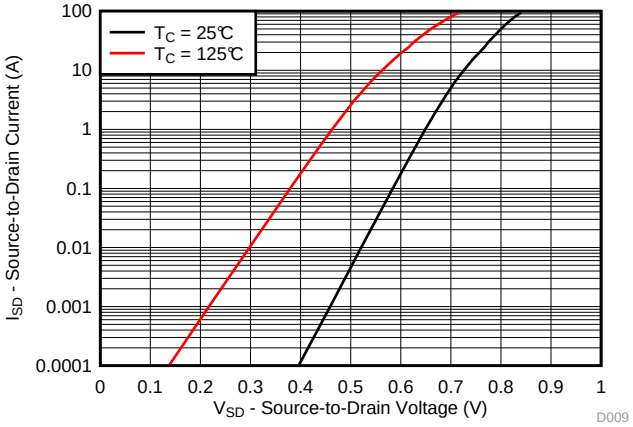


Figure 9. Typical Diode Forward Voltage

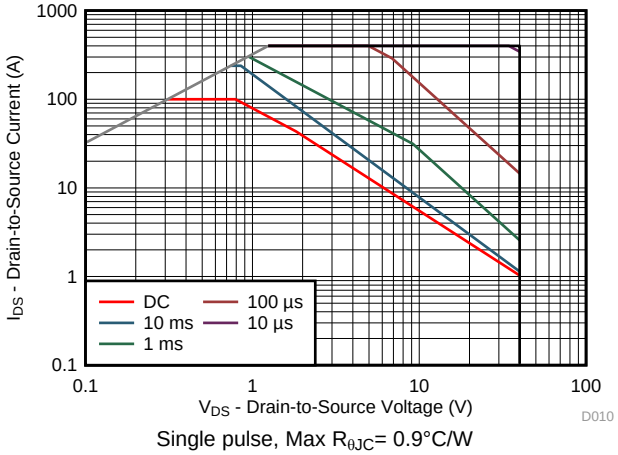


Figure 10. Maximum Safe Operating Area

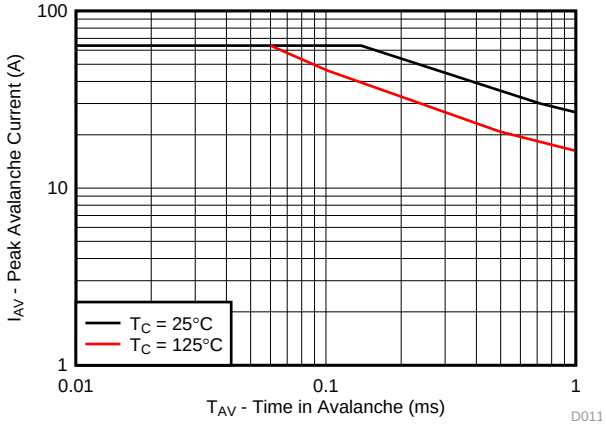


Figure 11. Single Pulse Unclamped Inductive Switching

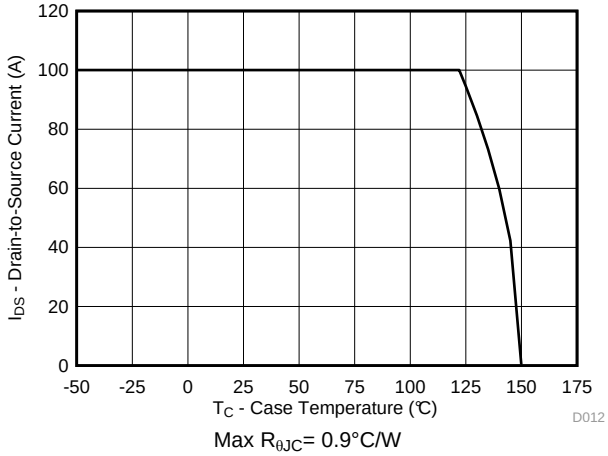


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 商标

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All other trademarks are the property of their respective owners.

6.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

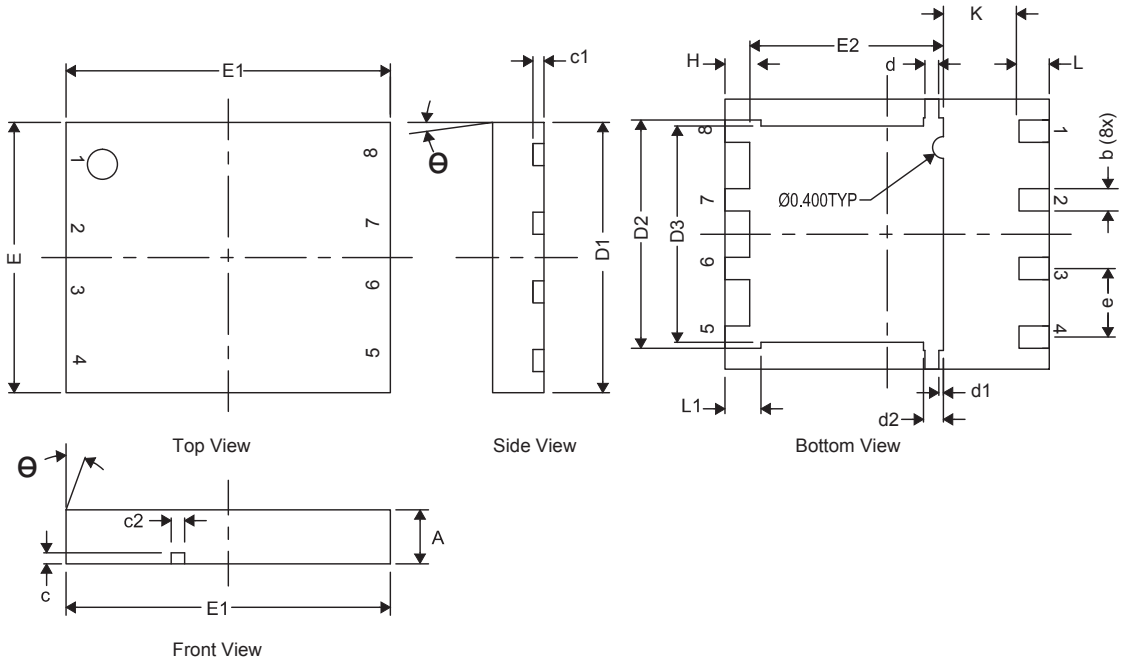
6.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

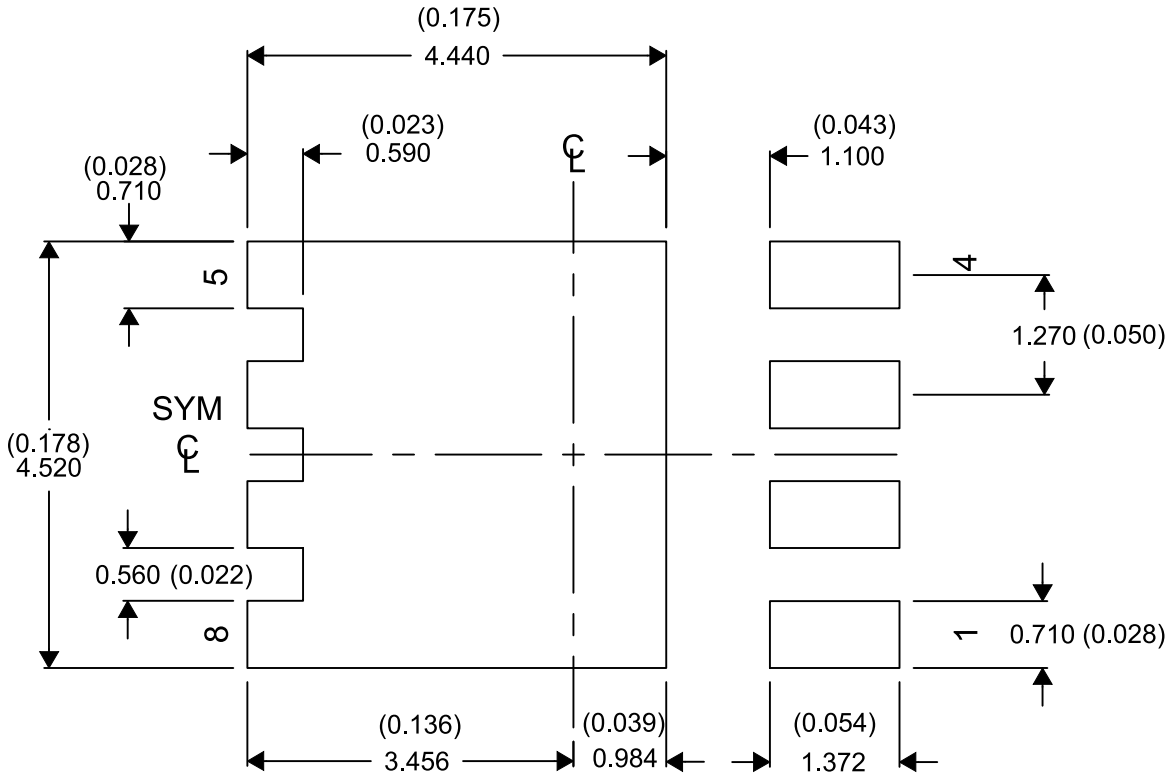
7 "机械、封装和可订购信息

7.1 Q5B 封装尺寸



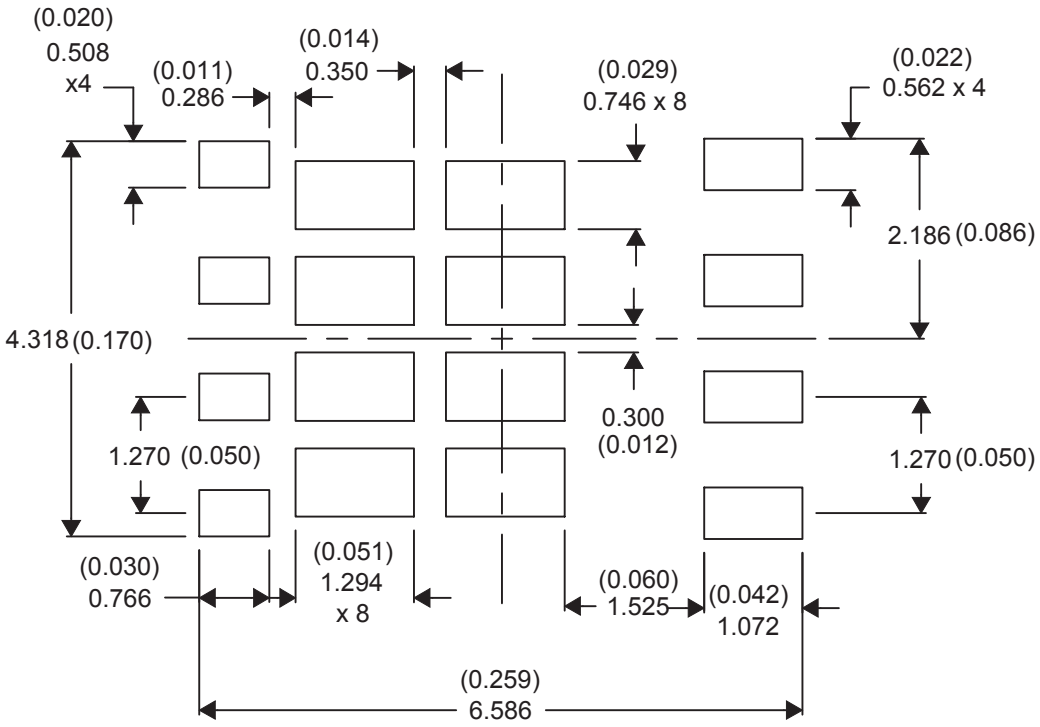
DIM	毫米		
	最小值	标称值	最大值
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 典型值		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 典型值		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	-	-
K	1.40 典型值		

7.2 建议 PCB 布局

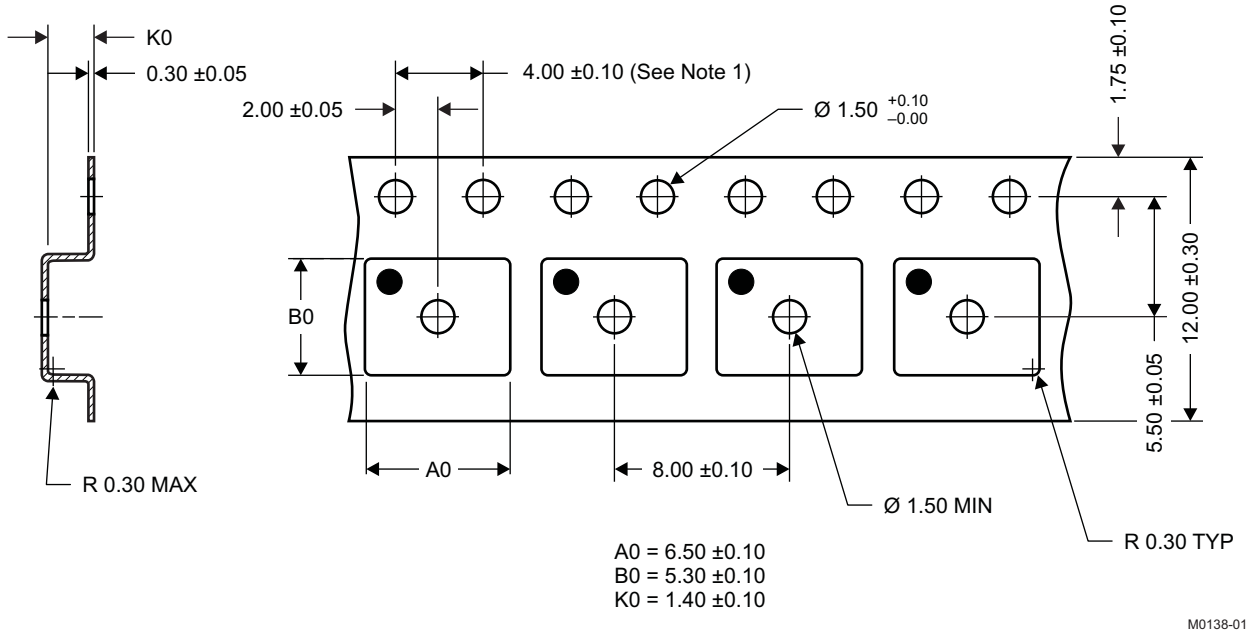


要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参阅《应用说明》SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

7.3 建议模板布局



7.4 Q5B 卷带信息



注释：

1. 10 个链齿孔的累积容差为 ±0.2。
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积。
3. 材料：黑色抗静电聚苯乙烯。
4. 全部尺寸为 mm（除非另外注明）。
5. 高于孔眼底部 0.3mm 的平面上测量得到 A0 和 B0 值.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD18512Q5B	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18512
CSD18512Q5BT	Active	Production	VSON-CLIP (DNK) | 8	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18512

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

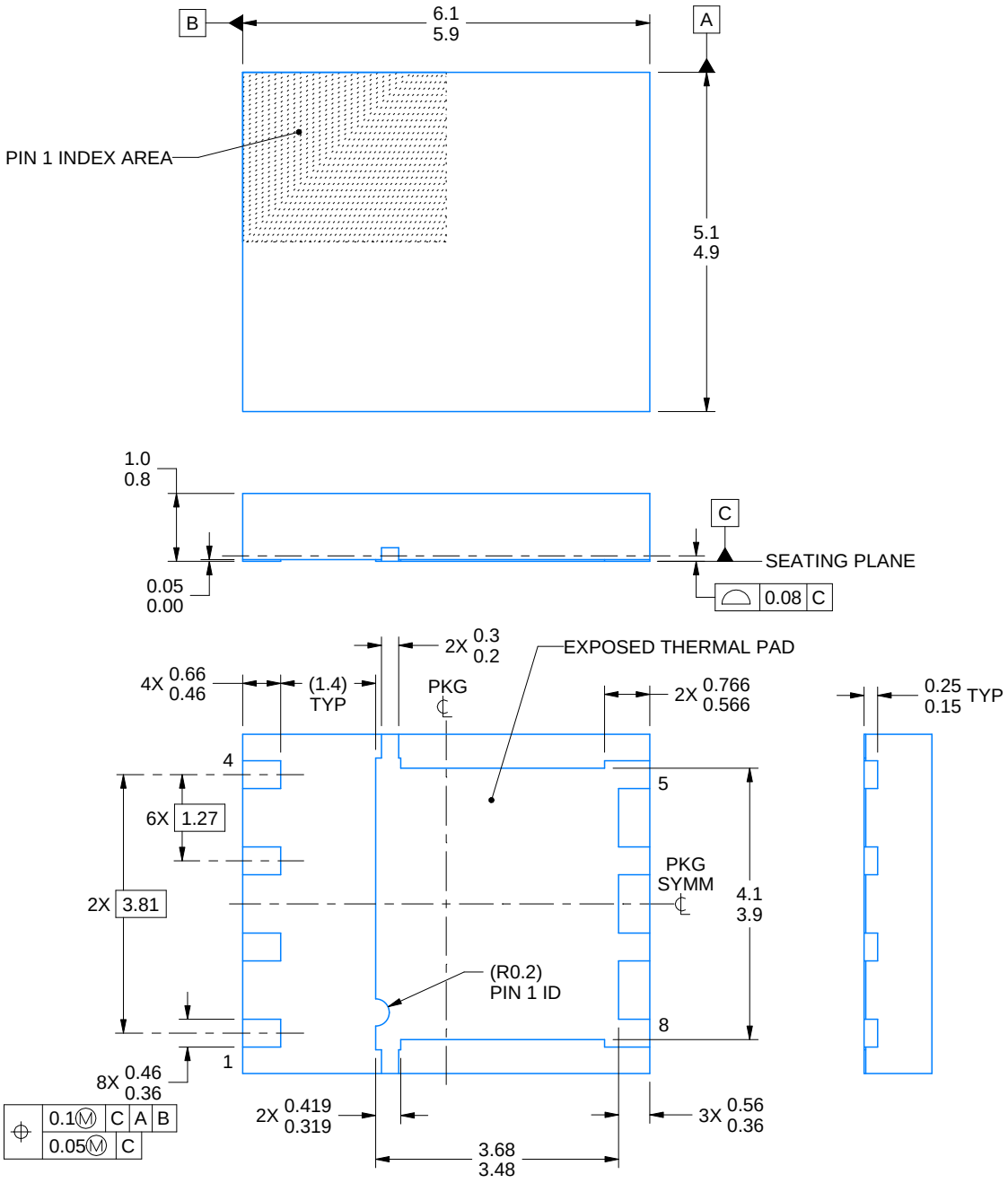
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DNK0008A

VSON-CLIP - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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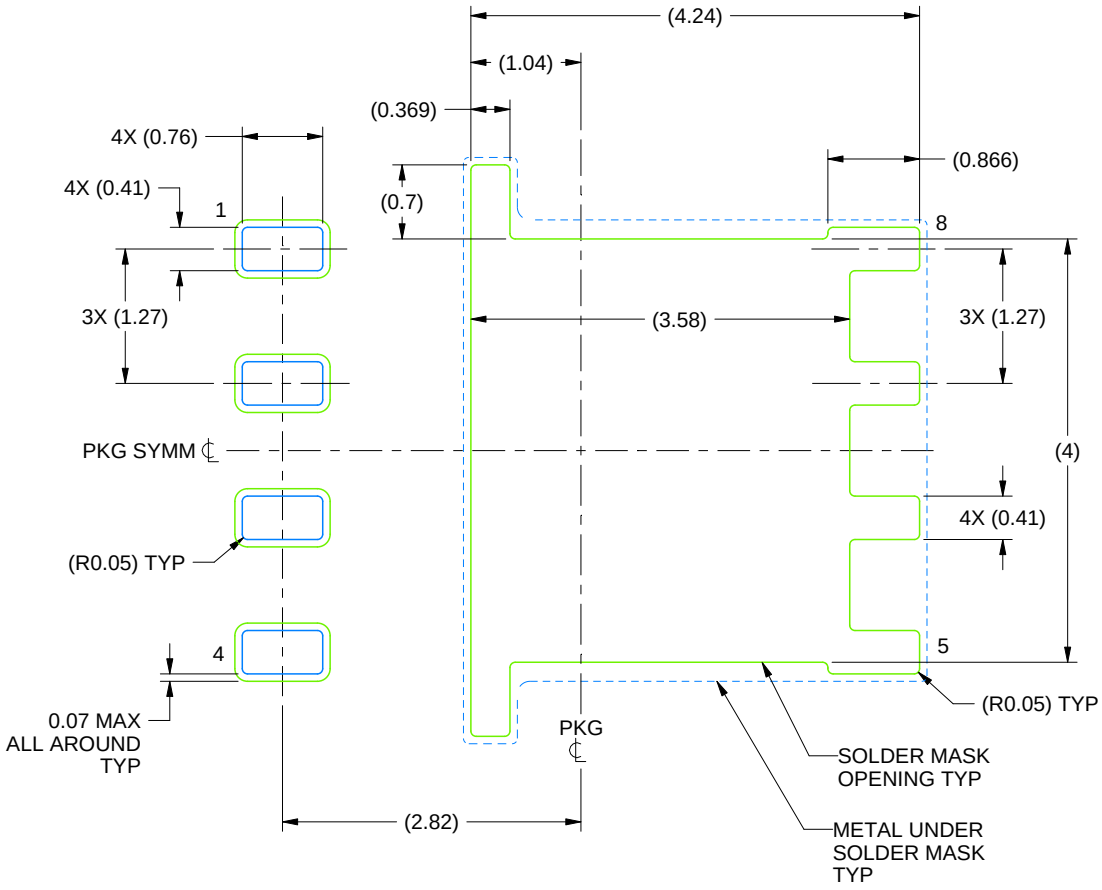
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 14X

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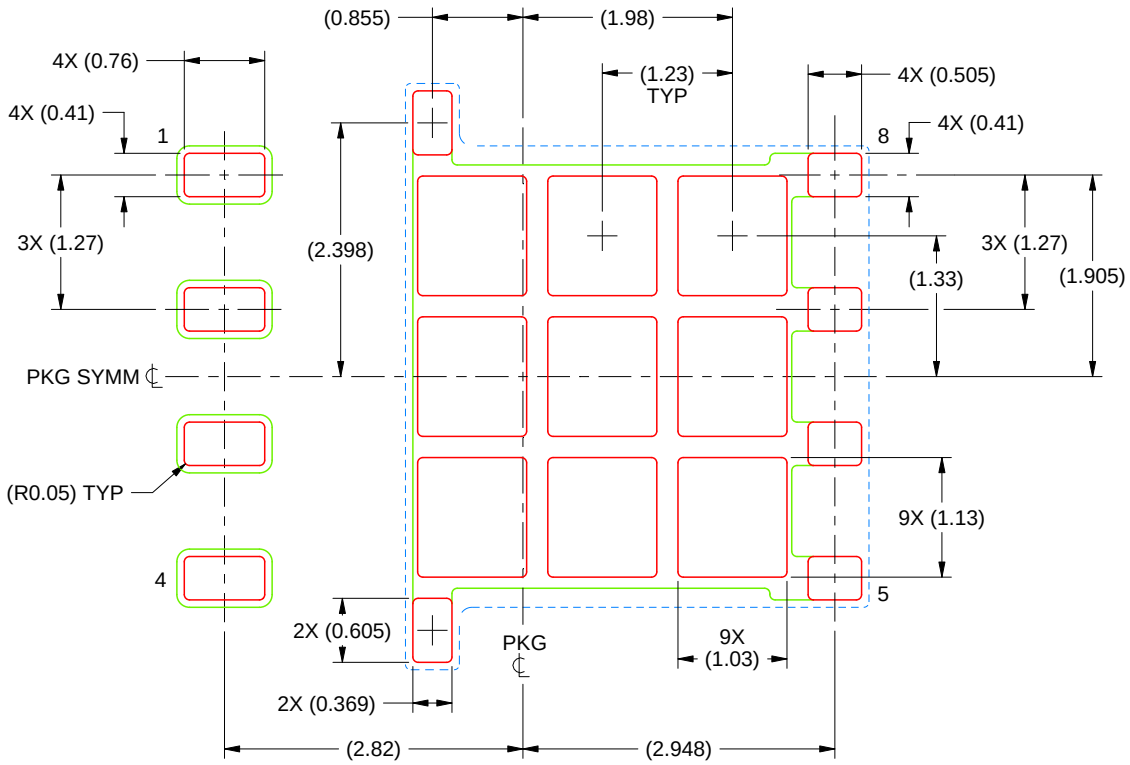
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 14X

74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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