

74LV05A

Hex inverter with open-drain outputs

Rev. 2 — 8 April 2024

Product data sheet

1. General description

The 74LV05A is a hex inverter with open-drain outputs. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

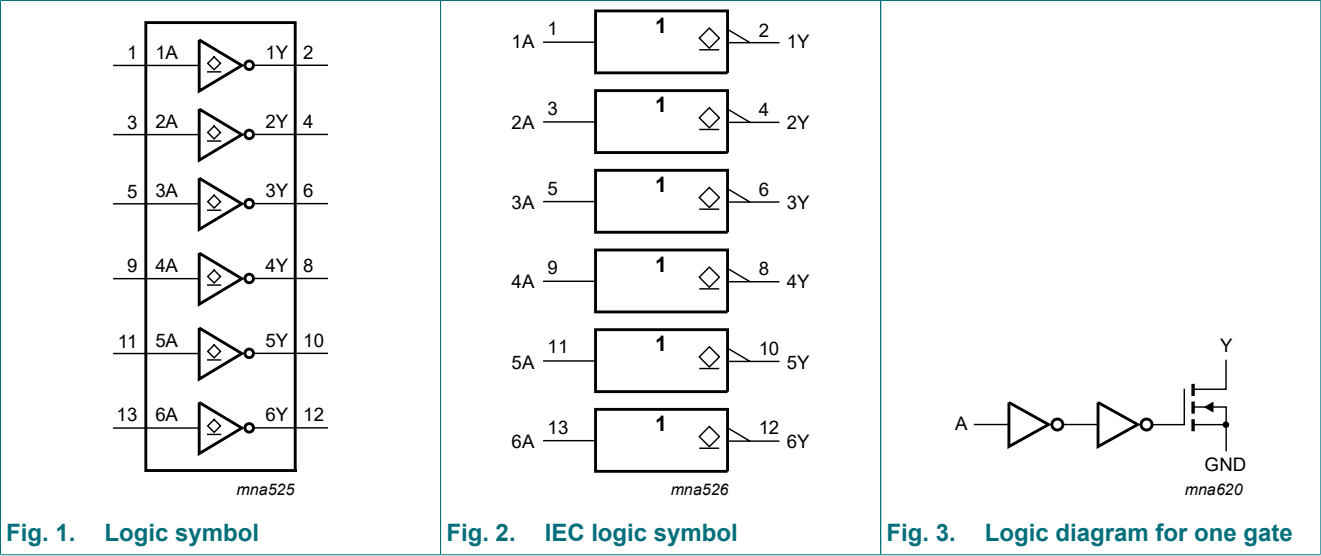
- Wide supply voltage range from 2.0 V to 5.5 V
- Typical $V_{OL(p)} < 0.8$ V at $V_{CC} = 3.3$ V, $T_{amb} = 25$ °C
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 3000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

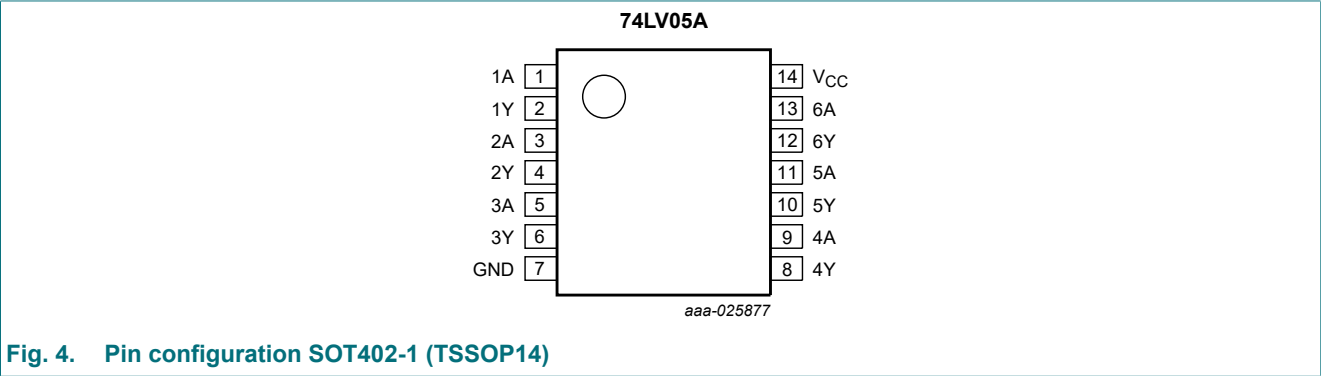
Type number	Package			
	Temperature range	Name	Description	Version
74LV05APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Input	Output
nA	nY
L	Z
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage	[1]	-0.5	+7.0	V
V _O	output voltage	output HIGH or LOW state [2][3]	-0.5	V _{CC} + 0.5	V
		output power-down [2]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-20	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±35	mA
I _{CC}	supply current		-	70	mA
I _{GND}	ground current		-70	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [4]	-	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] This value is limited to 7 V maximum.
[4] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.0	5.0	5.5	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	output LOW state, power-down or 3-state mode	0	-	5.5	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 2.7 V	-	-	200	ns/V
		V _{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V _{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 2.3 V to 2.7 V	0.7V _{CC}	-	-	0.7V _{CC}	-	0.7V _{CC}	-	V
		V _{CC} = 3.0 V to 3.6 V	0.7V _{CC}	-	-	0.7V _{CC}	-	0.7V _{CC}	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	0.7V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.3V _{CC}	-	0.3V _{CC}	-	0.3V _{CC}	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.3V _{CC}	-	0.3V _{CC}	-	0.3V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	-	0.3V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		V _{CC} = 2.0 V to 5.5 V; I _O = 50 µA	-	-	0.1	-	0.1	-	0.1	V
		V _{CC} = 2.3 V; I _O = 2 mA	-	-	0.4	-	0.4	-	0.4	V
		V _{CC} = 3.0 V; I _O = 6 mA	-	-	0.44	-	0.44	-	0.44	V
		V _{CC} = 4.5 V; I _O = 12 mA	-	-	0.55	-	0.55	-	0.55	V
I _{OZ}	OFF-state output current	V _{CC} = 5.5 V; V _I = V _{IH} or V _{IL} ; V _O = GND to 5.5 V	-	-	±0.25	-	±2.5	-	±2.5	µA
I _{OFF}	power-off leakage current	V _I or V _O = GND to 5.5 V; V _{CC} = 0 V	-	-	0.5	-	5	-	5	µA
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 0 V to 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2	-	20	-	20	µA

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. For test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t _{PZL}	OFF-state to LOW propagation delay	nA to nY; see Fig. 5								
		V _{CC} = 2.3 V to 2.7 V								
		C _L = 15 pF	-	5.5	12.2	1	15	1	16.5	ns
		C _L = 50 pF	-	7.8	16.6	1	19.5	1	21	ns
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.2	7.1	1	8.5	1	9.5	ns
		C _L = 50 pF	-	6.2	10.6	1	12	1	13	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.3	5.5	1	6.5	1	7.5	ns
		C _L = 50 pF	-	5.0	7.5	1	8.5	1	9.5	ns

Hex inverter with open-drain outputs

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t _{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Fig. 5								
		V _{CC} = 2.3 V to 2.7 V								
		C _L = 15 pF	-	5.1	10.4	1	13	1	13.5	ns
		C _L = 50 pF	-	9.7	15.2	1	18	1	18.5	ns
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.0	7.1	1	8.5	1	9	ns
		C _L = 50 pF	-	7.4	10.6	1	12	1	12.5	ns
		V _{CC} = 4.5 V to 5.5 V								
C _I	input capacitance	V _I = V _{CC} or GND; V _{CC} = 3.3 V	-	2	6	-	6	-	6	pF
C _O	output capacitance	V _O = V _{CC} or GND; V _{CC} = 3.3 V	-	4.5	-	-	-	-	-	pF
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} ; [2] C _L = 50 pF; f = 10 MHz								
		V _{CC} = 3.3 V	-	2.2	-	-	-	-	-	pF
		V _{CC} = 5.0 V	-	2.7	-	-	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 2.5 V, 3.3 V, and 5 V respectively, unless otherwise specified.

[2] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

Table 8. Noise characteristics

GND = 0 V. For test circuit see Figure 6.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ	Max	
V _{CC} = 3.3 V; C _L = 50 pF						
V _{OL(p)}	LOW-level output voltage (peak)		-	0.2	0.8	V
V _{OL(v)}	LOW-level output voltage (valley)		-0.8	-0.1	-	V
V _{IH(AC)}	AC HIGH-level input voltage (dynamic)		2.31	-	-	V
V _{IL(AC)}	AC LOW-level input voltage (dynamic)		-	-	0.99	V

10.1. Waveforms and test circuit

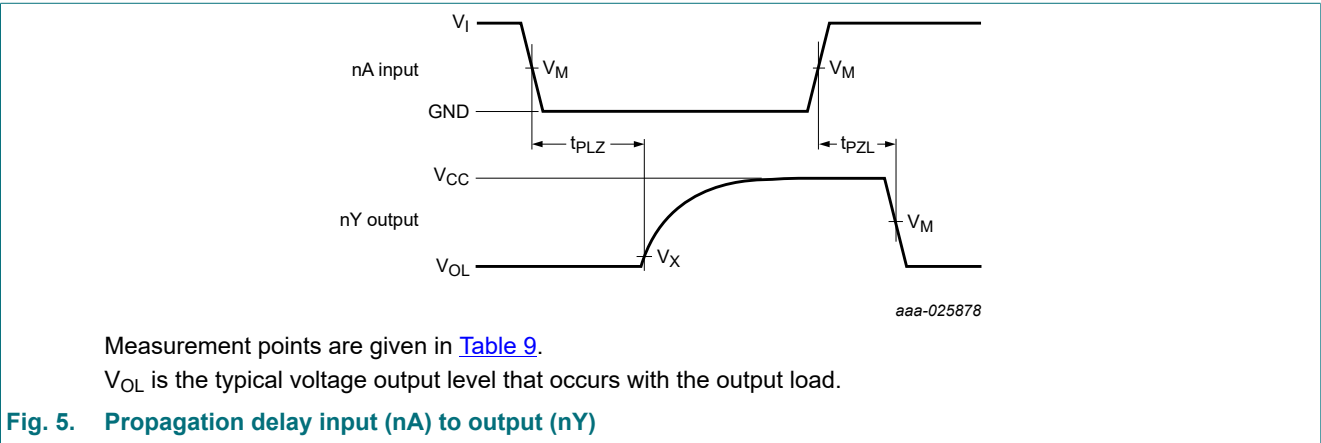


Table 9. Measurement points

Input	Output	
V_M	V_M	V_X
$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3\text{ V}$

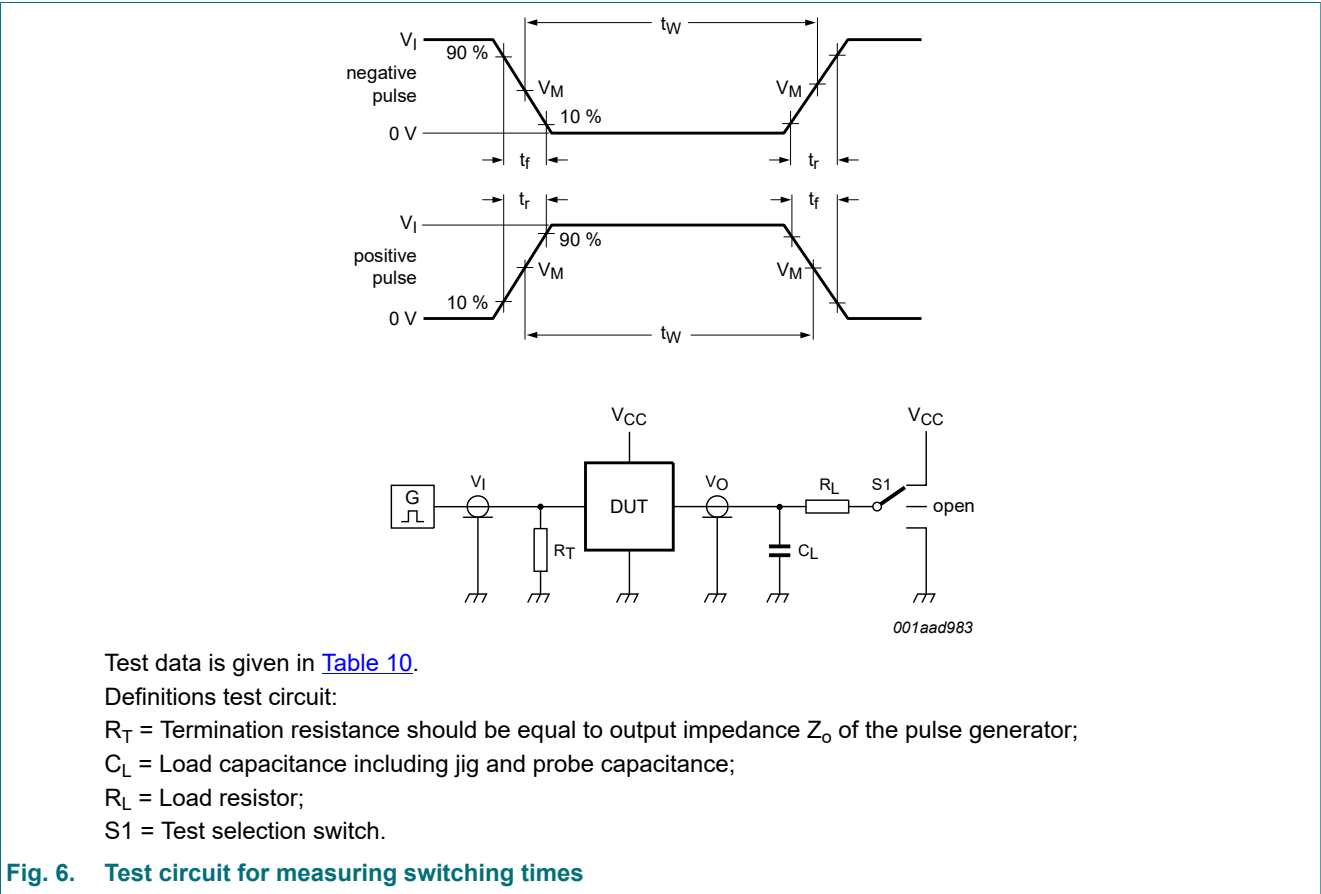


Table 10. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PLZ}, t_{PZL}
GND to V_{CC}	3.0 ns	15 pF, 50 pF	1 kΩ	V_{CC}

11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

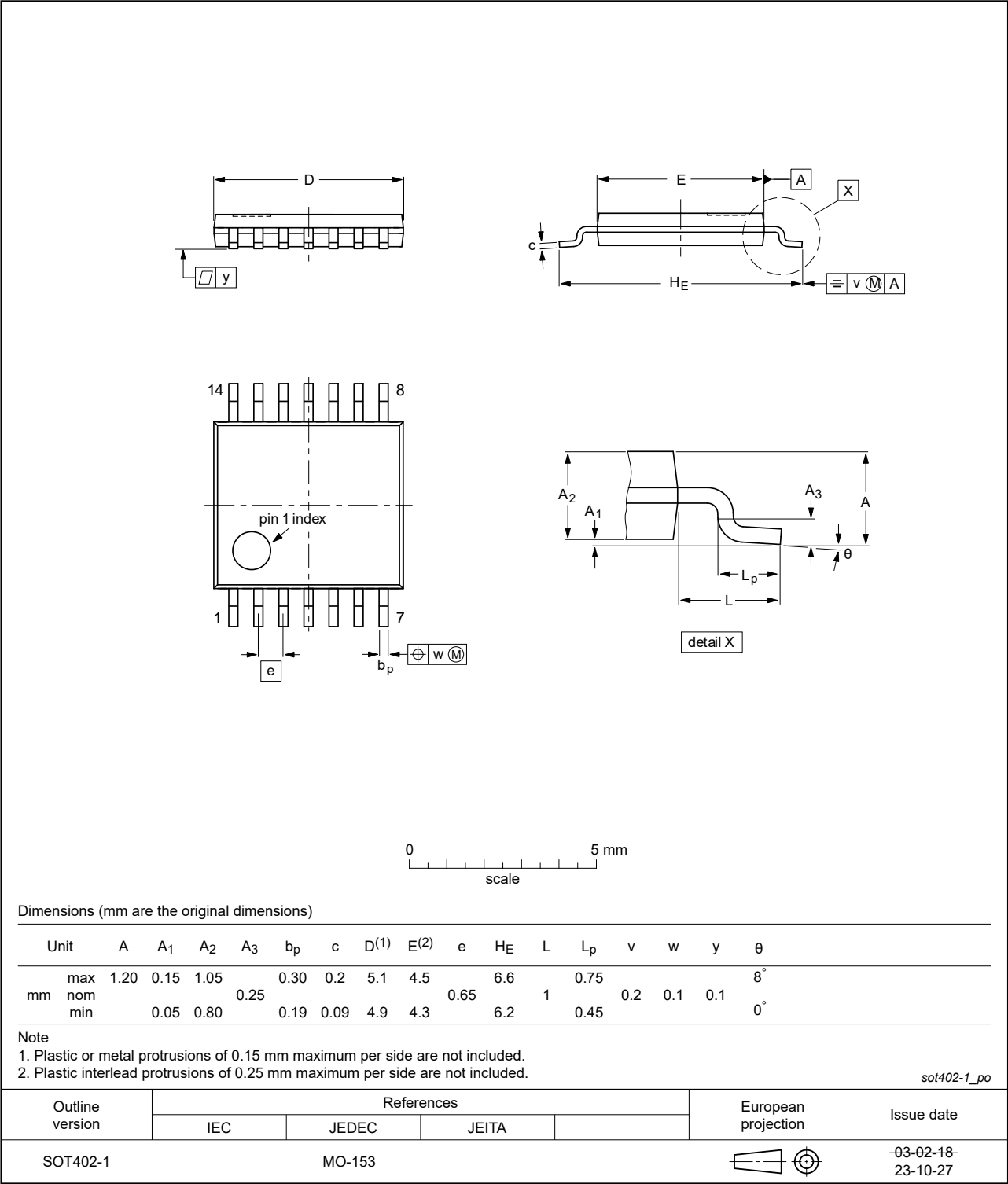


Fig. 7. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV05A v.2	20240408	Product data sheet	-	74LV05A v.1
Modifications	<ul style="list-style-type: none">• Fig. 7: Aligned TSSOP package outline drawing to JEDEC MO-153.• Section 2: ESD specification updated according to the latest JEDEC standard.• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.• Legal texts have been adapted to the new company name where appropriate.• Table 4: Derating values for P_{tot} total power dissipation updated.			
74LV05A v.1	20161219	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Ordering information..... 1

4. Functional diagram..... 2

5. Pinning information..... 2

5.1. Pinning..... 2

5.2. Pin description..... 2

6. Functional description..... 3

7. Limiting values..... 3

8. Recommended operating conditions..... 3

9. Static characteristics..... 4

10. Dynamic characteristics..... 4

10.1. Waveforms and test circuit..... 6

11. Package outline..... 7

12. Abbreviations..... 8

13. Revision history..... 8

14. Legal information..... 9

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