TLV1117 可调和固定低压降稳压器

1 特性

- 输出电压选项：1.5V、1.8V、2.5V、3.3V、5V 和可调
- 输出电流：800mA
- 在多个电流水平指定压差电压
- 线性调整率最大值：0.2%
- 负载调整率最大值：0.4%
- 有关采用固定输出 SOT-223 封装配置的直接替代产品和改进功能，请参阅 TLV761

2 应用

- 电子销售终端
- 医疗、保健和健身应用
- 打印机
- 电器和白色家电
- 电视机顶盒

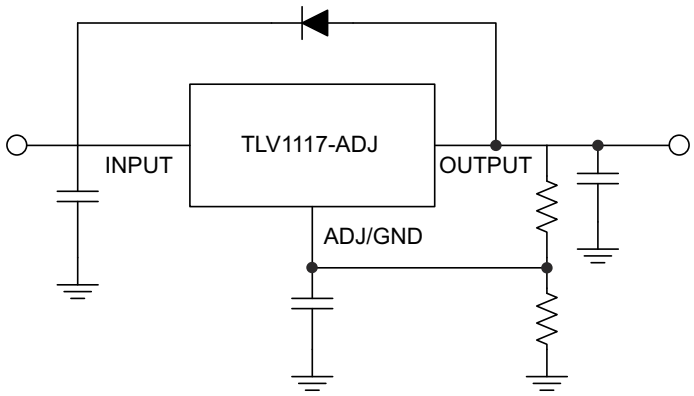
3 说明

TLV1117 是一款正低压降稳压器，可提供高达 800 mA 的输出电流。该器件具有 1.5V、1.8V、2.5V、3.3V、5V 和可调输出电压选项。所有内部电路均设计为可在低至 1V 输入/输出差压下运行。额定的最大压差电压为 1.3V（电流为 800mA），该值在较低的负载电流时会降低。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
TLV1117	DCY（SOT-223，4）	6.50mm × 3.50mm
	DRJ（WSON，8）	4.00mm × 4.00mm
	KVU（TO-252，3）	6.60mm × 6.10mm
	KCS（TO-220，3）	10.16mm × 8.70mm
	KCT（TO-220，3）	10.16mm × 8.59mm
	KTT（DDPAK/TO-263，3）	10.18mm × 8.41mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

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4 Revision History

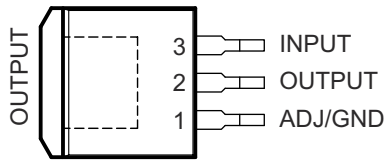
注：以前版本的页码可能与当前版本的页码不同

Changes from Revision L (October 2014) to Revision M (January 2023)	Page
• 向*特性* 部分添加了直接替代产品要点	1
• Changed *Handling Ratings* title to *ESD Ratings*	3
• Added *Application Information* section	11

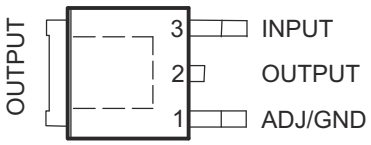
Changes from Revision K (April 2013) to Revision L (October 2014)	Page
• 将数据表更新为新的 TI 标准 - 无规格变化。	1
• 删除了“订购信息”表	1
• 删除了“订购信息”表	1
• 添加了“应用”	1
• Added Mechanical, Packaging, and Orderable Information section	14

5 Pin Configuration and Functions

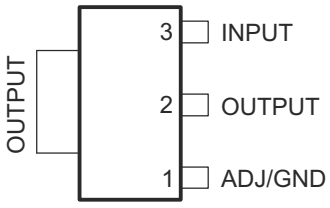
KTT (TO-263) PACKAGE
(TOP VIEW)



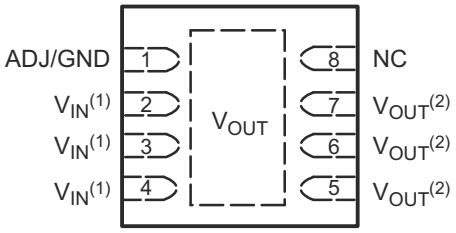
KVU (TO-252) PACKAGE
(TOP VIEW)



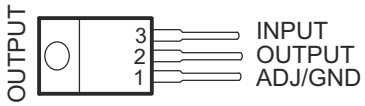
DCY (SOT-223) PACKAGE
(TOP VIEW)



DRJ (QFN) PACKAGE
(TOP VIEW)



KCT, KCS (TO-220) PACKAGE
(TOP VIEW)



(1) V_{IN} pins (2, 3, 4) must be connected together.
(2) V_{OUT} pins (5, 6, 7) must be connected together.

表 5-1. Pin Functions

PIN						TYPE	DESCRIPTION
NAME	KTT	KVU	DCY	DRJ	KCT		
ADJ/GND	1	1	1	1	1	I/O	Output voltage adjustment pin. Connect to a resistor divider.
INPUT	3	3	3	2, 3, 4	3	I	Voltage input
OUTPUT	2	2	2	5, 6, 7	2	O	Voltage output
NC	—	—	—	8	—	—	No connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Continuous input voltage		16	V
T_J	Operating virtual-junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN(1)	MAX	UNIT
V_{IN}	Input voltage	TLV1117	2.7	15	V
		TLV1117-15	2.9	15	
		TLV1117-18	3.2	15	
		TLV1117-25	3.9	15	
		TLV1117-33	4.7	15	
		TLV1117-50	6.4	15	
I_O	Output current			0.8	A
T_J	Operating virtual-junction temperature	TLV1117C	0	125	°C
		TLV1117I	–40	125	

(1) The input-to-output differential across the regulator should provide for some margin against regulator operation at the maximum dropout (for a particular current value). This margin is needed to account for tolerances in both the input voltage (lower limit) and the output voltage (upper limit). The absolute minimum V_{IN} for a desired maximum output current can be calculated by the following: $V_{IN(min)} = V_{OUT(max)} + V_{DO(max\ at\ rated\ current)}$

6.4 Thermal Information

THERMAL METRIC(1) (2) (3)		TLV1117							UNITS
		PowerFlex							
		KTE (3 PINS)	KTP (3 PINS)	DRJ (8 PINS)	DCY (4 PINS)	KVU (3 PINS)	KCS, KCT (3 PINS)	KTT (3 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.6	49.2	38.3	104.3	50.9	30.1	27.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.7	60.6	36.5	53.7	57.9	44.6	43.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.2	3.1	60.5	5.7	34.8	1.2	17.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.9	8.7	0.2	3.1	6	5	2.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.1	3	12	5.5	23.7	1.2	9.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3	3	4.7	n/a	0.4	0.4	0.3	°C/W
$R_{\theta JP}$	Thermal resistance between the die junction and the bottom of the exposed pad.	2.7	1.4	1.78	n/a	n/a	3	1.94	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

6.5 TLV1117C Electrical Characteristics

T_J = 0°C to 125°C, all typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
Reference voltage, V_{REF}	V_{IN} – V_{OUT} = 2 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117	1.238	1.25	1.262	V
	V_{IN} – V_{OUT} = 1.4 V to 10 V, I_{OUT} = 10 mA to 800 mA		1.225	1.25	1.27	
Output voltage, V_{OUT}	V_{IN} = 3.5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-15	1.485	1.5	1.515	
	V_{IN} = 2.9 V to 10 V, I_{OUT} = 0 mA to 800 mA		1.455	1.5	1.545	
	V_{IN} = 3.8 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-18	1.782	1.8	1.818	
	V_{IN} = 3.2 V to 10 V, I_{OUT} = 0 mA to 800 mA		1.746	1.8	1.854	
	V_{IN} = 4.5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-25	2.475	2.5	2.525	
	V_{IN} = 3.9 V to 10 V, I_{OUT} = 0 mA to 800 mA		2.450	2.5	2.550	
	V_{IN} = 5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-33	3.267	3.3	3.333	
	V_{IN} = 4.75 V to 10 V, I_{OUT} = 0 mA to 800 mA		3.235	3.3	3.365	
	V_{IN} = 7 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-50	4.950	5.0	5.050	
	V_{IN} = 6.5 V to 12 V, I_{OUT} = 0 mA to 800 mA		4.900	5.0	5.100	
Line regulation	I_{OUT} = 10 mA, V_{IN} – V_{OUT} = 1.5 V to 13.75 V	TLV1117		0.035%	0.2%	—
	I_{OUT} = 0 mA, V_{IN} = 2.9 V to 10 V	TLV1117-15		1	6	mV
	I_{OUT} = 0 mA, V_{IN} = 3.2 V to 10 V	TLV1117-18		1	6	
	I_{OUT} = 0 mA, V_{IN} = 3.9 V to 10 V	TLV1117-25		1	6	
	I_{OUT} = 0 mA, V_{IN} = 4.75 V to 15 V	TLV1117-33		1	6	
	I_{OUT} = 0 mA, V_{IN} = 6.5 V to 15 V	TLV1117-50		1	10	
Load regulation	I_{OUT} = 10 mA to 800 mA, V_{IN} – V_{OUT} = 3 V	TLV1117		0.2%	0.4%	—
	I_{OUT} = 0 mA to 800 mA, V_{IN} = 2.9 V	TLV1117-15		1	10	mV
	I_{OUT} = 0 mA to 800 mA, V_{IN} = 3.2 V	TLV1117-18		1	10	
	I_{OUT} = 0 mA to 800 mA, V_{IN} = 3.9 V	TLV1117-25		1	10	
	I_{OUT} = 0 mA to 800 mA, V_{IN} = 4.75 V	TLV1117-33		1	10	
	I_{OUT} = 0 mA to 800 mA, V_{IN} = 6.5 V	TLV1117-50		1	15	
Dropout voltage, V_{DO} [2]	I_{OUT} = 100 mA			1.1	1.2	V
	I_{OUT} = 500 mA			1.15	1.25	
	I_{OUT} = 800 mA			1.2	1.3	
Current limit	V_{IN} – V_{OUT} = 5 V, T_J = 25°C[3]		0.8	1.2	1.6	A
Minimum load current	V_{IN} = 15 V	TLV1117		1.7	5	mA
Quiescent current	$V_{IN} \leqslant$ 15 V	All fixed-voltage options		5	10	mA
Thermal regulation	30-ms pulse, T_A = 25°C			0.01	0.1	%/W
Ripple rejection	V_{IN} – V_{OUT} = 3 V, V_{ripple} = 1 V_{pp}, f = 120 Hz		60	75		dB
ADJ pin current				80	120	μA
Change in ADJ pin current	V_{IN} – V_{OUT} = 1.4 V to 10 V, I_{OUT} = 10 mA to 800 mA			0.2	5	μA
Temperature stability	T_J = full range			0.5%		—
Long-term stability	1000 hrs, no load, T_A = 125°C			0.3%		—
Output noise voltage (% of V_{OUT})	f = 10 Hz to 100 kHz			0.003%		—

(1) All characteristics are measured with a 10-μF capacitor across the input and a 10-μF capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
(2) Dropout is defined as the V_{IN} to V_{OUT} differential at which V_{OUT} drops 100 mV below the value of V_{OUT}, measured at V_{IN} = $V_{OUT(nom)}$ + 1.5 V.
(3) Current limit test specified under recommended operating conditions.

6.6 TLV1117I Electrical Characteristics

T_J = –40°C to 125°C, all typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
Reference voltage, V_{REF}	V_{IN} – V_{OUT} = 2 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117	1.238	1.25	1.262	V
	V_{IN} – V_{OUT} = 1.4 V to 10 V, I_{OUT} = 10 mA to 800 mA		1.200	1.25	1.29	
Output voltage, V_{OUT}	V_{IN} = 3.5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-15	1.485	1.5	1.515	
	V_{IN} = 2.9 V to 10 V, I_{OUT} = 0 mA to 800 mA		1.44	1.5	1.56	
	V_{IN} = 3.8 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-18	1.782	1.8	1.818	
	V_{IN} = 3.2 V to 10 V, I_{OUT} = 0 mA to 800 mA		1.728	1.8	1.872	
	V_{IN} = 4.5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-25	2.475	2.5	2.525	
	V_{IN} = 3.9 V to 10 V, I_{OUT} = 0 mA to 800 mA		2.4	2.5	2.6	
	V_{IN} = 5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-33	3.267	3.3	3.333	
	V_{IN} = 4.75 V to 10 V, I_{OUT} = 0 mA to 800 mA		3.168	3.3	3.432	
	V_{IN} = 7 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-50	4.95	5.0	5.05	
	V_{IN} = 6.5 V to 12 V, I_{OUT} = 0 mA to 800 mA		4.80	5.0	5.20	
Line regulation	I_{OUT} = 10 mA, V_{IN} – V_{OUT} = 1.5 V to 13.75 V	TLV1117		0.035%	0.3%	—
	I_{OUT} = 0 mA, V_{IN} = 2.9 V to 10 V	TLV1117-15		1	10	mV
	I_{OUT} = 0 mA, V_{IN} = 3.2 V to 10 V	TLV1117-18		1	10	
	I_{OUT} = 0 mA, V_{IN} = 3.9 V to 10 V	TLV1117-25		1	10	
	I_{OUT} = 0 mA, V_{IN} = 4.75 V to 15 V	TLV1117-33		1	10	
	I_{OUT} = 0 mA, V_{IN} = 6.5 V to 15 V	TLV1117-50		1	15	
Load regulation	I_{OUT} = 10 mA to 800 mA, V_{IN} – V_{OUT} = 3 V	TLV1117		0.2%	0.5%	—
	I_{OUT} = 0 mA to 800 mA, V_{IN} = 2.9 V	TLV1117-15		1	15	mV
	I_{OUT} = 0 mA to 800 mA, V_{IN} = 3.2 V	TLV1117-18		1	15	
	I_{OUT} = 0 mA to 800 mA, V_{IN} = 3.9 V	TLV1117-25		1	15	
	I_{OUT} = 0 mA to 800 mA, V_{IN} = 4.75 V	TLV1117-33		1	15	
	I_{OUT} = 0 mA to 800 mA, V_{IN} = 6.5 V	TLV1117-50		1	20	
Dropout voltage, V_{DO} [2]	I_{OUT} = 100 mA			1.1	1.3	V
	I_{OUT} = 500 mA			1.15	1.35	
	I_{OUT} = 800 mA			1.2	1.4	
Current limit	V_{IN} – V_{OUT} = 5 V, T_J = 25°C[3]		0.8	1.2	1.6	A
Minimum load current	V_{IN} = 15 V	TLV1117		1.7	5	mA
Quiescent current	$V_{IN} \leqslant$ 15 V	All fixed-voltage options		5	15	mA
Thermal regulation	30-ms pulse, T_A = 25°C			0.01	0.1	%/W
Ripple rejection	V_{IN} – V_{OUT} = 3 V, V_{ripple} = 1 V_{pp}, f = 120 Hz		60	75		dB
ADJ pin current				80	120	µA
Change in ADJ pin current	V_{IN} – V_{OUT} = 1.4 V to 10 V, I_{OUT} = 10 mA to 800 mA			0.2	10	µA
Temperature stability	T_J = full range			0.5%		—
Long-term stability	1000 hrs, No load, T_A = 125°C			0.3%		—
Output noise voltage (% of V_{OUT})	f = 10 Hz to 100 kHz			0.003%		—

(1) All characteristics are measured with a 10-µF capacitor across the input and a 10-µF capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
(2) Dropout is defined as the V_{IN} to V_{OUT} differential at which V_{OUT} drops 100 mV below the value of V_{OUT}, measured at V_{IN} = $V_{OUT(nom)}$ + 1.5 V.
(3) Current limit test specified under recommended operating conditions

6.7 Typical Characteristics

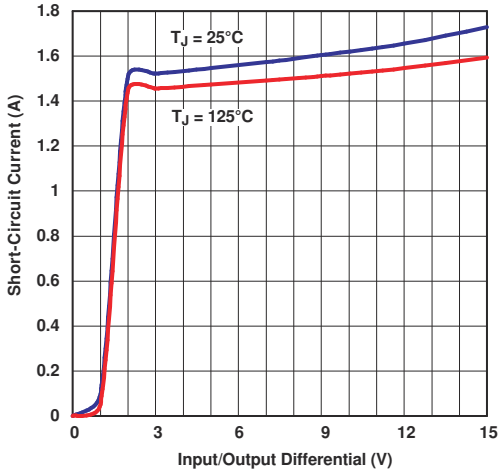


图 6-1. Short-Circuit Current vs (V_{IN} – V_{OUT})

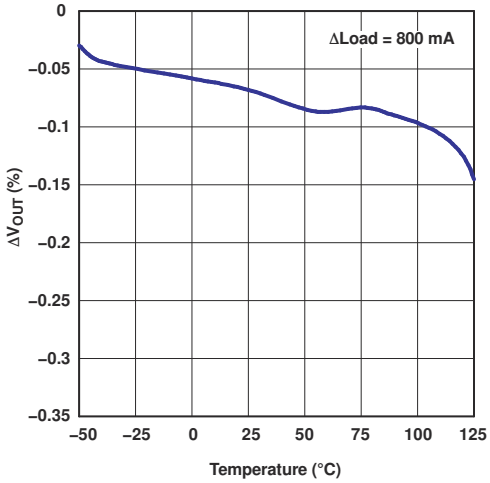


图 6-2. Load Regulation

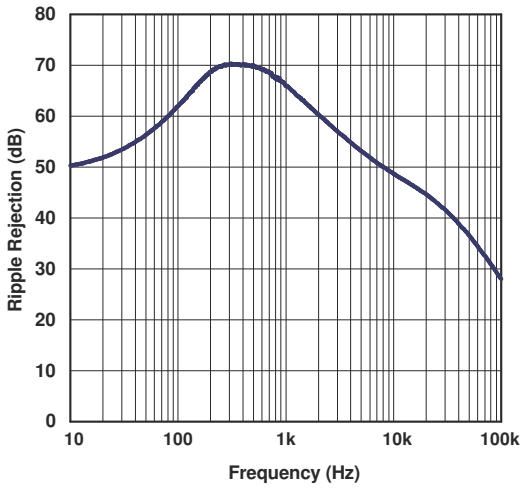


图 6-3. Ripple Rejection vs Frequency (ADJ Version)

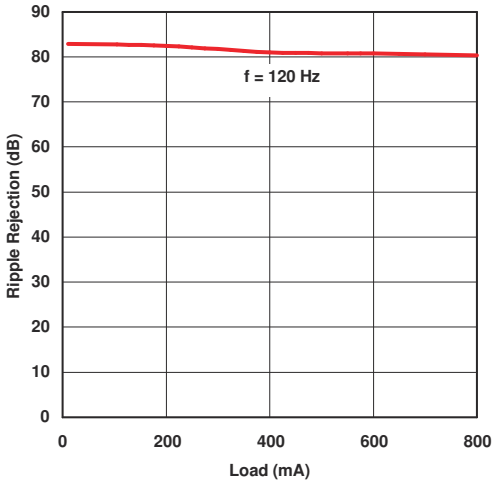


图 6-4. Ripple Rejection vs Load Current (ADJ Version)

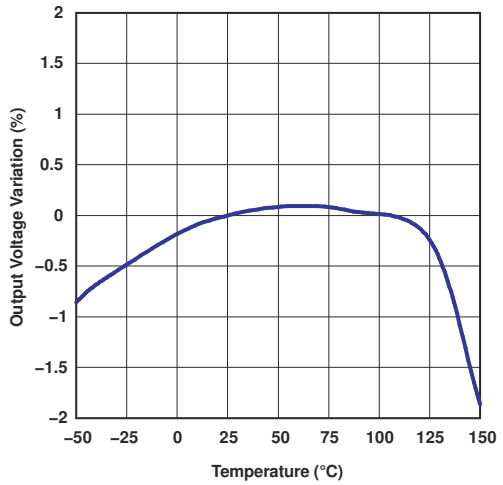


图 6-5. Temperature Stability

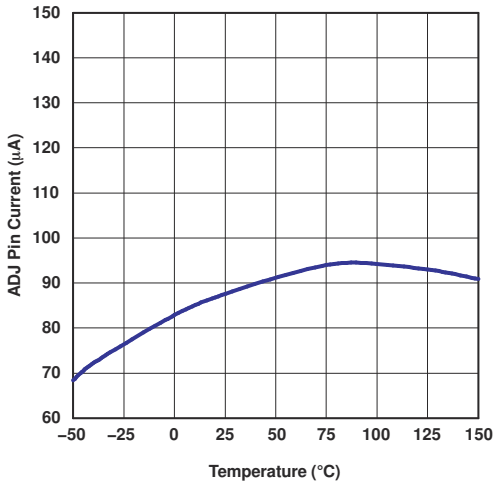


图 6-6. ADJ Pin Current vs Temperature

6.7 Typical Characteristics (continued)

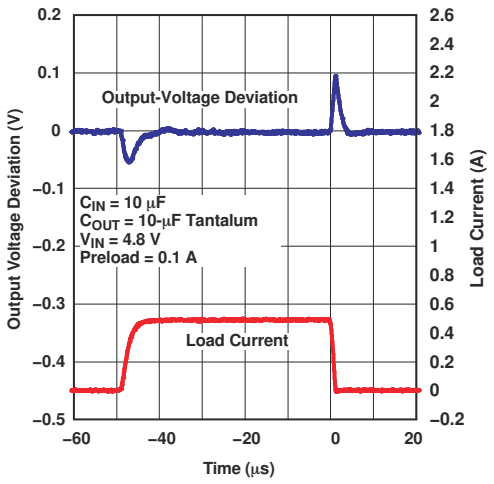


图 6-7. TLV1117-33 Load Transient Response

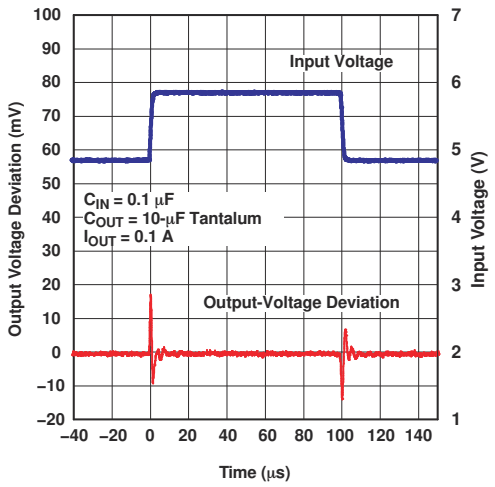


图 6-8. TLV1117-33 Line Transient Response

7 Detailed Description

7.1 Overview

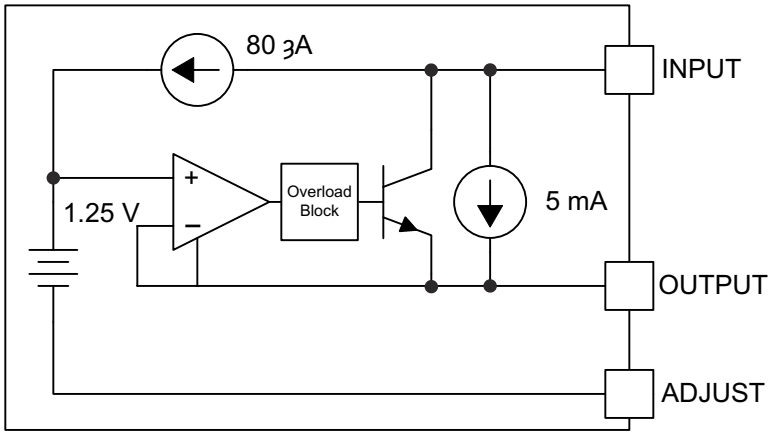
The TLV1117 is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. The device is available in 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V, and adjustable-output voltage options. All internal circuitry is designed to operate down to a 1-V, input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents.

The TLV1117 is designed to be stable with tantalum and aluminum electrolytic output capacitors having an equivalent series resistance (ESR) between 0.2 Ω and 10 Ω.

Unlike positive-negative-positive (PNP)-type regulators, in which up to 10% of the output current is wasted as quiescent current, the quiescent current of the TLV1117 flows into the load, increasing efficiency.

The TLV1117C is characterized for operation over the virtual junction temperature range of 0°C to +125°C, and the TLV1117I is characterized for operation over the virtual junction temperature range of –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 NPN Output Drive

Negative-positive-negative (NPN) output topology provides lower output impedance than most LDOs. However, an output capacitor is required. To support maximum current and lowest temperature, use a 1.4-V headroom (less for lower currents) (V_I – V_O).

7.3.2 Overload Block

Current limiting and overtemperature shutdown protects against overload or under heat sinking.

7.3.3 Programmable Feedback

An op amp with a 1.25-V offset input at the ADJUST pin provides easy output voltage programming. For current regulation applications, use a single resistor whose resistance value is 1.25 V / IOUT with a power rating greater than $(1.25\ V)^2$ / R. For voltage regulation applications, two resistors set the output voltage.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device OUTPUT pin sources current necessary to make the OUTPUT pin 1.25 V greater than the ADJUST terminal to provide output regulation.

7.4.2 Operation With Low Input Voltage

The adjustable version of the device requires a 1-V headroom (V_I – V_O) to operate in regulation. With less headroom, the device can drop out and the OUTPUT voltage is the INPUT voltage minus the dropout voltage.

7.4.3 Operation at Light Loads

The device passes the bias current to the OUTPUT pin. The load or feedback must consume this minimum current for regulation or the output can possibly be too high.

7.4.4 Operation in Self Protection

When an overload occurs, the device shuts down the output stage or reduces the output current to prevent device damage. The device automatically resets from the overload. The output can be reduced or alternate between on and off until the overload is removed.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TLV1117 is a versatile and high-performance, linear regulator with a wide temperature range and tight line and load regulation operation. An output capacitor is required to further improve transient response and stability. For the adjustable option, the ADJ pin can also be bypassed to achieve very-high, ripple-rejection ratios. The TLV1117 is versatile in the device applications, including being used as a post regulator for DC/DC converters, battery chargers, and microprocessor supplies.

8.2 Typical Application

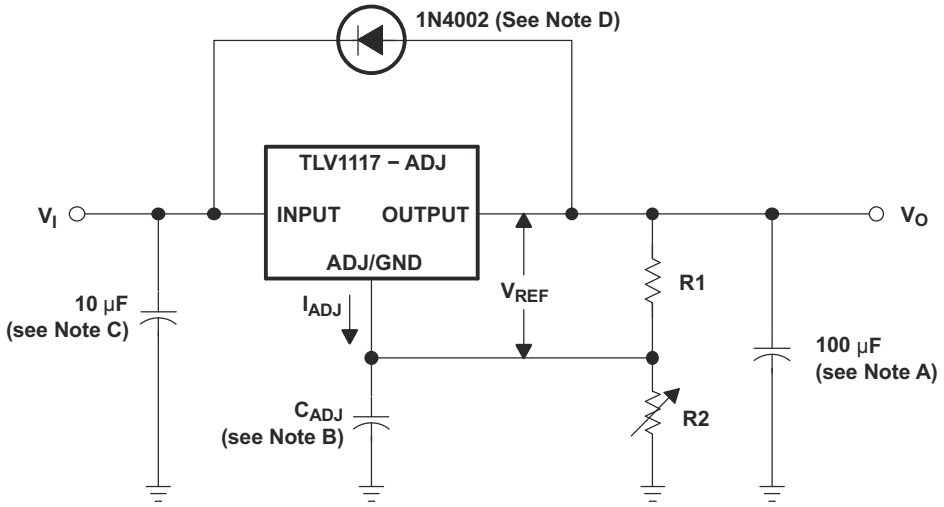


图 8-1. Basic Adjustable Regulator

The adjustable version of the TLV1117 takes a 2.7-V to 15-V input. The voltage V_{REF} refers to the voltage between the output and the ADJUST pin, typically 1.25 V. The V_{REF} voltage causes a current to flow across R1, which is the same current that flows across R2 (minus the negligible 50-µA I_{ADJ}). Therefore, R2 can be adjusted to create a larger voltage drop from GND and set the output voltage. The output voltage equation is described in the *Detailed Design Procedure* section.

8.2.1 Design Requirements

- (A) Output capacitor selection is critical for regulator stability. Larger C_{OUT} values benefit the regulator by improving transient response and loop stability. This device is designed to be stable with tantalum and aluminum electrolytic output capacitors having an ESR between 0.2 Ω and 10 Ω.
- (B) C_{ADJ} can be used to improve ripple rejection. If C_{ADJ} is used, a C_{OUT} that is larger in value than C_{ADJ} must be used.
- (C) C_{IN} is recommended if the TLV1117 is not located near the power-supply filter.
- (D) An external diode is recommended to protect the regulator if the input instantaneously is shorted to GND.

8.2.2 Detailed Design Procedure

The output voltage can be calculated as shown in 方程式 1:

$$V_{OUT} = V_{REF}\left(1+\frac{R2}{R1}\right)+\left(I_{ADJ}\times R2\right) \quad (1)$$

I_{ADJ} can be neglected in most applications because the value is approximately 80 μA.

8.2.3 Application Curve

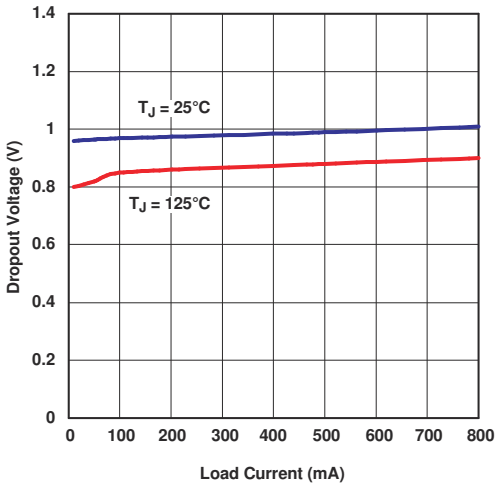


图 8-2. Dropout Voltage vs Load Current

8.3 Power Supply Recommendations

The fixed and adjustable versions of the TLV1117 have different recommended ranges of operating voltage. See the *Recommended Operating Conditions* table for specific operating ranges.

8.4 Layout

8.4.1 Layout Guidelines

One or two input capacitors are recommended if the TLV1117 is not located near the power-supply output filter capacitor. These capacitors can filter high-frequency noise and mitigate brief voltage surges from the input. Traces on the input and output pins of the device must be wide enough to support the full range of current needed in the application to minimize I×R drop.

8.4.2 Layout Example

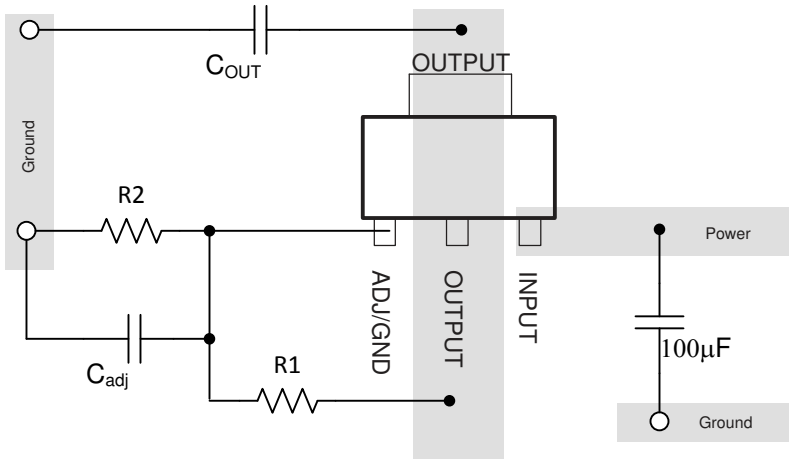


图 8-3. Layout Example

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1117-15CDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	T2	Samples
TLV1117-15CDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	T2	Samples
TLV1117-15CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	T2	Samples
TLV1117-15CDRJR	ACTIVE	SON	DRJ	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYH	Samples
TLV1117-15IDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T3	Samples
TLV1117-15IDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T3	Samples
TLV1117-15IKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	ZF15	Samples
TLV1117-18CDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	T4	Samples
TLV1117-18CDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	T4	Samples
TLV1117-18CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	T4	Samples
TLV1117-18CDRJR	ACTIVE	SON	DRJ	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYK	Samples
TLV1117-18CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	ZE18	Samples
TLV1117-18IDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T5	Samples
TLV1117-18IDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T5	Samples
TLV1117-18IDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T5	Samples
TLV1117-18IDRJR	ACTIVE	SON	DRJ	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYL	Samples
TLV1117-18IKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	ZF18	Samples
TLV1117-25CDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	T6	Samples
TLV1117-25CDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	T6	Samples
TLV1117-25CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	T6	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1117-25CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	ZE25	Samples
TLV1117-25IDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T8	Samples
TLV1117-25IDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T8	Samples
TLV1117-25IDRJR	ACTIVE	SON	DRJ	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYN	Samples
TLV1117-33CDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	V3	Samples
TLV1117-33CDCYG3	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	V3	Samples
TLV1117-33CDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	V3	Samples
TLV1117-33CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	V3	Samples
TLV1117-33CDRJR	ACTIVE	SON	DRJ	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYP	Samples
TLV1117-33CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	ZE33	Samples
TLV1117-33IDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	(V3, VS)	Samples
TLV1117-33IDCYG3	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	(V3, VS)	Samples
TLV1117-33IDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	VS	Samples
TLV1117-33IDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	VS	Samples
TLV1117-33IDRJR	ACTIVE	SON	DRJ	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYR	Samples
TLV1117-33IKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	ZF33	Samples
TLV1117-50CDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	VT	Samples
TLV1117-50CDCYG3	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	VT	Samples
TLV1117-50CDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	VT	Samples
TLV1117-50CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	VT	Samples
TLV1117-50CDRJR	ACTIVE	SON	DRJ	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZE50	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1117-50CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	ZE50	Samples
TLV1117-50IDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	VU	Samples
TLV1117-50IDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	VU	Samples
TLV1117-50IDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	VU	Samples
TLV1117-50IDRJR	ACTIVE	SON	DRJ	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZF50	Samples
TLV1117-50IDRJRG4	ACTIVE	SON	DRJ	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZF50	Samples
TLV1117-50IKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	ZF50	Samples
TLV1117CDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	V4	Samples
TLV1117CDCYG3	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	V4	Samples
TLV1117CDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	V4	Samples
TLV1117CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	V4	Samples
TLV1117CDRJR	ACTIVE	SON	DRJ	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 125	ZYS	Samples
TLV1117CKCS	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TLV1117C	Samples
TLV1117CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS & Green	SN	Level-3-245C-168 HR	0 to 125	TLV1117C	Samples
TLV1117CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS & Green	SN	Level-3-245C-168 HR	0 to 125	TLV1117C	Samples
TLV1117CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	TV1117	Samples
TLV1117IDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	V2	Samples
TLV1117IDCYG3	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	V2	Samples
TLV1117IDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	V2	Samples
TLV1117IDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	V2	Samples
TLV1117IDRJR	ACTIVE	SON	DRJ	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYT	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1117IKCS	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	TLV1117I	Samples
TLV1117IKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	TLV1117I	Samples
TLV1117IKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	TLV1117I	Samples
TLV1117IKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	TY1117	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

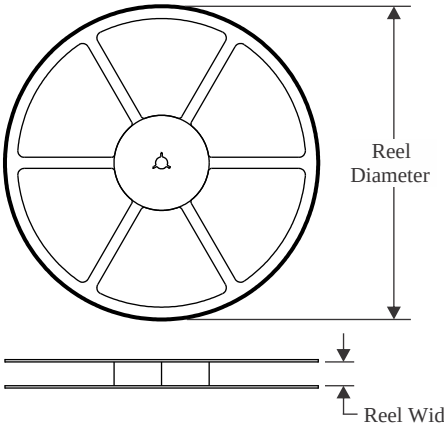
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

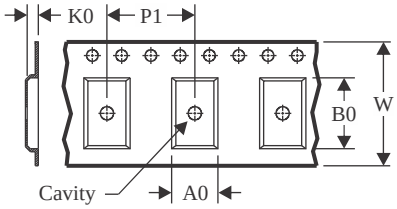
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

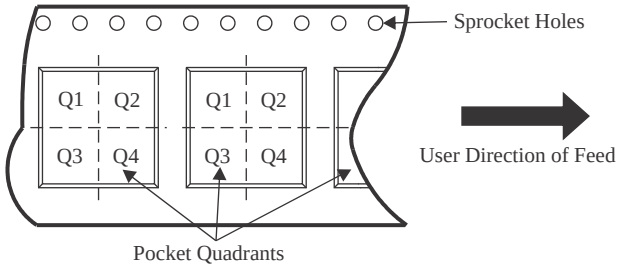


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

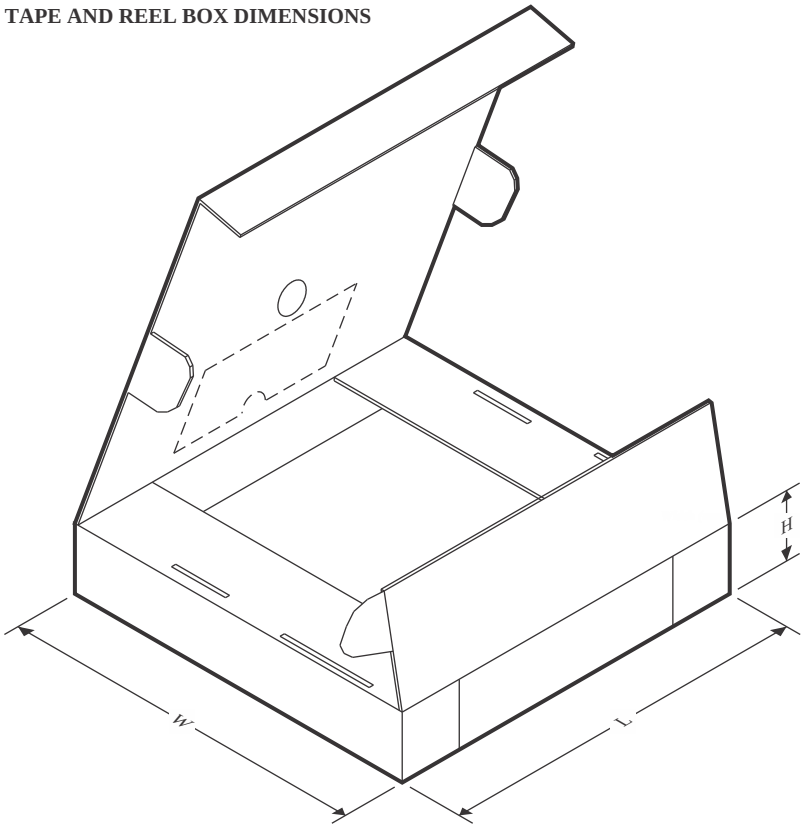


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1117-15CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-15CDRJR	SON	DRJ	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-15IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-15IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-15IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-18CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-18CDRJR	SON	DRJ	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-18CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-18IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-18IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-18IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-25CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-25CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-25CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-25IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-25IDRJR	SON	DRJ	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1117-33CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-33CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-33CDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-33CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-33IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-33IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-33IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-33IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-50CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-50CDRJR	SON	DRJ	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-50CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117-50IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117-50IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117-50IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117-50IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117CDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TLV1117CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV1117IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TLV1117IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
TLV1117IDRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV1117IKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TLV1117IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

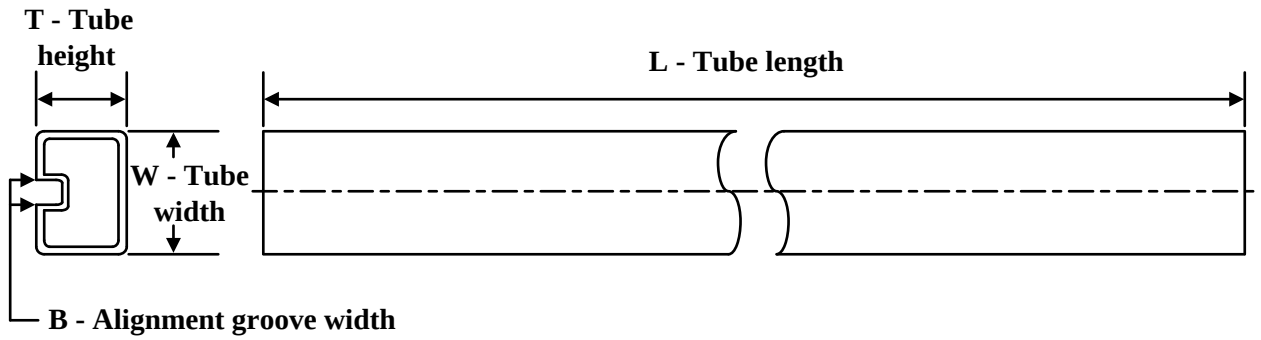


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1117-15CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-15CDRJR	SON	DRJ	8	3000	367.0	367.0	35.0
TLV1117-15IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-15IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-15IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-18CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-18CDRJR	SON	DRJ	8	3000	367.0	367.0	35.0
TLV1117-18CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-18IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-18IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-18IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-25CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-25CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-25CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-25IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-25IDRJR	SON	DRJ	8	3000	367.0	367.0	35.0
TLV1117-33CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-33CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1117-33CDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-33CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-33IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-33IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-33IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-33IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-50CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-50CDRJR	SON	DRJ	8	3000	367.0	367.0	35.0
TLV1117-50CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117-50IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117-50IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117-50IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117-50IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117CDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TLV1117CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV1117IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TLV1117IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
TLV1117IDRJR	SON	DRJ	8	1000	210.0	185.0	35.0
TLV1117IKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TLV1117IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0

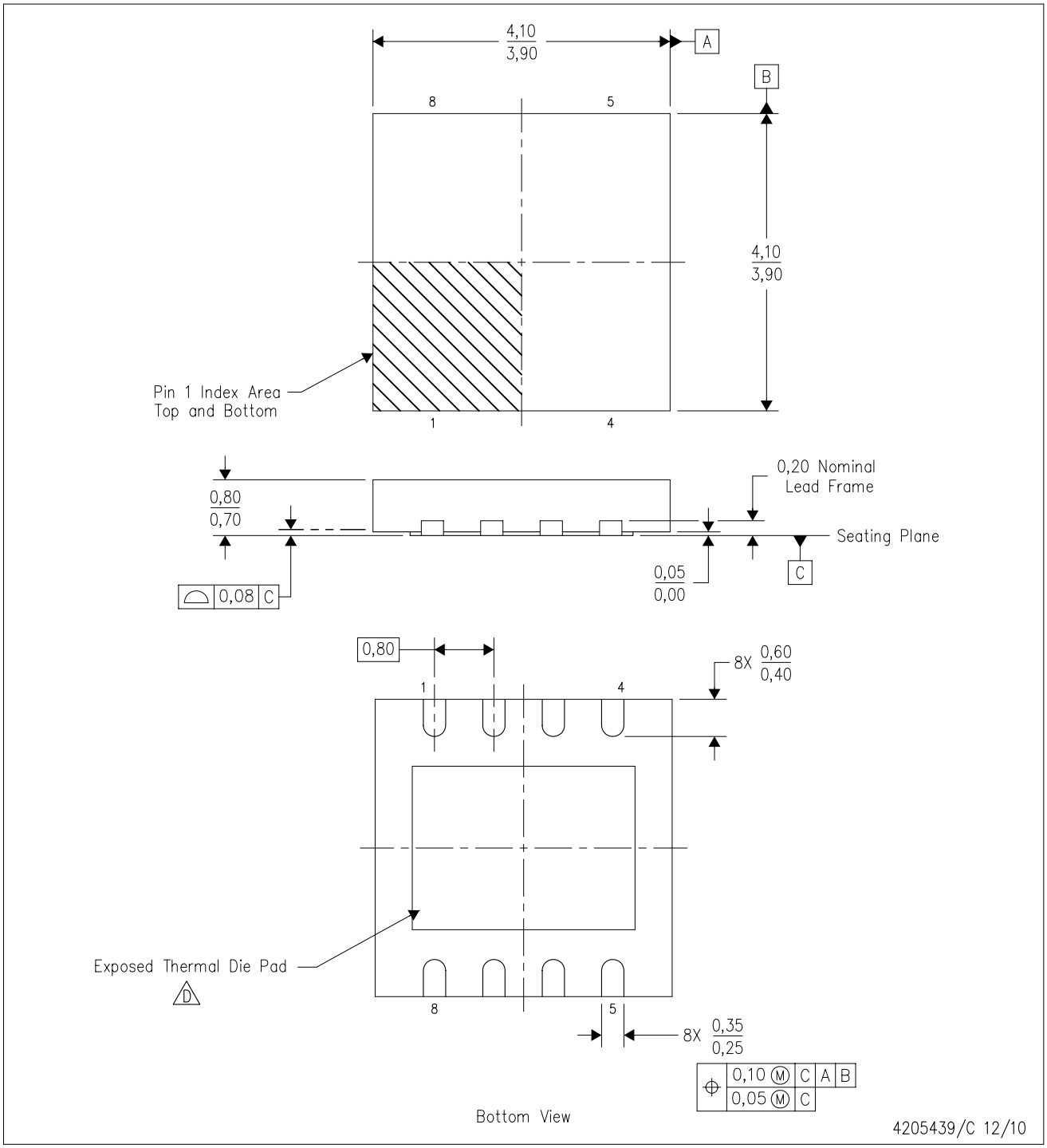
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV1117-15CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-15IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-18CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-18IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-25CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-25IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-33CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-33CDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-33IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-33IDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-50CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-50CDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117-50IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117CDCY	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
TLV1117CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117CDCYG3	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
TLV1117CDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
TLV1117CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
TLV1117IDCY	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
TLV1117IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117IDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
TLV1117IDCYG3	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
TLV1117IKCS	KCS	TO-220	3	50	532	34.1	700	9.6
TLV1117IKCS	KCS	TO-220	3	50	532	34.1	700	9.6
TLV1117IKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
TLV1117IKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6

DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229 variation WGGB.

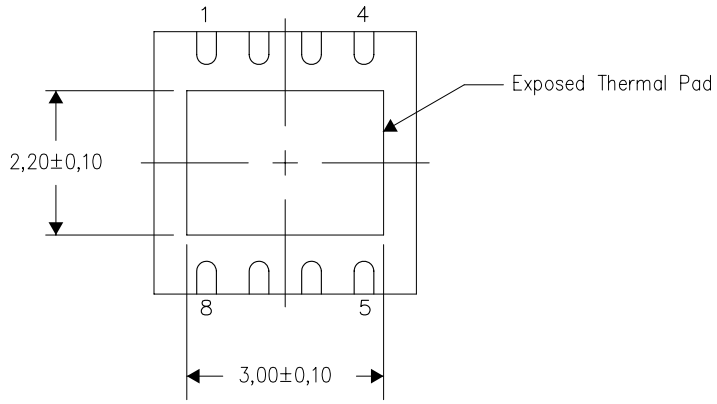
DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



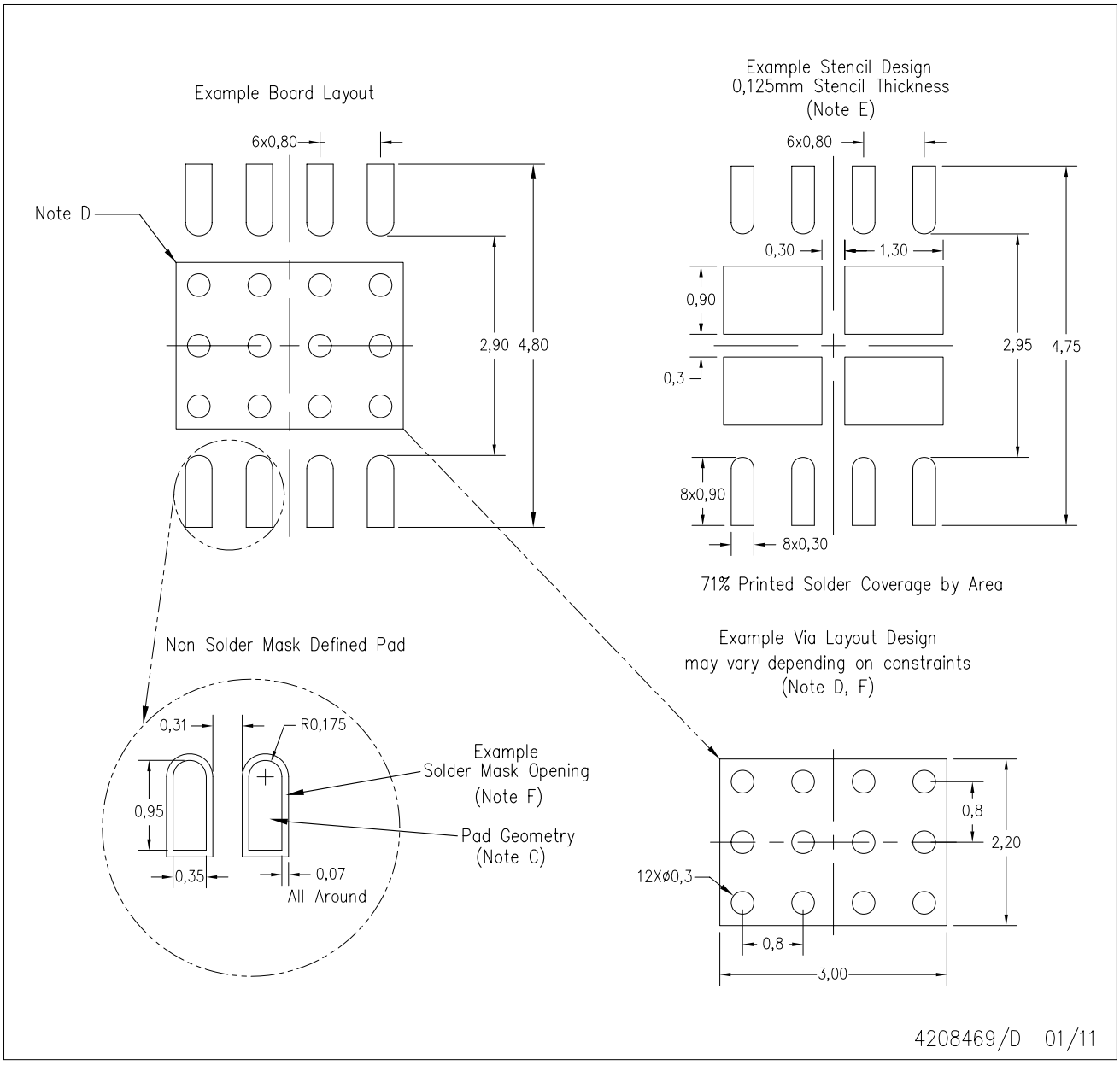
Bottom View

Exposed Thermal Pad Dimensions

4206882/F 01/11

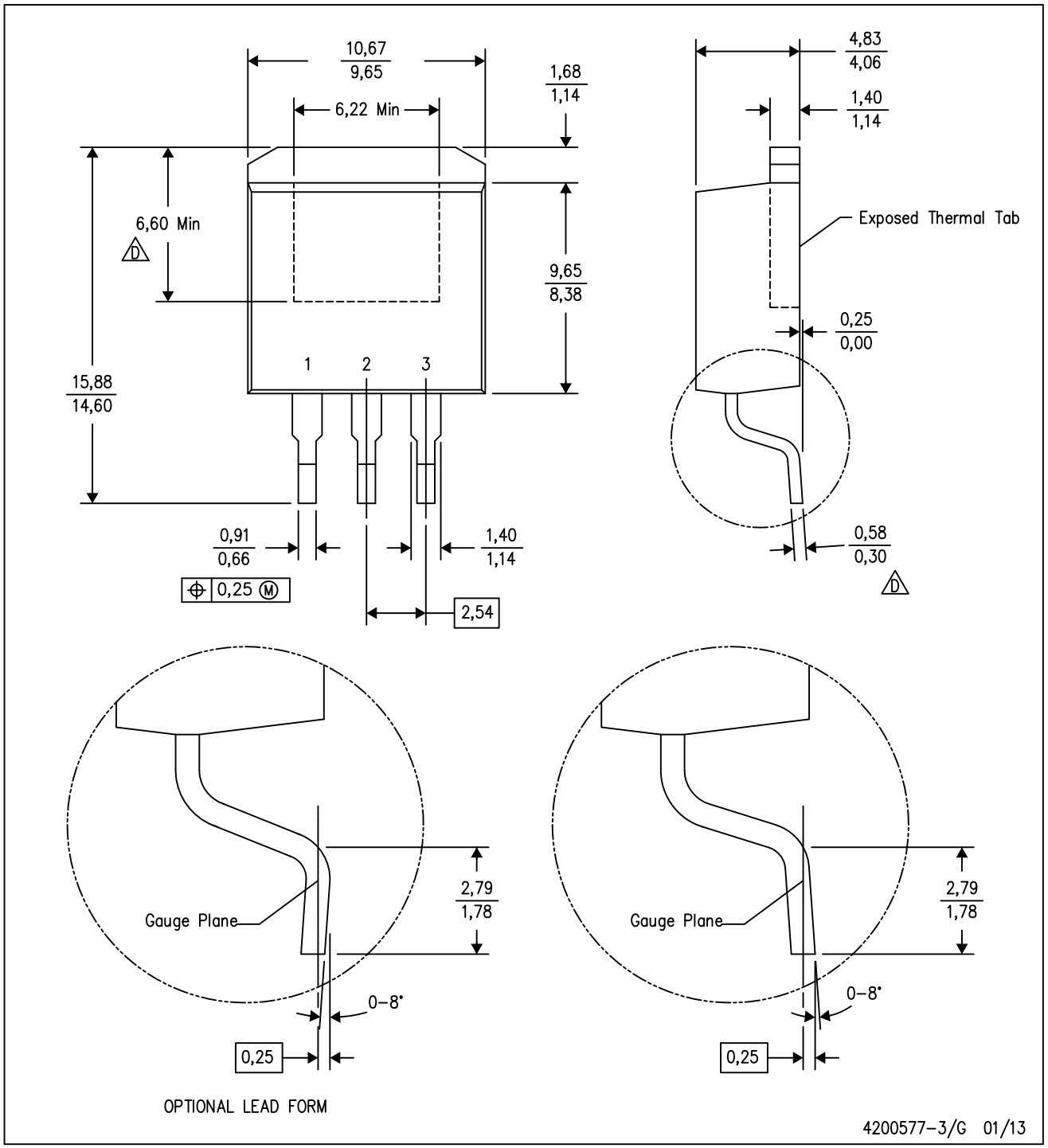
NOTE: All linear dimensions are in millimeters

DRJ (S–PWSON–N8) SMALL PACKAGE OUTLINE NO–LEAD



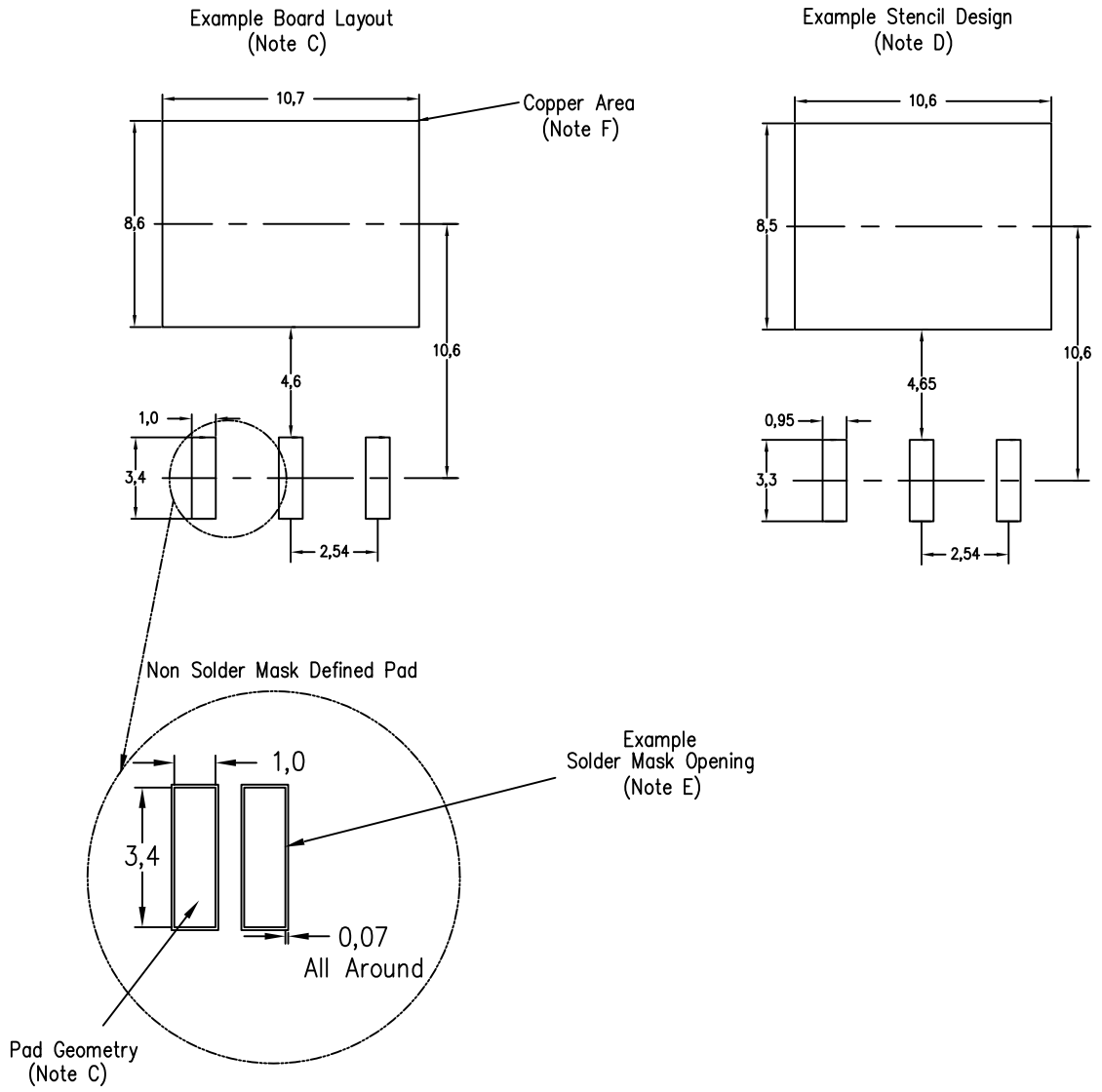
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

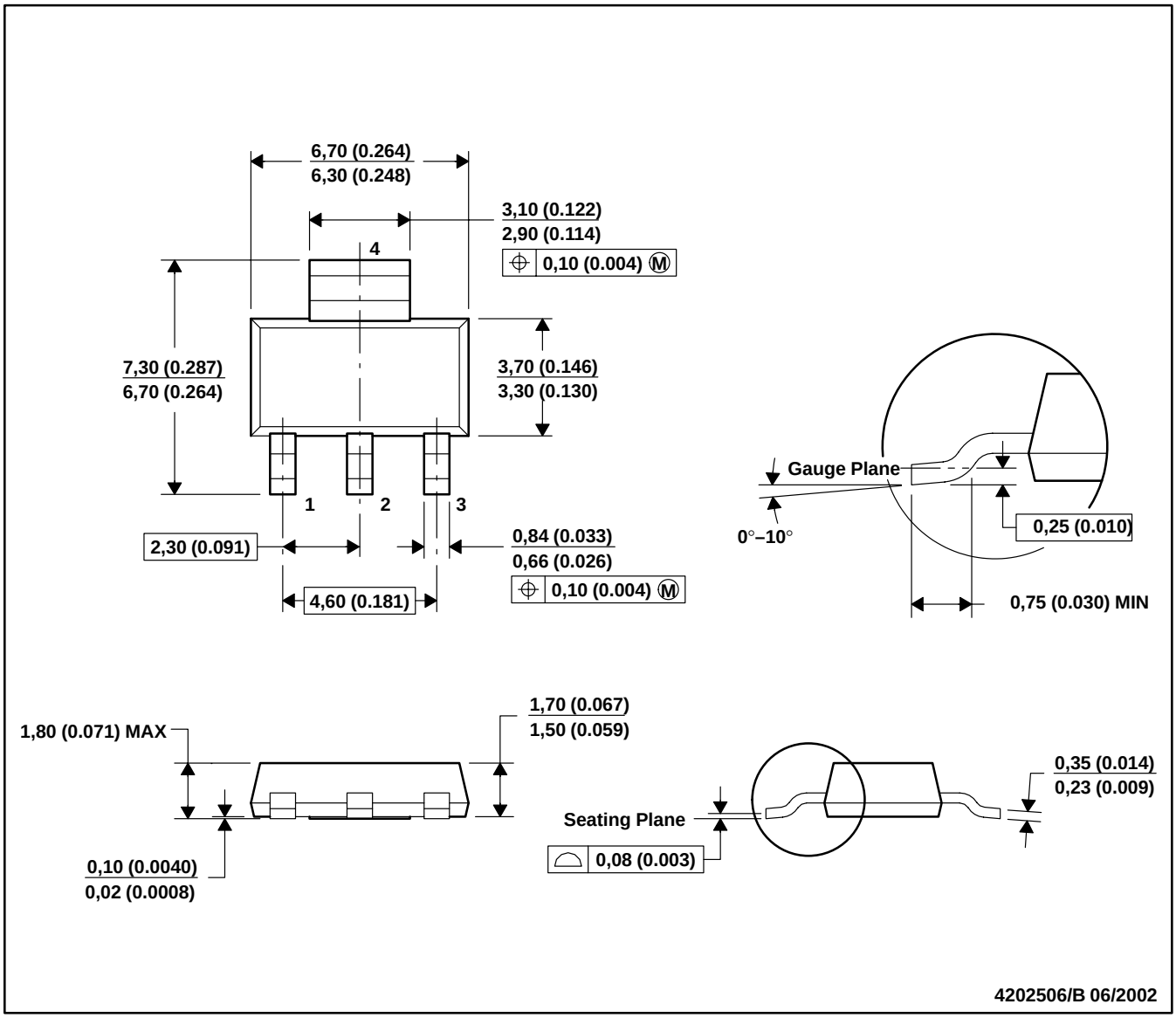
KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

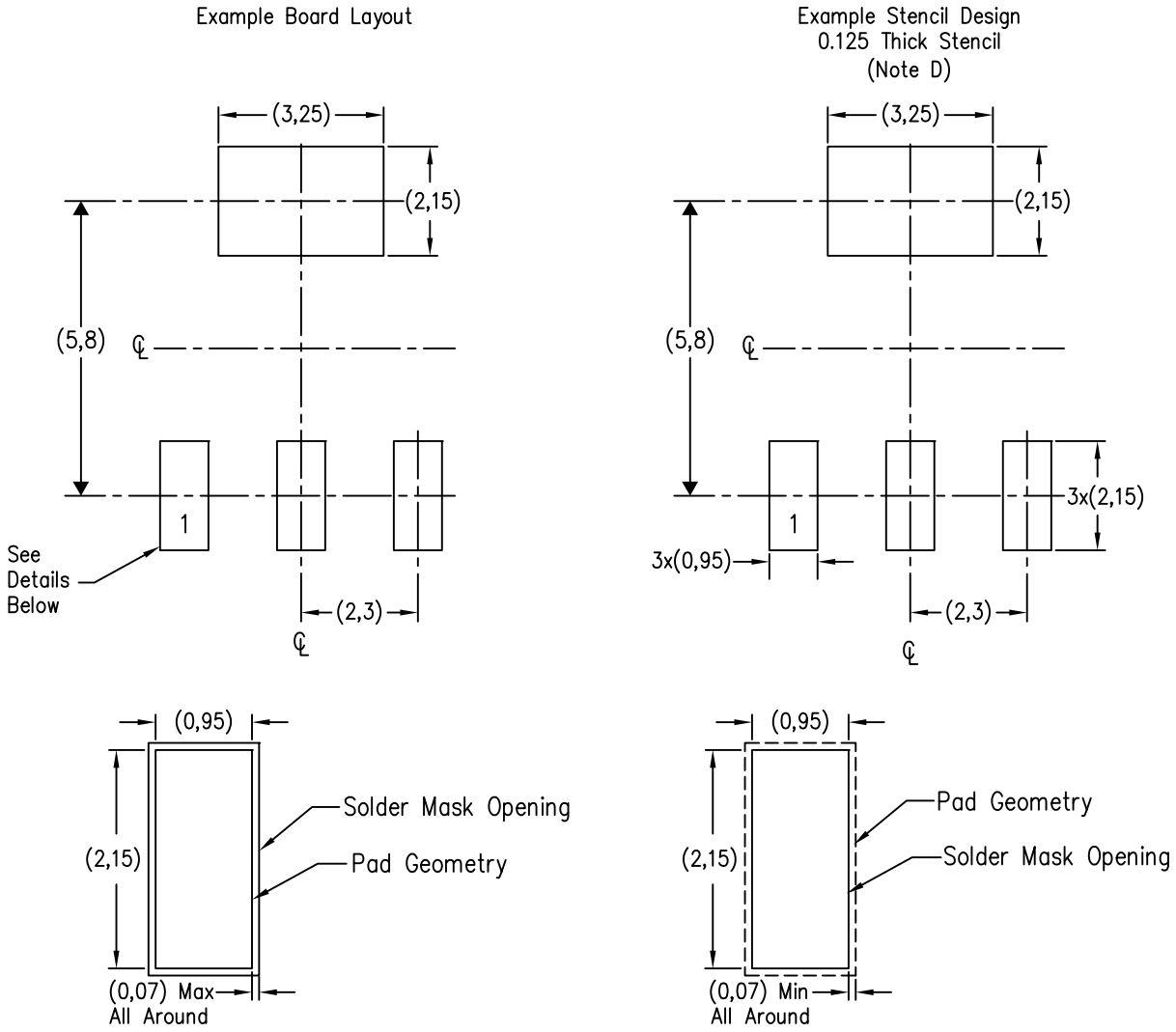
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

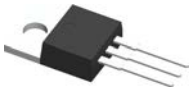
DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

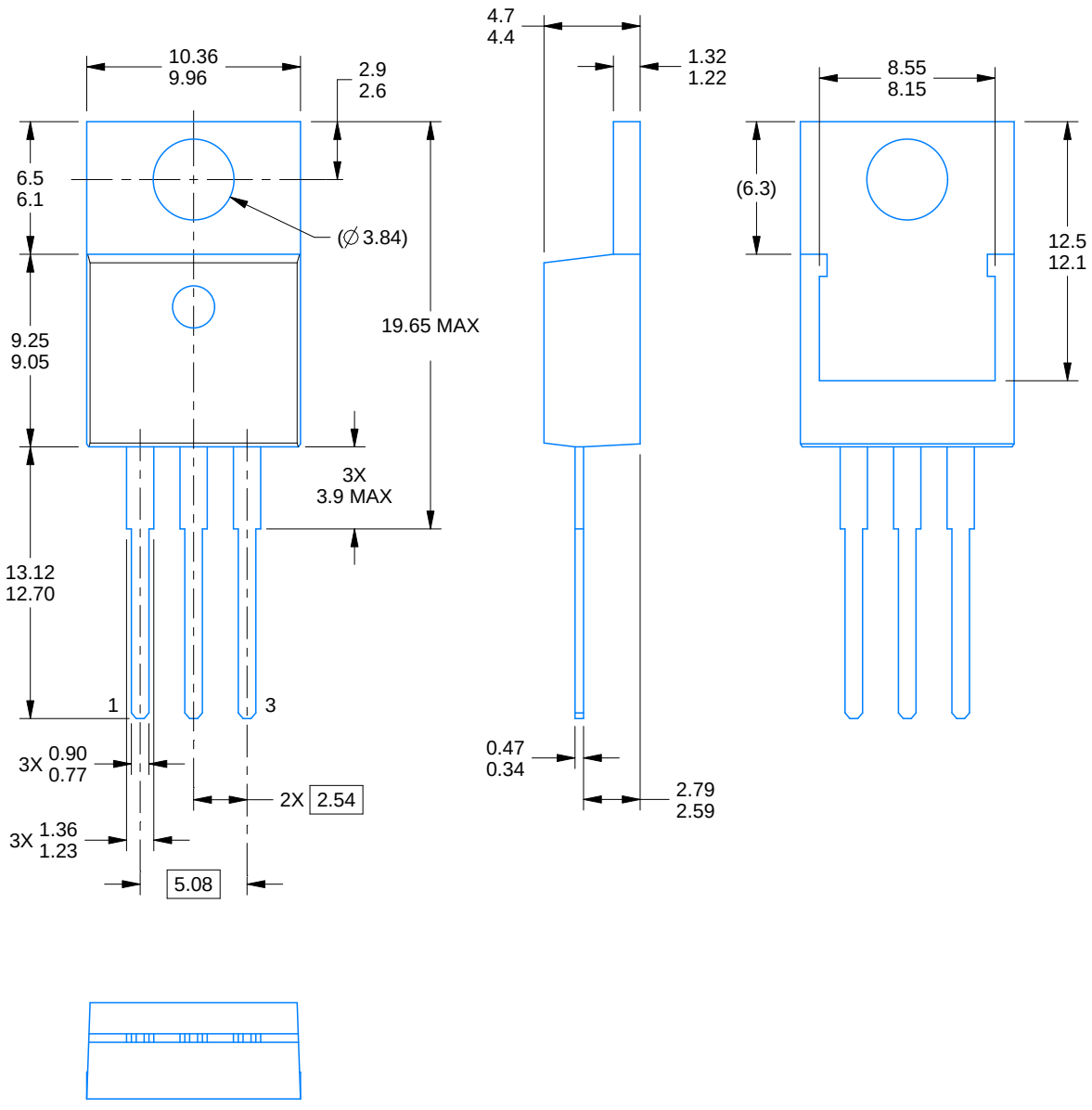
KCS0003B



PACKAGE OUTLINE

TO-220 - 19.65 mm max height

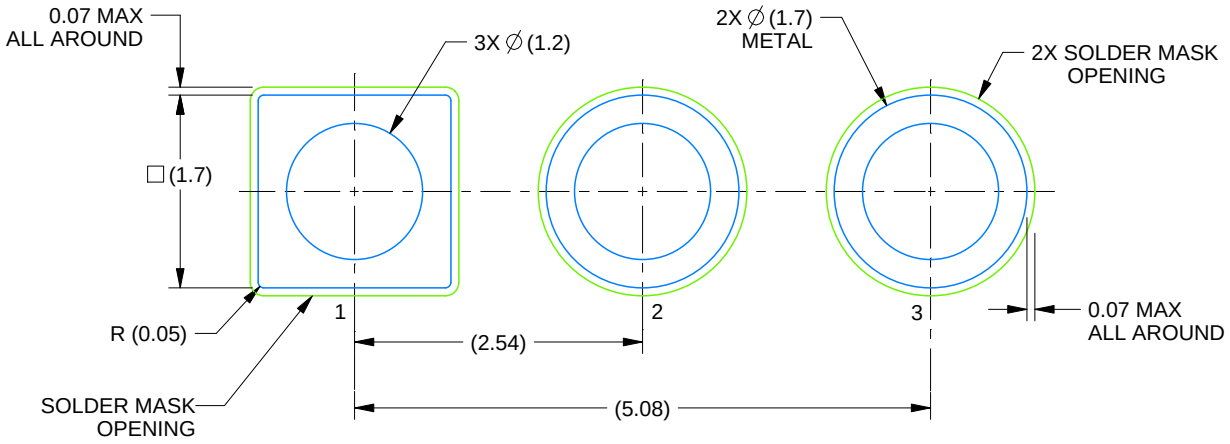
TO-220



4222214/B 08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



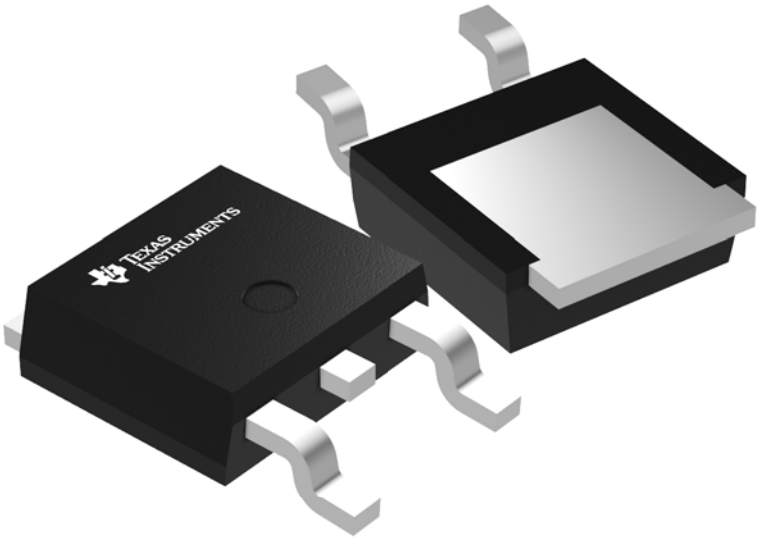
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



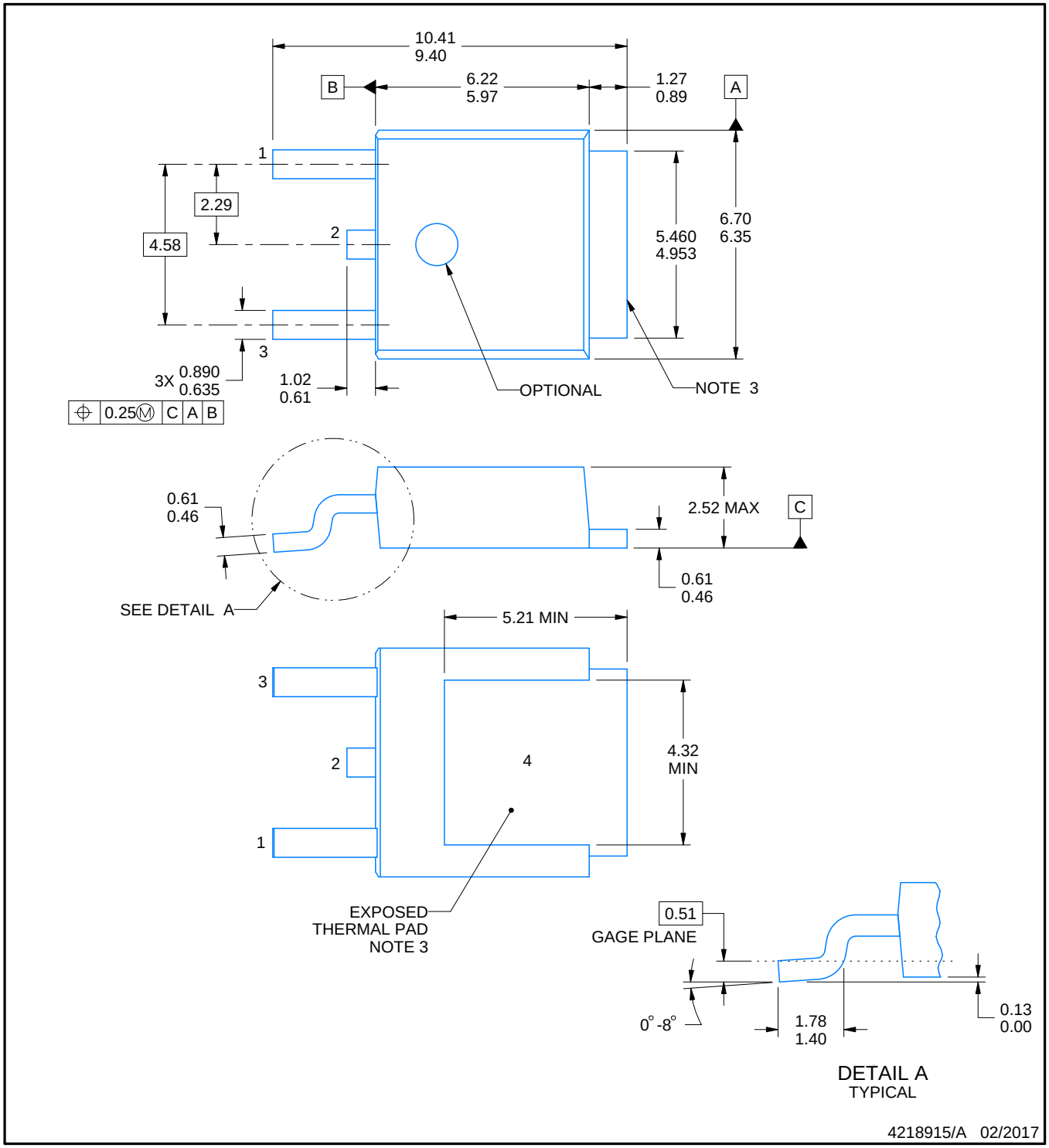
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

KVU0003A

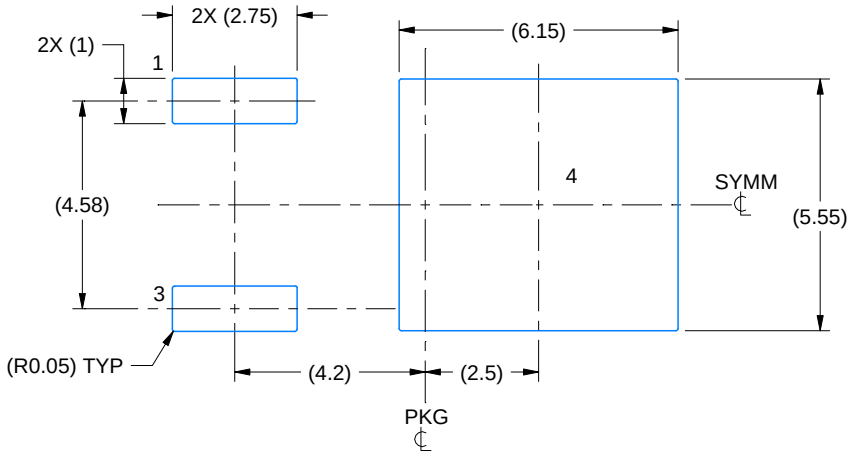
TO-252 - 2.52 mm max height

TO-252

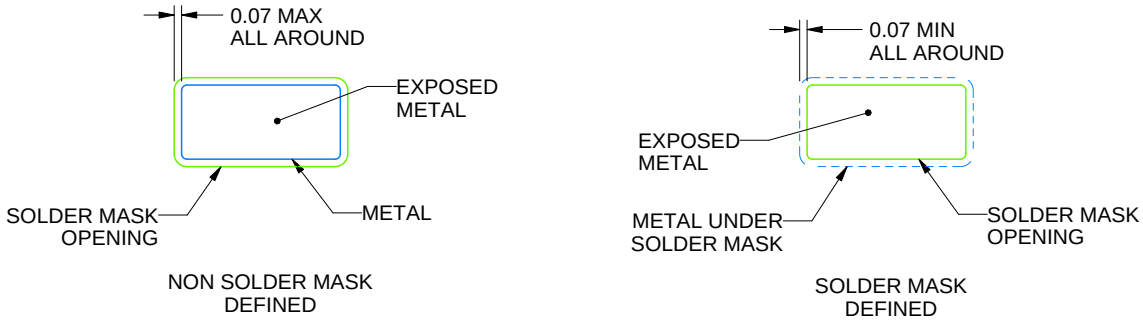


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

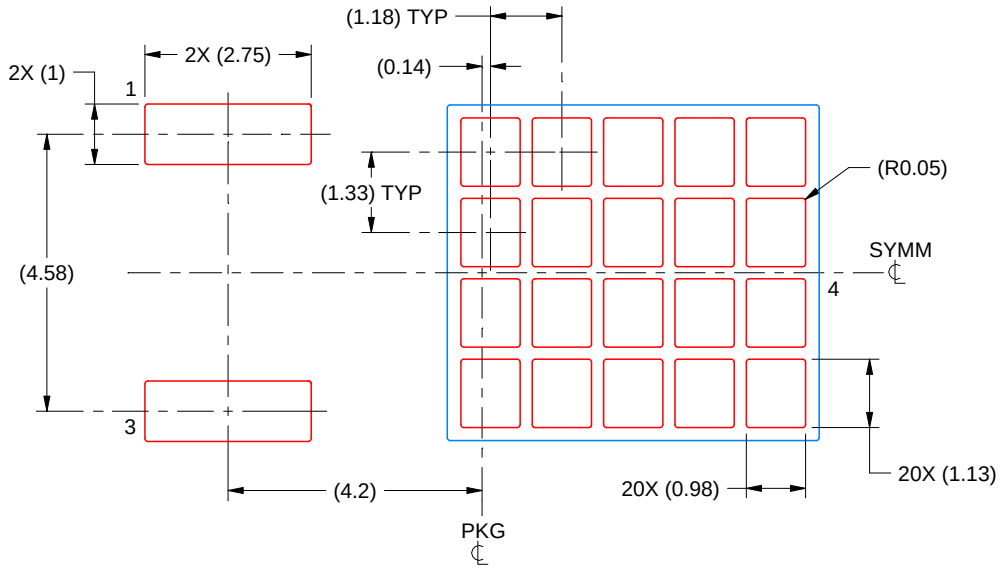
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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