

SN74LVC1G34 Single Buffer Gate

1 Features

- Available in the Ultra Small 0.64-mm² Package (DPW) with 0.5-mm Pitch
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to V_{CC}
- Max t_{pd} of 3.5 ns at 3.3 V
- Low Power Consumption, 1-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- DVD Recorder and Player
- Embedded PC
- MP3 Player/Recorder (Portable Audio)
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

4 Simplified Schematic



3 Description

This single buffer gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G34 device performs the Boolean function $Y = A$ in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} Operating range.

The SN74LVC1G34 is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8 mm × 0.8 mm.

Device Information⁽¹⁾

| DEVICE NAME | PACKAGE (PINS) | BODY SIZE |
|----------------|----------------|-------------------|
| SN74LVC1G34YFP | DSBGA (4) | 0.76 mm × 0.76 mm |
| SN74LVC1G34YZP | DSBGA (5) | 1.38 mm × 0.88 mm |
| SN74LVC1G34YZV | DSBGA (4) | 0.88 mm × 0.88 mm |
| SN74LVC1G34DPW | X2SON (5) | 0.80 mm × 0.80 mm |
| SN74LVC1G34DBV | SOT-23 (5) | 2.90 mm × 2.80 mm |
| SN74LVC1G34DCK | SC70 (5) | 2.00 mm × 2.10 mm |
| SN74LVC1G34DRL | SOT (5) | 1.60 mm × 1.60 mm |
| SN74LVC1G34DRY | SON (6) | 1.45 mm × 1.00 mm |
| SN74LVC1G34DSF | SON(6) | 1.00 mm × 1.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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5 Revision History

Changes from Revision L (April 2014) to Revision M

Page

| | | |
|---|--|---|
| • | Changed X2SON from 4 pin to 5 pin on <i>Device Information</i> table | 1 |
| • | Moved Storage temperature range from <i>ESD Ratings</i> table to <i>Absolute Maximum Ratings</i> table | 5 |
| • | Added Junction temperature to <i>Absolute Maximum Ratings</i> table | 5 |
| • | Added package temperature specification for DSBGA package | 6 |

Changes from Revision K (March 2014) to Revision L

Page

| | | |
|---|--|----|
| • | Added Device Information table. | 1 |
| • | Added Pin Functions table. | 4 |
| • | Updated Handling Ratings table. | 5 |
| • | Updated operating temperature range. | 6 |
| • | Added Thermal Information table. | 6 |
| • | Added Typical Characteristics. | 8 |
| • | Added Detailed Description section. | 11 |
| • | Added Application and Implementation section. | 12 |

Changes from Revision J (December 2013) to Revision K

Page

| | | |
|---|---|---|
| • | Added Applications. | 1 |
| • | DPW Package. | 4 |
| • | Moved T_{stg} to Handling Ratings table. | 5 |

Changes from Revision I (June2011) to Revision J**Page**

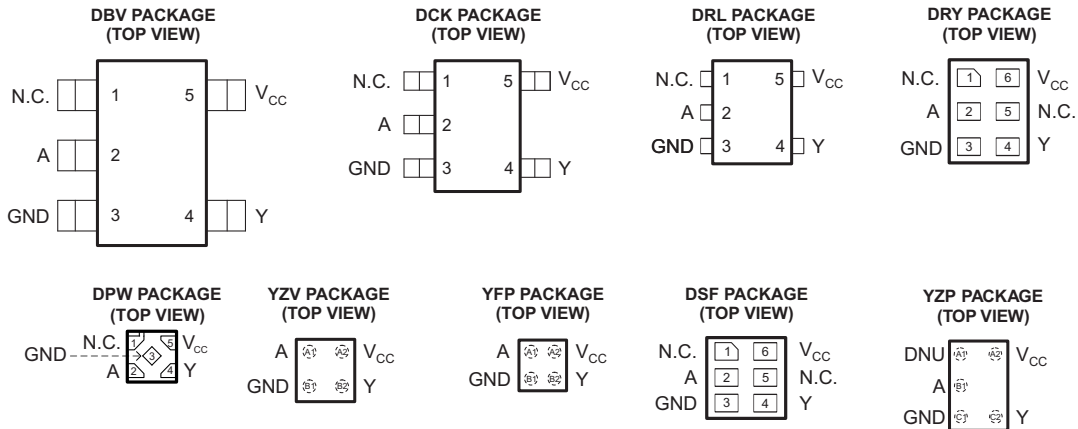
-
- Updated document to new TI data sheet format. 1
 - Removed Ordering Information table. 1
-

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6 Pin Configuration and Functions



See mechanical drawings for dimensions.
 N.C. – No internal connection
 DNU – Do not use

Pin Functions

| NAME | PIN | | | | | DESCRIPTION |
|-----------------|---------------|-----|----------|-----|----------|---------------|
| | DRL, DCK, DBV | DPW | DRY, DSF | YZP | YFP, YZV | |
| NC | 1 | 1 | 1, 5 | A1 | – | Not connected |
| A | 2 | 2 | 2 | B1 | A1 | Input |
| GND | 3 | 3 | 3 | C1 | B1 | Ground |
| Y | 4 | 4 | 4 | C2 | B2 | Output |
| V _{CC} | 5 | 5 | 6 | A2 | A2 | Power pin |

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------|---|-----------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V_I | Input voltage range | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through V_{CC} or GND | | ±100 | mA |
| T_{stg} | Storage temperature range | -65 | 150 | °C |
| T_J | Max Junction temperature | | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

7.2 ESD Ratings

| | | MIN | MAX | UNIT |
|-------------|-------------------------|--|-----|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±1 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT | |
|-----------------|------------------------------------|---|------------------------|------------------------|------|
| V _{CC} | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 3 V to 3.6 V | 2 | | |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 0.7 | |
| | | V _{CC} = 3 V to 3.6 V | | 0.8 | |
| | | V _{CC} = 4.5 V to 5.5 V | | 0.3 × V _{CC} | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | 0 | V _{CC} | V | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | –4 | mA |
| | | V _{CC} = 2.3 V | | –8 | |
| | | V _{CC} = 3 V | | –16 | |
| | | V _{CC} = 4.5 V | | –24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | |
| | | V _{CC} = 3 V | | 16 | |
| | | V _{CC} = 4.5 V | | 24 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | V _{CC} = 3.3 V ± 0.3 V | | 10 | |
| | | V _{CC} = 5 V ± 0.5 V | | 10 | |
| T _A | Operating free-air temperature | DSBGA package | –40 | 85 | °C |
| | | All other packages | –40 | 125 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74LVC1G34 | | | | | | UNIT | |
|-------------------------------|--|--------|--------|--------|--------|--------|------|------|
| | DBV | DCK | DRL | DRY | YZP | DPW | | |
| | 5 PINS | 5 PINS | 5 PINS | 6 PINS | 5 PINS | 4 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 229 | 278 | 243 | 439 | 130 | 340 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 164 | 93 | 78 | 277 | 54 | 215 | |
| R _{θJB} | Junction-to-board thermal resistance | 62 | 65 | 78 | 271 | 51 | 294 | |
| Ψ _{JT} | Junction-to-top characterization parameter | 44 | 2 | 10 | 84 | 1 | 41 | |
| Ψ _{JB} | Junction-to-board characterization parameter | 62 | 64 | 77 | 271 | 50 | 294 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | – | – | – | – | – | 250 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | –40°C to 85°C | | | –40°C to 125°C | | | UNIT |
|------------------|---|-----------------|-----------------------|--------------------|-----|-----------------------|--------------------|-----|------|
| | | | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP ⁽¹⁾ | MAX | |
| V _{OH} | I _{OH} = –100 μA | 1.65 V to 5.5 V | V _{CC} – 0.1 | | | V _{CC} – 0.1 | | | V |
| | I _{OH} = –4 mA | 1.65 V | 1.2 | | | 1.2 | | | |
| | I _{OH} = –8 mA | 2.3 V | 1.9 | | | 1.9 | | | |
| | I _{OH} = –16 mA | 3 V | 2.4 | | | 2.4 | | | |
| | I _{OH} = –24 mA | | 2.3 | | | 2.3 | | | |
| | I _{OH} = –32 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 5.5 V | 0.1 | | | 0.1 | | | V |
| | I _{OL} = 4 mA | 1.65 V | 0.45 | | | 0.45 | | | |
| | I _{OL} = 8 mA | 2.3 V | 0.3 | | | 0.3 | | | |
| | I _{OL} = 16 mA | 3 V | 0.4 | | | 0.4 | | | |
| | I _{OL} = 24 mA | | 0.55 | | | 0.55 | | | |
| | I _{OL} = 32 mA | 4.5 V | 0.55 | | | 0.55 | | | |
| I _I | V _I = 5.5 V or GND | 0 to 5.5 V | ±1 | | | ±2 | | | μA |
| I _{off} | V _I or V _O = 5.5 V | 0 | ±10 | | | ±10 | | | μA |
| I _{CC} | V _I = 5.5 V or GND, I _O = 0 | 1.65 V to 5.5 V | 1 | | | 10 | | | μA |
| ΔI _{CC} | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 3 V to 5.5 V | 500 | | | 500 | | | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | 3.5 | | | | | | pF |

 (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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7.6 Switching Characteristics, $C_L = 15\text{ pF}$

over recommended operating free-air temperature range, $C_L = 15\text{ pF}$ (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C to 85°C | | | | | | | | UNIT |
|-----------|--------------|-------------|---|-----|--|-----|--|-----|--|-----|------|
| | | | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | Y | 2 | 9.9 | 1.5 | 6 | 1 | 3.5 | 1 | 2.9 | ns |

7.7 Switching Characteristics, -40°C to 85°C

over recommended operating free-air temperature range, $C_L = 30\text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C to 85°C | | | | | | | | UNIT |
|-----------|--------------|-------------|---|-----|--|-----|--|-----|--|-----|------|
| | | | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | Y | 3.2 | 8.6 | 1.5 | 4.4 | 1.5 | 4.1 | 1 | 3.2 | ns |

7.8 Switching Characteristics, -40°C to 125°C

over recommended operating free-air temperature range, $C_L = 30\text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 4)

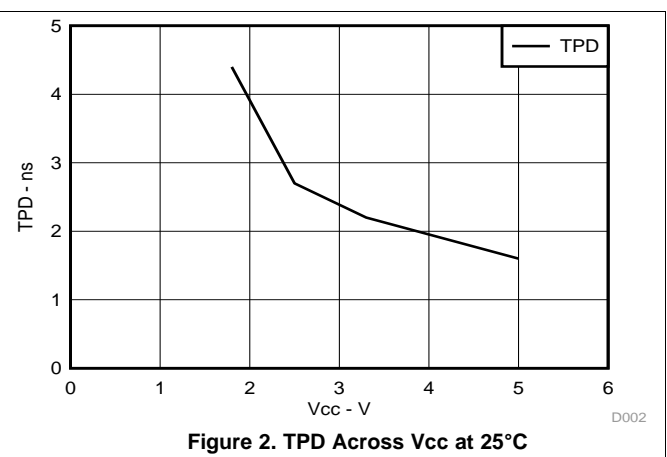
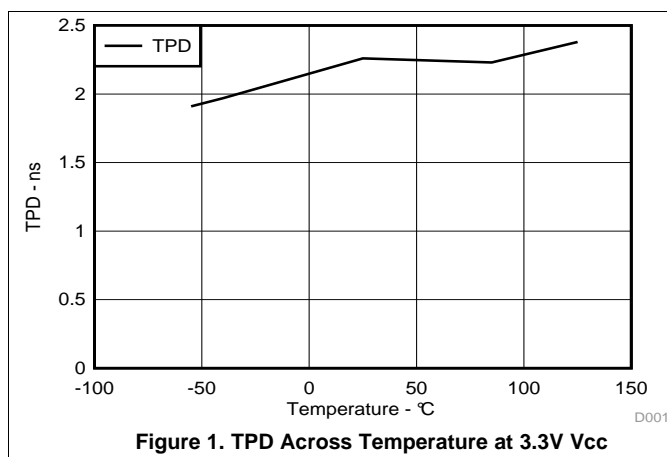
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C to 125°C | | | | | | | | UNIT |
|-----------|--------------|-------------|---|-----|--|-----|--|-----|--|-----|------|
| | | | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | Y | 3.2 | 9.5 | 1.5 | 5.1 | 1.5 | 4.7 | 1 | 3.9 | ns |

7.9 Operating Characteristics

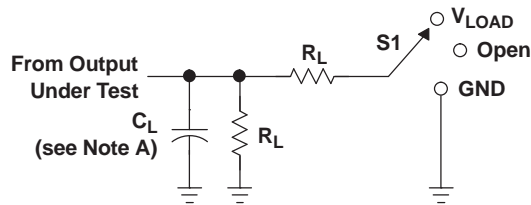
$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|--|---------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
| | | TYP | TYP | TYP | TYP | |
| C_{pd} Power dissipation capacitance | $f = 10\text{ MHz}$ | 16 | 16 | 16 | 18 | pF |

7.10 Typical Characteristics



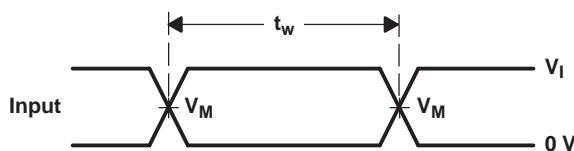
8 Parameter Measurement Information



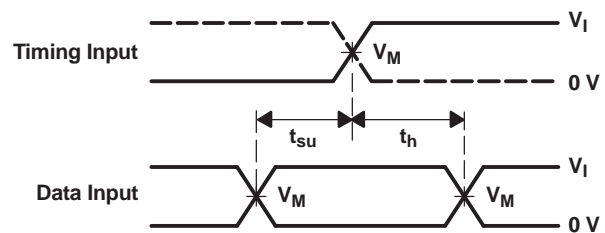
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

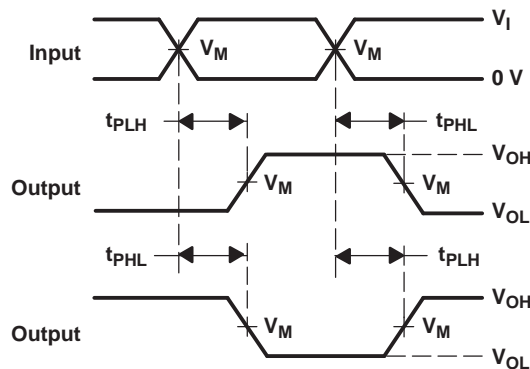
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 1 M Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.3 V |



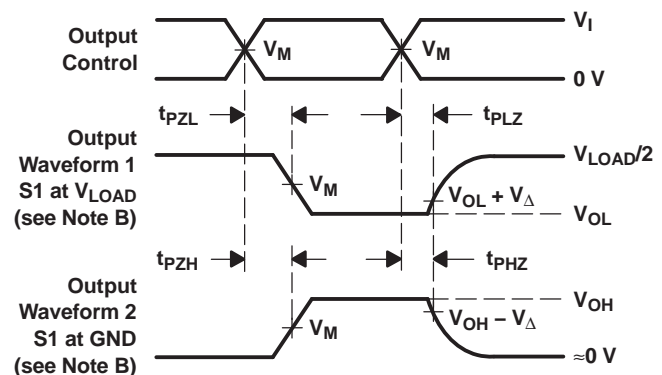
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

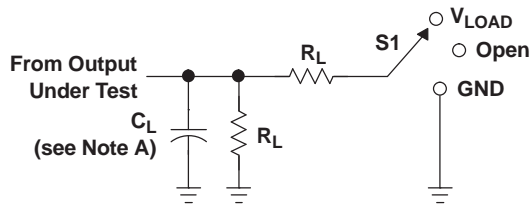


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

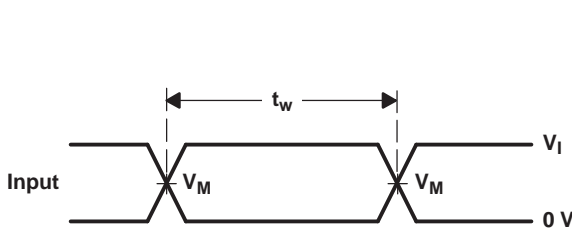
Parameter Measurement Information (continued)



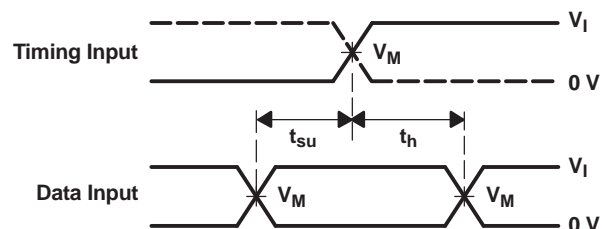
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

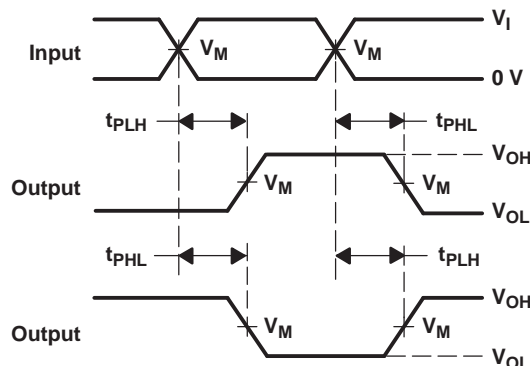
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



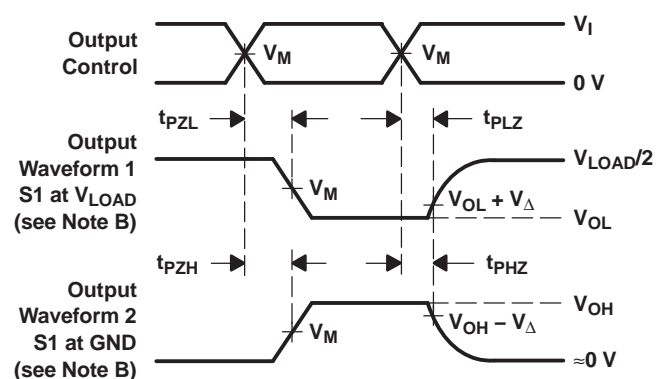
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74LVC1G34 device contains one buffer gate device and performs the Boolean function $Y = A$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

9.2 Functional Block Diagram



9.3 Feature Description

- Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V.

9.4 Device Functional Modes

Function Table

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

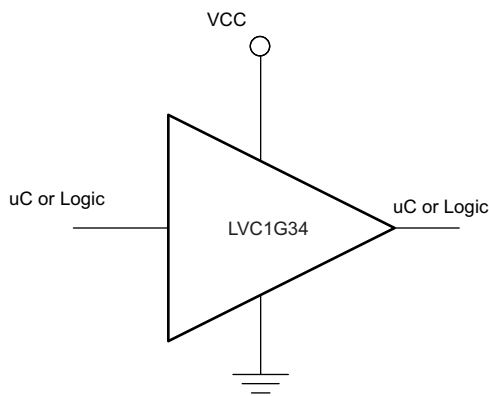
10 Application and Implementation

10.1 Application Information

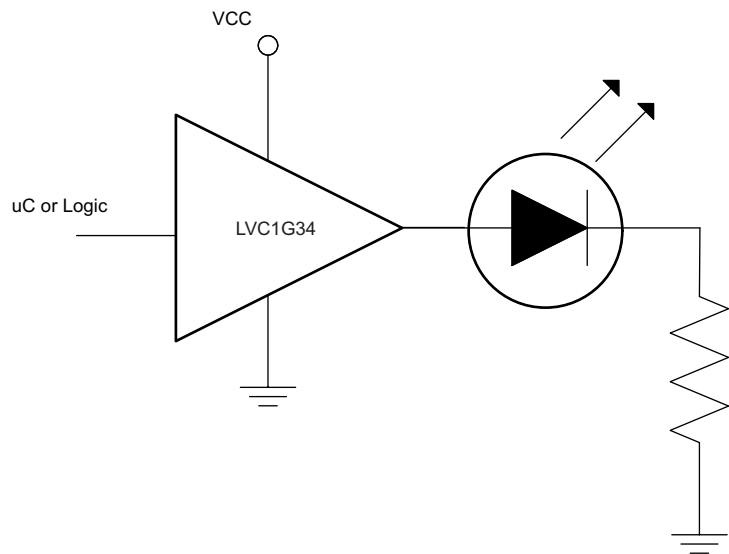
The SN74LVC1G34 is a high drive CMOS device that can be used as a buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC} .

10.2 Typical Application

Buffer Function



Basic LED Driver



10.2.1 Design Requirements

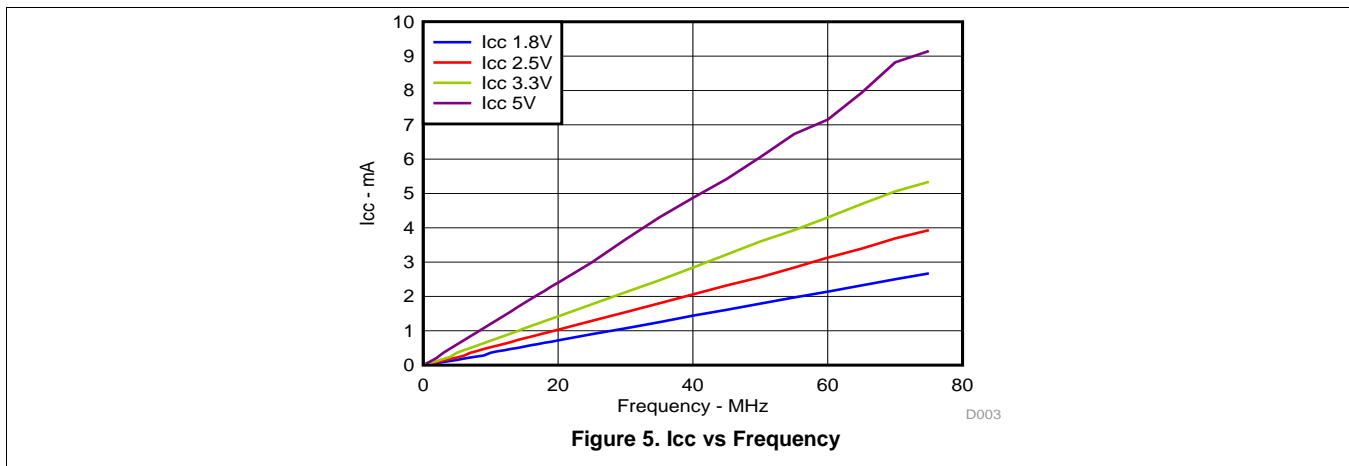
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs. See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as $(VI \text{ max})$ in the [Recommended Operating Conditions](#) table at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents should not exceed $(I_O \text{ max})$ per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Absolute Max Ratings](#) table.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

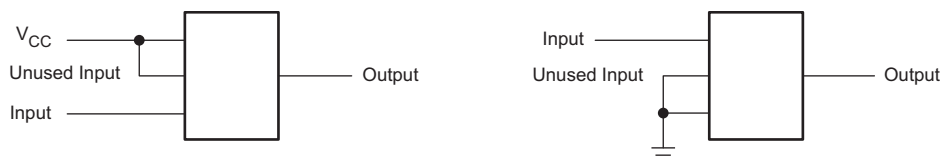
Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1- μ F capacitor is recommended and if there are multiple V_{CC} pins then a 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to Gnd or V_{CC} whichever make more sense or is more convenient.

12.2 Layout Example



13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| SN74LVC1G34DBVR | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU SN NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C345, C34F, C34J, C34K, C34R) (C34H, C34P, C34S) |
| SN74LVC1G34DBVR.Z | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C345, C34F, C34J, C34K, C34R) (C34H, C34P, C34S) |
| SN74LVC1G34DBVRE4 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |
| SN74LVC1G34DBVRG4 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |
| SN74LVC1G34DBVRG4.Z | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |
| SN74LVC1G34DBVT | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU SN NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C345, C34J, C34K, C34R) (C34H, C34S) |
| SN74LVC1G34DBVT.Z | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C345, C34J, C34K, C34R) (C34H, C34S) |
| SN74LVC1G34DBVTE4 | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |
| SN74LVC1G34DBVTG4 | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |
| SN74LVC1G34DBVTG4.Z | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |
| SN74LVC1G34DCKR | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU SN NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C95, C9F, C9J, C9 R) (C9H, C9P, C9S) |
| SN74LVC1G34DCKR.Z | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (C95, C9F, C9J, C9 R) (C9H, C9P, C9S) |
| SN74LVC1G34DCKRE4 | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C95 C9S |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| SN74LVC1G34DCKRG4 | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C95 C9S |
| SN74LVC1G34DCKRG4.Z | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C95 C9S |
| SN74LVC1G34DCKT | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU SN NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C95, C9J, C9R) (C9H, C9S) |
| SN74LVC1G34DCKT.Z | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C95, C9J, C9R) (C9H, C9S) |
| SN74LVC1G34DCKTG4 | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C95 C9S |
| SN74LVC1G34DCKTG4.Z | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C95 C9S |
| SN74LVC1G34DPWR | Active | Production | X2SON (DPW) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | P4 |
| SN74LVC1G34DPWR.Z | Active | Production | X2SON (DPW) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | P4 |
| SN74LVC1G34DRLR | Active | Production | SOT-5X3 (DRL) 5 | 4000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (C97, C9R) |
| SN74LVC1G34DRLR.Z | Active | Production | SOT-5X3 (DRL) 5 | 4000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (C97, C9R) |
| SN74LVC1G34DRYR | Active | Production | SON (DRY) 6 | 5000 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34DRYR.Z | Active | Production | SON (DRY) 6 | 5000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34DRYRG4.Z | Active | Production | SON (DRY) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34DSFR | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34DSFR.Z | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34DSFRG4.Z | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34YFPR | Active | Production | DSBGA (YFP) 4 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | C9 N |
| SN74LVC1G34YFPR.Z | Active | Production | DSBGA (YFP) 4 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | C9 N |
| SN74LVC1G34YZPR | Active | Production | DSBGA (YZP) 5 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | C9N |
| SN74LVC1G34YZPR.Z | Active | Production | DSBGA (YZP) 5 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | C9N |
| SN74LVC1G34YZVR | Active | Production | DSBGA (YZV) 4 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | C9 N |
| SN74LVC1G34YZVR.Z | Active | Production | DSBGA (YZV) 4 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | C9 N |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G34DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKRG4 | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKTG4 | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q3 |
| SN74LVC1G34DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G34DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G34YFPR | DSBGA | YFP | 4 | 3000 | 178.0 | 9.2 | 0.89 | 0.89 | 0.58 | 4.0 | 8.0 | Q1 |
| SN74LVC1G34YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |
| SN74LVC1G34YZVR | DSBGA | YZV | 4 | 3000 | 178.0 | 9.2 | 1.0 | 1.0 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G34DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G34DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G34DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DBVT | SOT-23 | DBV | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G34DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G34DCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DCKTG4 | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G34DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G34DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G34DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G34YFPR | DSBGA | YFP | 4 | 3000 | 220.0 | 220.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G34YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |
| SN74LVC1G34YZVR | DSBGA | YZV | 4 | 3000 | 220.0 | 220.0 | 35.0 |

GENERIC PACKAGE VIEW

DPW 5

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

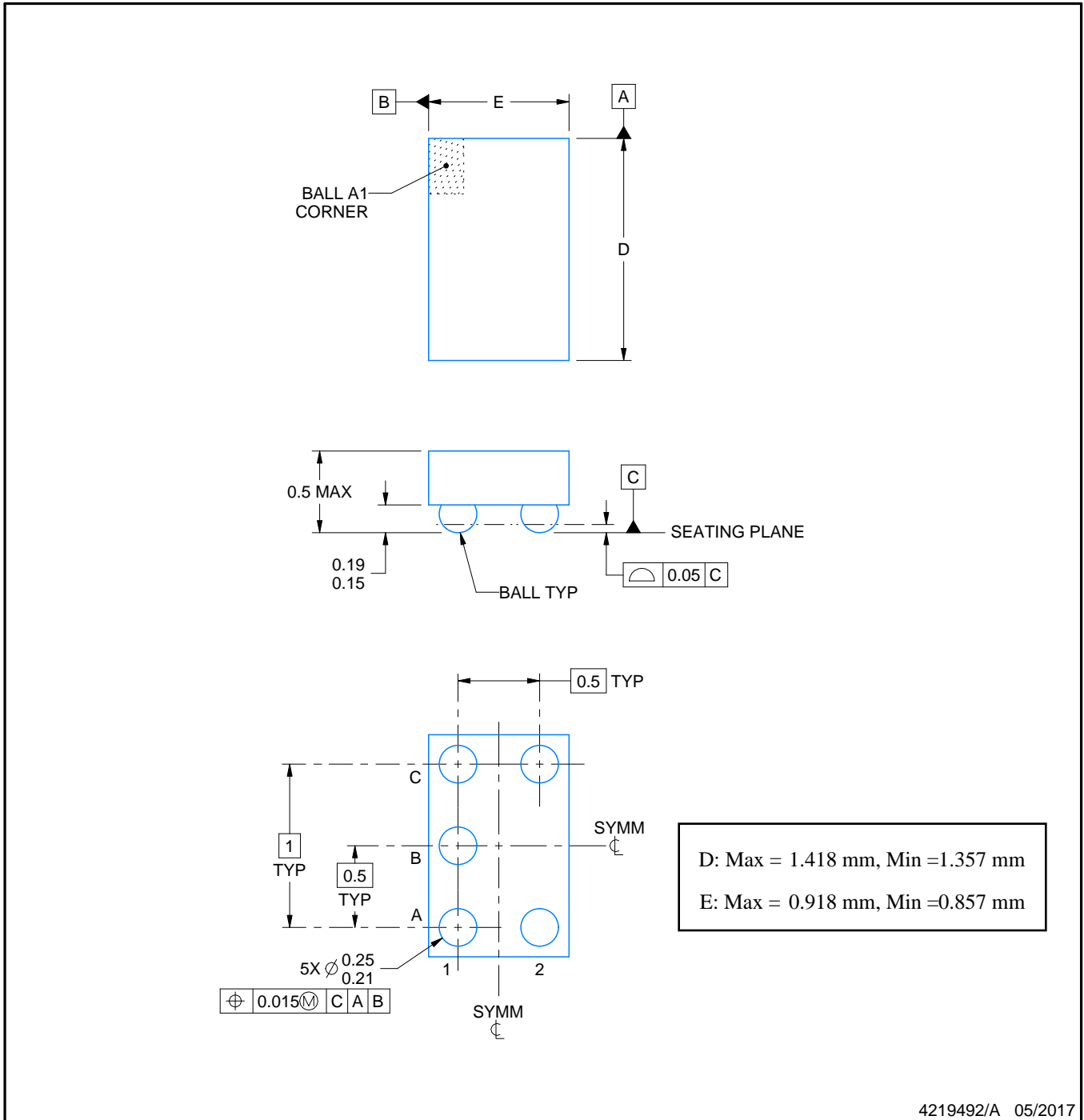
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

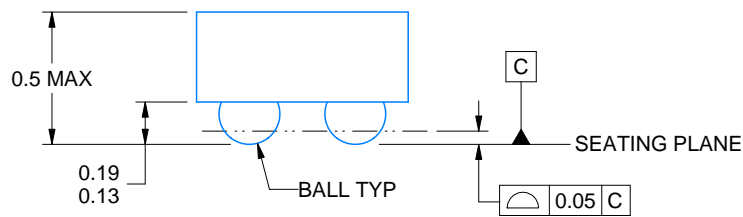
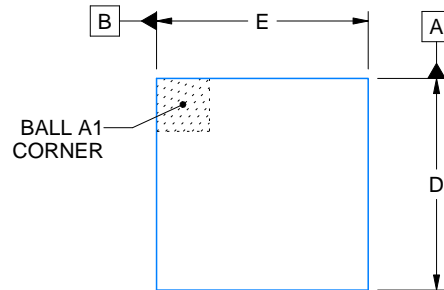
YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.



D: Max = 0.79 mm, Min = 0.73 mm
 E: Max = 0.79 mm, Min = 0.73 mm

4223507/A 01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

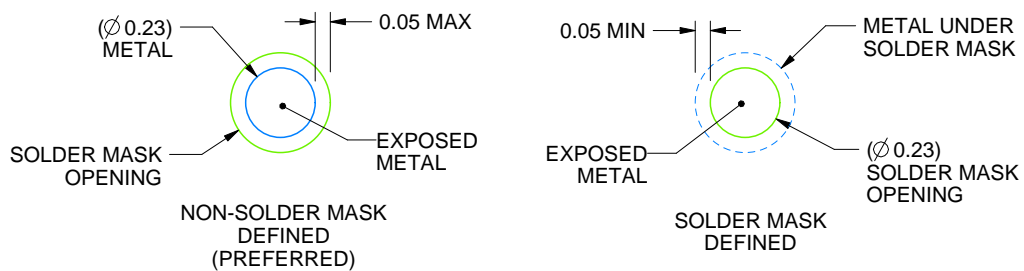
YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

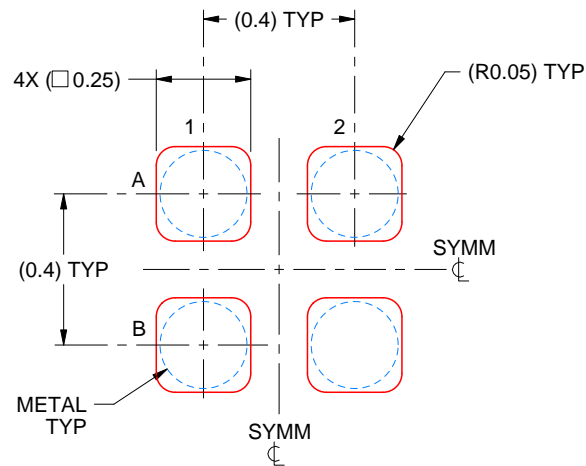
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A 01/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

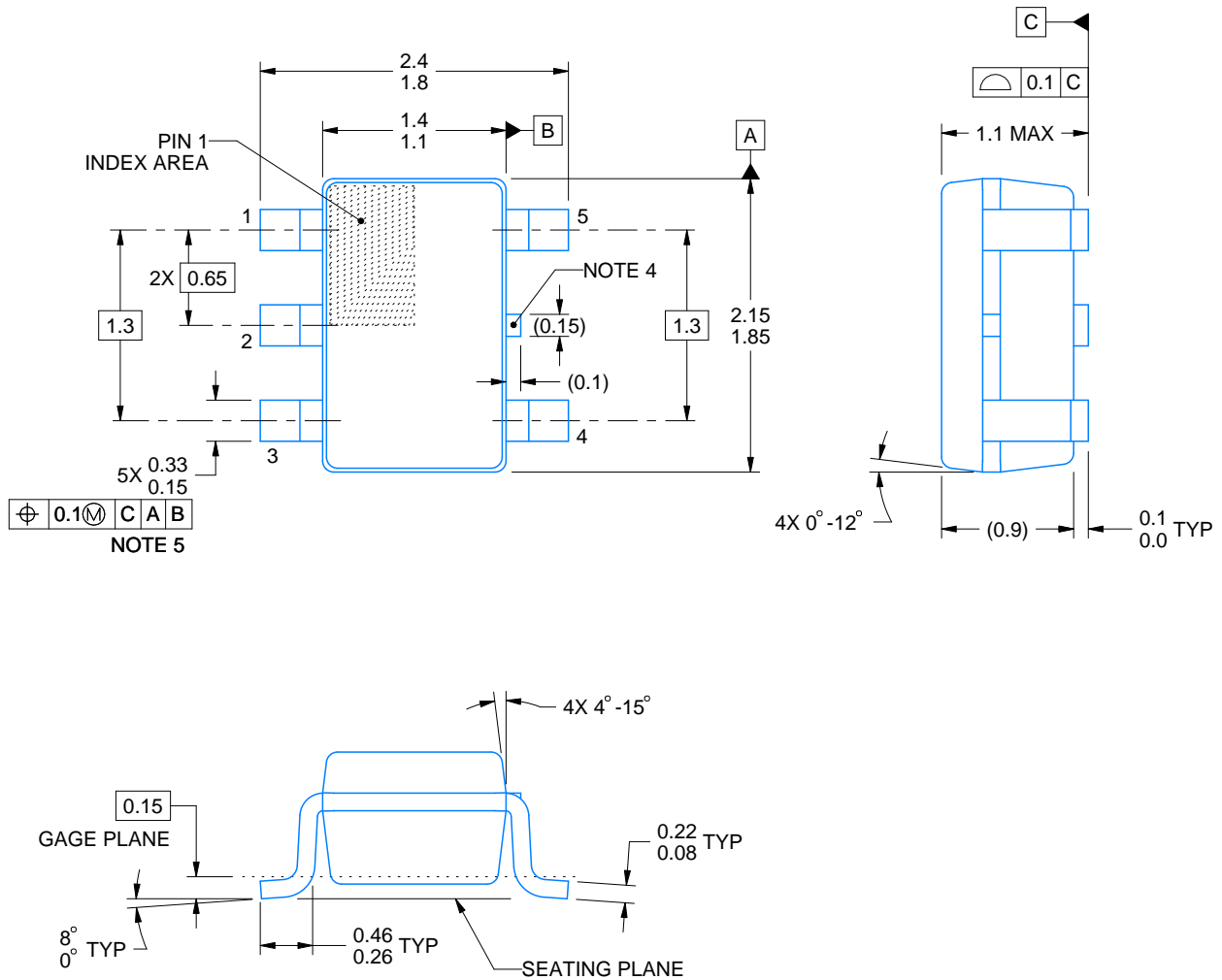
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

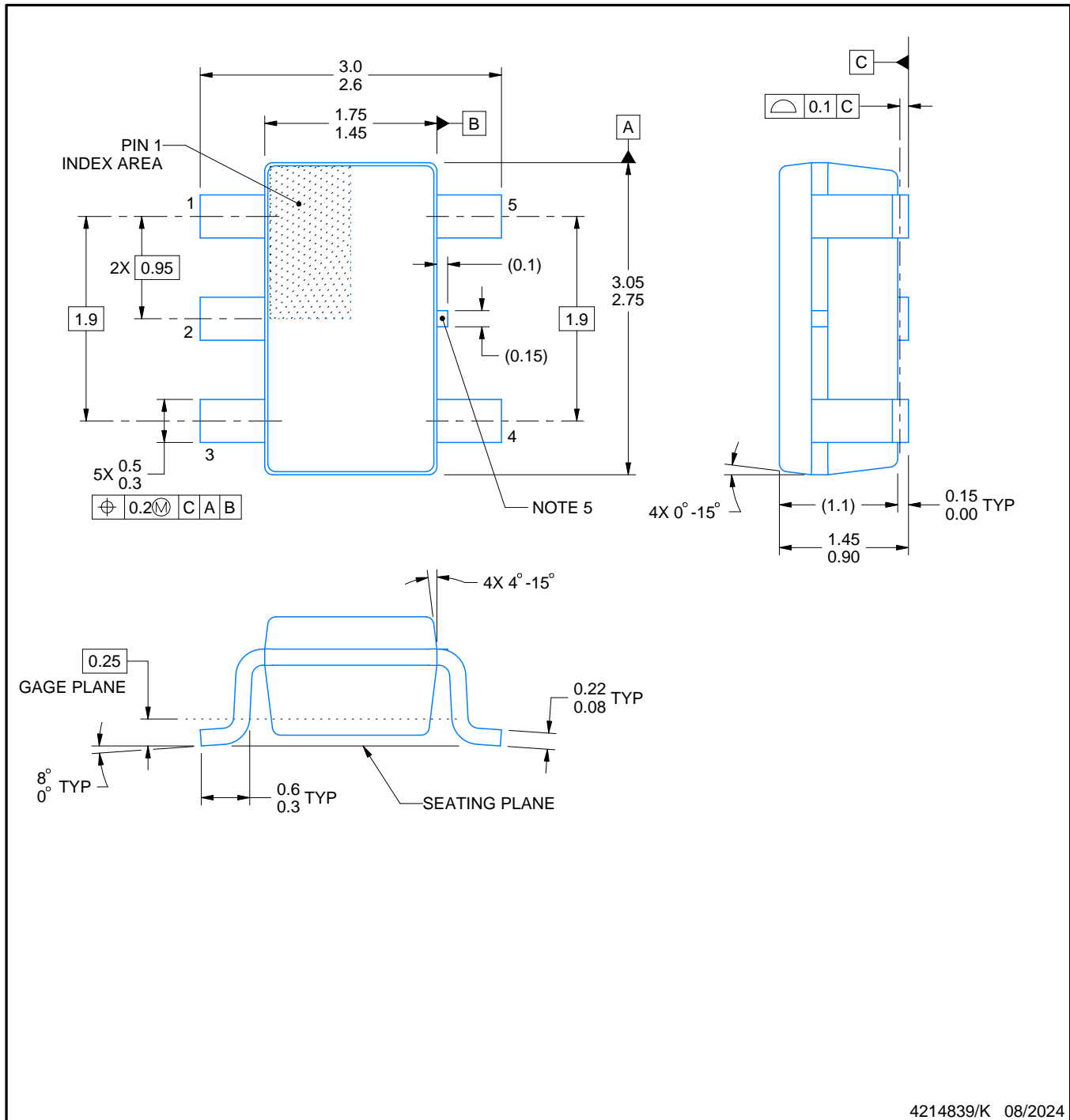
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Reference JEDEC MO-178.
- Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

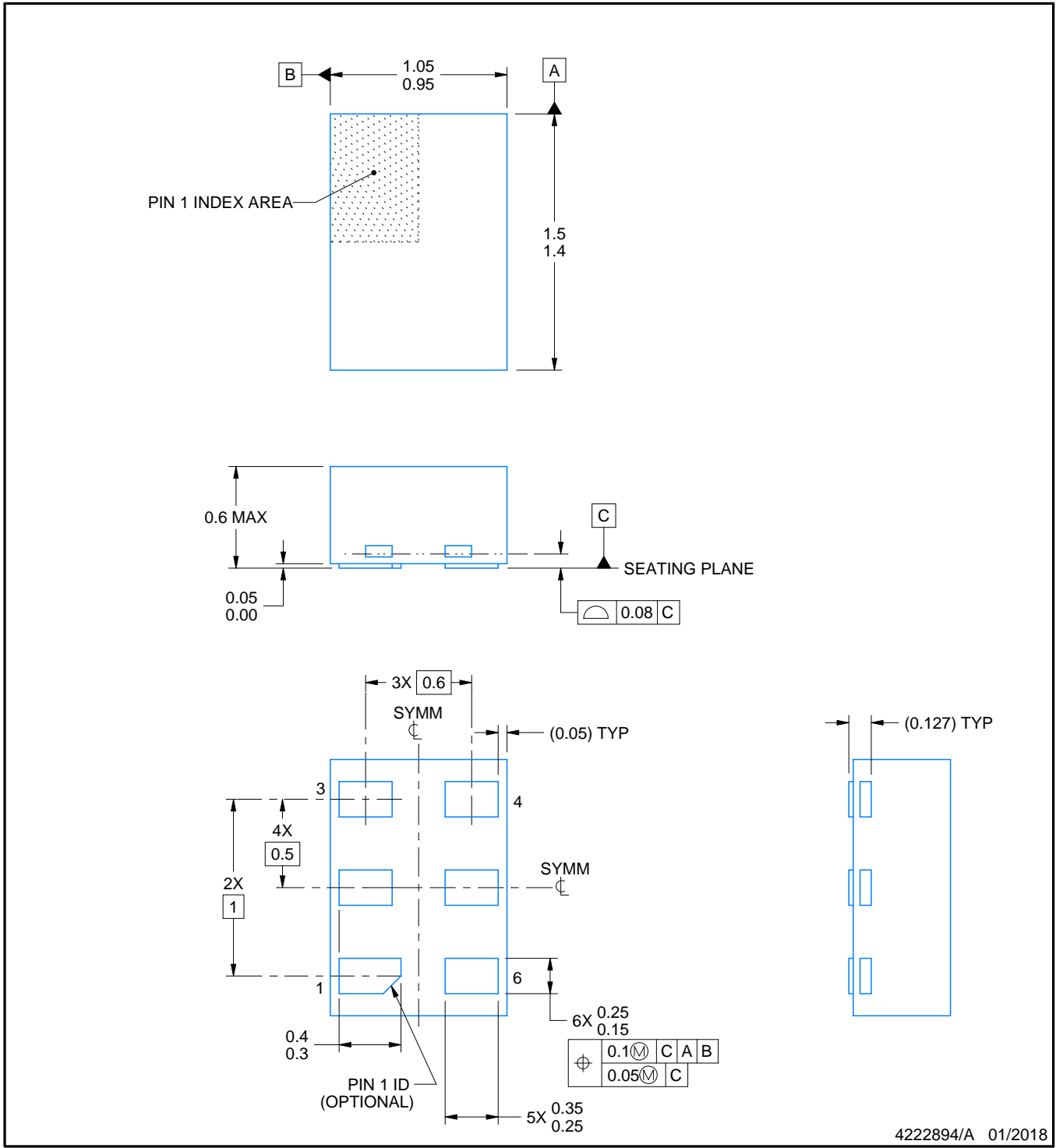
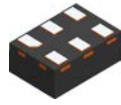
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G



4222894/A 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

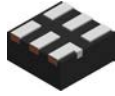


SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/B 06/2022

NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

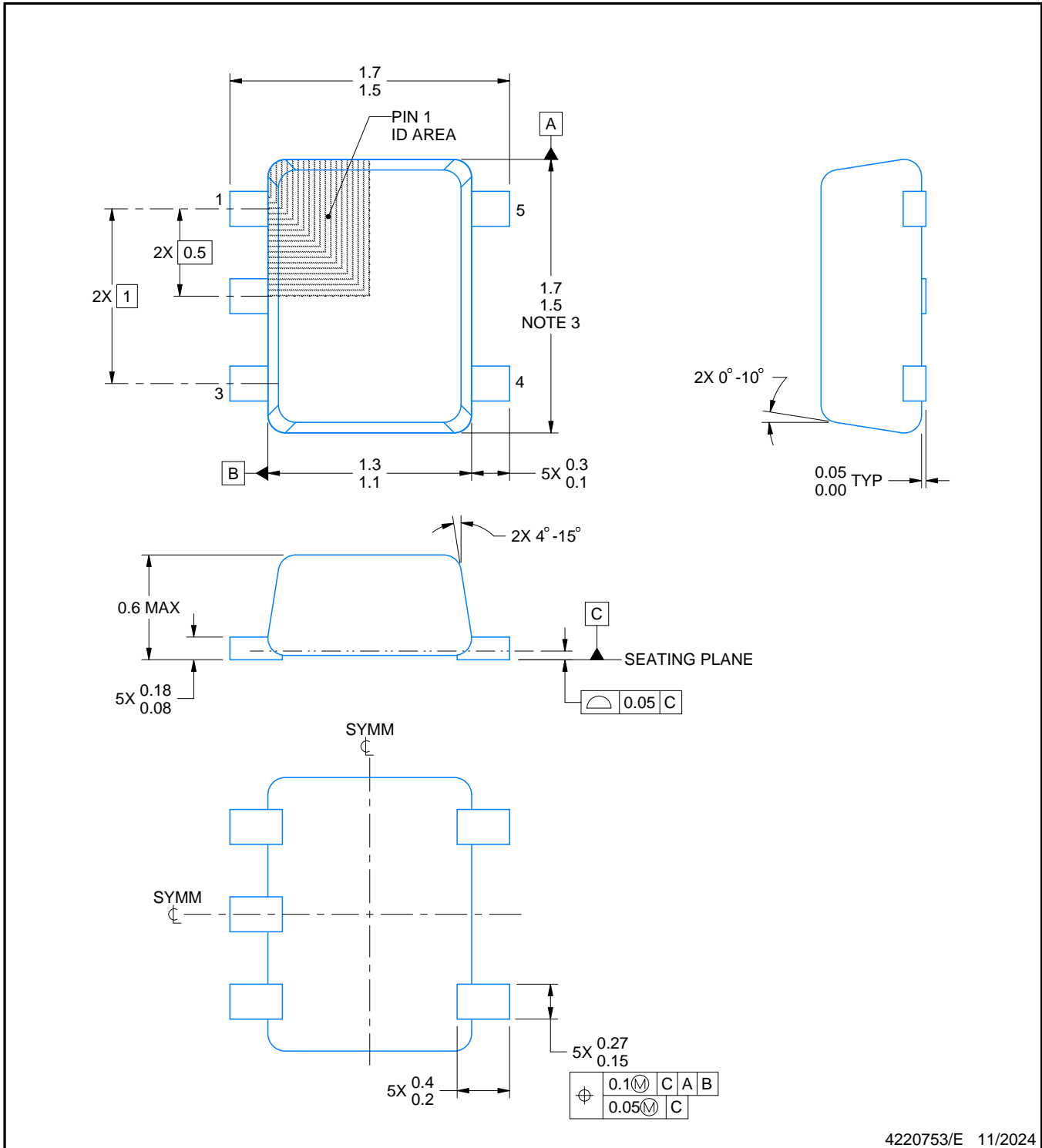
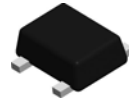


SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220753/E 11/2024

NOTES:

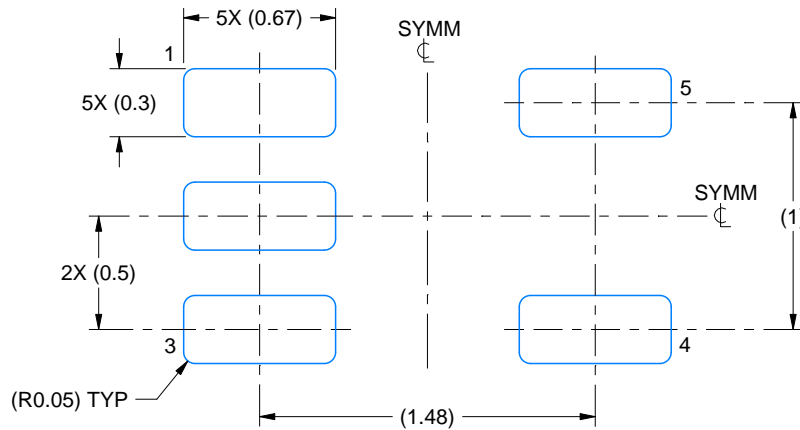
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

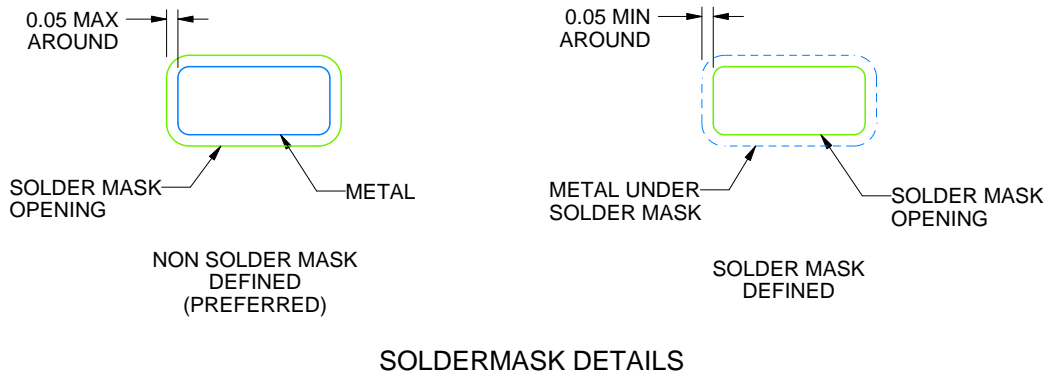
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

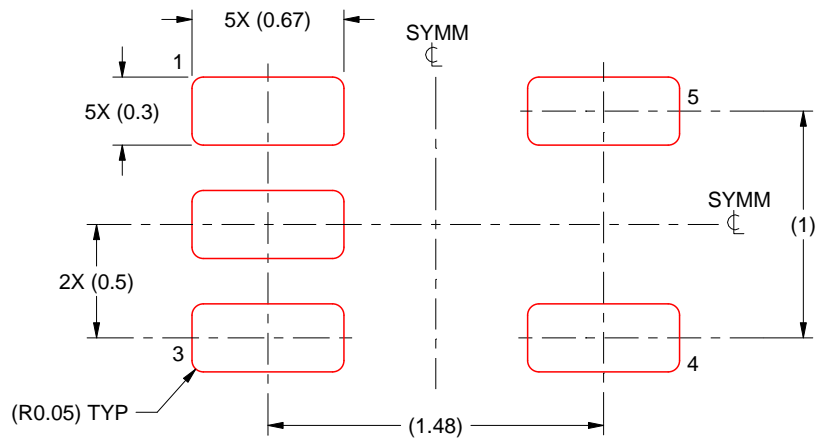
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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