

TS3A27518E-Q1 具有集成 IEC L-4 ESD 及 1.8V 逻辑兼容控制输入的 6 位、2 选 1 多路复用器或多路信号分离器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
 - 器件温度等级 2：-40°C 至 105°C 环境温度工作温度范围
 - 器件 HBM ESD 分类等级 H2
 - 器件 CDM ESD 分类等级 C3B
- 提供功能安全型
 - 有助于进行功能安全系统设计的文档
- 1.65V 至 3.6V 单电源运行
- 关断保护（在处于断电模式时提供隔离，在 $V_+ = 0$ 时处于高阻抗状态）
- 低电容开关，21.5pF（典型值）
- 可为高速轨到轨信号处理提供高达 240MHz 的带宽
- 串扰及断开隔离为 -62dB
- 用于控制输入的 1.8V 逻辑阈值兼容性
- 可耐受 3.6V 电压的控制输入
- ESD 性能：NC/NO 端口
 - ±6kV 接触放电 (IEC 61000-4-2)
- 24 引脚 TSSOP (7.80mm × 4.40mm) 和 24 引脚 QFN (4.00mm × 4.00mm) 封装

2 应用

- SD/SDIO 和 MMC 两端口多路复用器
- PC VGA 视频多路复用器/视频系统
- 音频和视频信号路由

3 说明

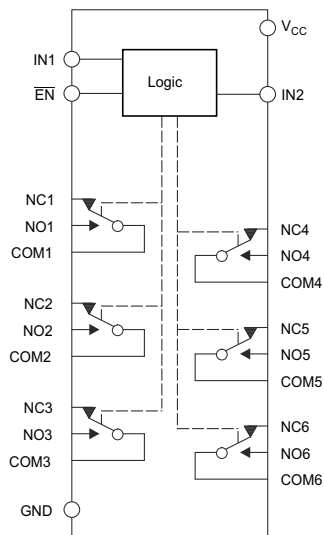
TS3A27518E-Q1 是一款 6 位、2 选 1 多路复用器/多路解复用器，其设计工作电压为 1.65V 至 3.6V。此器件可以处理数字信号和模拟信号，并允许向任意方向传输高达 V_+ 的信号。TS3A27518E-Q1 有两个控制引脚，每个引脚可同时控制三个 2 选 1 复用器，并且一个使能引脚可用于将所有输出置于高阻抗模式。这个控制引脚与 1.8V 逻辑阈值兼容并且也与 2.5V 和 3.3V 阈值向后兼容。

由于 SDIO 接口包含 6 位信号，即 CMD、CLK 和 Data[0:3] 信号，TS3A27518E-Q1 允许 SD、SDIO 和多媒体卡主机控制器扩展至多个卡或者外设。TS3A27518E-Q1 有两个控制引脚，这两个引脚可为用户提供附加灵活性，例如复用两个设备中不同的音视频信号（诸如 LCD 电视、LCD 监视器、或者笔记本扩展坞）的功能。

封装信息⁽¹⁾

器件型号	封装	封装尺寸（标称值）
TS3A27518E-Q1	RTW (WQFN, 24)	4.00mm × 4.00mm
	PW (TSSOP, 24)	7.80mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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功能方框图



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (January 2019) to Revision D (November 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 向特性部分添加了“提供功能安全”信息.....	1

Changes from Revision B (May 2012) to Revision C (January 2019)	Page
• 添加了器件信息表、ESD 等级表、建议运行条件表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1

Changes from Revision A (March 2012) to Revision B (May 2012)	Page
• 将器件的温度等级从 1 更改为 2，删除了最大耐受电压信息，将 C3B2 更改为 C3B.....	1
• 在订购信息表中添加了额外一行.....	1
• Changed $T_A = -40^{\circ}\text{C}$ to 85°C to $T_A = -40^{\circ}\text{C}$ to 105°C	5
• Changed Full to -40°C to 85°C and added extra row with 85°C to 105°C and limits -7.5 to 7.5.....	5
• Changed Full to -40°C to 85°C and added extra row with 85°C to 105°C with limits 68.....	5
• Changed Full to -40°C to 85°C and added extra row with 85°C to 105°C with limits 70.....	5
• Changed Full to -40°C to 85°C and added extra row with 85°C to 105°C with limits 5 μA	5
• Changed $T_A = -40^{\circ}\text{C}$ to 85°C to $T_A = -40^{\circ}\text{C}$ to 105°C	7
• Changed Full to -40°C to 85°C and added extra row with 85°C to 105°C with limits 38.4.....	7
• Changed Full to -40°C to 85°C and added extra row with 85°C to 105°C with limits 3.....	7
• Changed $T_A = -40^{\circ}\text{C}$ to 85°C to $T_A = -40^{\circ}\text{C}$ to 105°C	9
• Changed Full to -40°C to 85°C and added extra row with 85°C to 105°C and limits -5.8 to 5.8.....	9
• Changed Full to -40°C to 85°C and added extra row with 85°C to 105°C with limits 35.2.....	9
• Changed Full to -40°C to 85°C and added extra row with 85°C to 105°C with limits 2.5.....	9

5 Pin Configuration and Functions

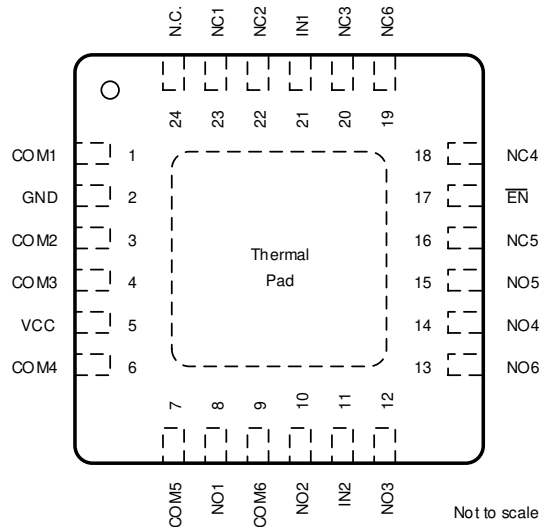


图 5-1. RTW Package, 24-Pin WQFN (Top View)

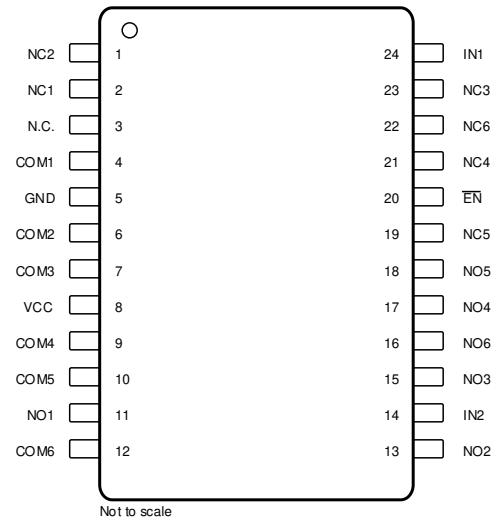


图 5-2. PW Package, 24-Pin TSSOP (Top View)

表 5-1. Pin Functions

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	RTW	PW		
COM1	1	4	I/O	Common-signal path
COM2	3	6	I/O	Common-signal path
COM3	4	7	I/O	Common-signal path
COM4	6	9	I/O	Common-signal path
COM5	7	10	I/O	Common-signal path
COM6	9	12	I/O	Common-signal path
EN	17	20	I	Digital control to enable or disable all signal paths
GND	2	5	—	Ground.
IN1	21	24	I	Digital control to connect COM to NC or NO
IN2	11	14	I	Digital control to connect COM to NC or NO
N.C.	24	3	—	Not connected
NC1	23	2	I/O	Normally closed-signal path
NC2	22	1	I/O	Normally closed-signal path
NC3	20	23	I/O	Normally closed-signal path
NC4	18	21	I/O	Normally closed-signal path
NC5	16	19	I/O	Normally closed-signal path
NC6	19	22	I/O	Normally closed-signal path
NO1	8	11	I/O	Normally open-signal path
NO2	10	13	I/O	Normally open-signal path
NO3	12	15	I/O	Normally open-signal path
NO4	14	17	I/O	Normally open-signal path
NO5	15	18	I/O	Normally open-signal path
NO6	13	16	I/O	Normally open-signal path
V _{CC}	5	8	—	Voltage supply

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_+	Supply voltage range ⁽²⁾	- 0.5	4.6	V
V_{NC} V_{NO} V_{COM}	Analog voltage range ^{(2) (3) (4)}	- 0.5	4.6	V
I_K	Analog port diode current ⁽⁵⁾	$V_+ < V_{NC}, V_{NO}, V_{COM} < 0$		mA
I_{NC} I_{NO} I_{COM}	ON-state switch current ⁽⁶⁾	$V_{NC}, V_{NO}, V_{COM} = 0 \text{ to } V_+$		mA
V_I	Digital input voltage range ^{(2) (3)}	- 0.5	4.6	V
I_{IK}	Digital input clamp current ^{(2) (3)}	$V_{IO} < V_I < 0$		mA
I_+	Continuous current through V_+		100	mA
I_{GND}	Continuous current through GND	- 100		mA
T_{stg}	Storage temperature range	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.
- (5) Requires clamp diodes on analog port to V_+ .
- (6) Pulse at 1-ms duration <10% duty cycle

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ AEC-Q100 Classification Level H2	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ AEC-Q100 Classification Level C3B	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process..
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	1.65	3.6	V
Analog signal voltage	V_{NC}	0	V_{CC}	V
	V_{NO}			
	V_{COM}			
Digital input voltage	V_I	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS3A27518E		UNIT
		PW (TSSOP)	RTW (WQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104	40.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.6	42.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	19.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.9	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.1	19.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics for 3.3-V Supply

$V_+ = 3\text{ V}$ to 3.6 V , $T_A = -40^\circ\text{C}$ to 105°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Analog Switch									
ON-state resistance	r _{on}	0 ≤ (V _{NC} or V _{NO}) ≤ V ₊ , I _{COM} = - 32 mA,	Switch ON, See 图 7-1	25°C	3 V	4.4	6.2	Ω	
				Full		7.6			
ON-state resistance match between channels	Δ r _{on}	V _{NC} or V _{NO} = 2.1 V, I _{COM} = - 32 mA,	Switch ON, See 图 7-1	25°C	3 V	0.3	0.7	Ω	
				Full		0.8			
ON-state resistance flatness	r _{on(flat)}	0 ≤ (V _{NC} or V _{NO}) ≤ V ₊ , I _{COM} = - 32 mA,	Switch ON, See 图 7-2	25°C	3 V	0.95	2.1	Ω	
				Full		2.3			
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 1 V, V _{COM} = 3 V, or V _{NC} or V _{NO} = 3 V, V _{COM} = 1 V,	Switch OFF, See 图 7-2	25°C	3.6 V	- 0.5	0.05	0.5	μ A
				Full		- 7	7		
	I _{NC(PWROFF)} , I _{NO(PWROFF)}	V _{NC} or V _{NO} = 0 to 3.6 V, V _{COM} = 3.6 V to 0, or V _{NC} or V _{NO} = 3.6 V to 0, V _{COM} = 0 to 3.6 V,		25°C	0 V	- 1	0.05	1	
				Full		- 12	12		
COM OFF leakage current	I _{COM(OFF)}	V _{NC} or V _{NO} = 3 V, V _{COM} = 1 V, or V _{NC} or V _{NO} = 1 V, V _{COM} = 3 V,	Switch OFF, See 图 7-2	25°C	3.6 V	- 1	0.01	1	μ A
				Full		- 2	2		
	I _{COM(PWROFF)}	V _{NC} or V _{NO} = 3.6 V to 0, V _{COM} = 0 to 3.6 V, or V _{NC} or V _{NO} = 0 to 3.6 V, V _{COM} = 3.6 V to 0,		25°C	0 V	- 1	0.02	1	
				Full		- 12	12		
NC, NO ON leakage current	I _{NO(ON)} , I _{NC(ON)}	V _{NC} or V _{NO} = 1 V, V _{COM} = Open, or V _{NC} or V _{NO} = 3 V, V _{COM} = Open,	Switch ON, See 图 7-3	25°C	3.6 V	- 2.5	0.04	2.2	μ A
				- 40°C to 85°C		- 7	7		
				85°C to 105°C		- 7.5	7.5		
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 1 V, or V _{NC} or V _{NO} = Open, V _{COM} = 3 V,	Switch ON, See 图 7-3	25°C	3.6 V	- 2	0.03	2	μ A
				Full		- 7	7		
Digital Control Inputs (IN1, IN2, EN) ⁽¹⁾									
Input logic high	V _{IH}			Full	3.6 V	1.2		3.6	V
Input logic low	V _{IL}			Full	3.6 V	0		0.65	V

6.5 Electrical Characteristics for 3.3-V Supply (continued)

$V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }105^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Input leakage current	I _{IH} , I _{IL}	V _I = V ₊ or 0		25°C	3.6 V	- 0.1	0.05	0.1	μ A
				Full		- 2.5		2.5	
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω, C _L = 35 pF, See 图 7-5	25°C	3.3 V	18.1		59	ns	
			- 40°C to 85°C	3 V to 3.6 V			60		
			85°C to 105°C				68		
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω, C _L = 35 pF, See 图 7-5	25°C	3.3 V	25.4		60.6	ns	
			- 40°C to 85°C	3 V to 3.6 V			61		
			85°C to 105°C				70		
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω, C _L = 35 pF, See 图 7-6	25°C	3.3 V	4	11.1	22.7	ns	
			Full	3 V to 3.6 V			28		
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0, C _L = 0.1 nF, See 图 7-10	25°C	3.3 V	0.81			pC	
NC, NO OFF capacitance	C _{NC(OFF)} , C _{NO(OFF)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF, See 图 7-4	25°C	3.3 V	13			pF	
COM OFF capacitance	C _{COM(OFF)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF, See 图 7-4		3.3 V	8.5			pF	
NC, NO ON capacitance	C _{NC(ON)} , C _{NO(ON)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF, See 图 7-4	25°C	3.3 V	21.5			pF	
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON, See 图 7-4	25°C	3.3 V	21.5			pF	
Digital input capacitance	C _I	V _I = V ₊ or GND See 图 7-4	25°C	3.3 V	2			pF	
Bandwidth	BW	R _L = 50 Ω, Switch ON, See 图 7-6	25°C	3.3 V	240			MHz	
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 10 MHz, Switch OFF, See 图 7-8	25°C	3.3 V	- 62			dB	
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 10 MHz, Switch ON, See 图 7-9	25°C	3.3 V	- 62			dB	
Crosstalk adjacent	X _{TALK(ADJ)}	R _L = 50 Ω, f = 10 MHz, Switch ON, See 图 7-9	25°C	3.3 V	- 71			dB	
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF, f = 20 Hz to 20 kHz, See 图 7-11	25°C	3.3 V	0.05			%	
Supply									
Positive supply current	I ₊	V _I = V ₊ or GND, Switch ON or OFF	25°C	3.6 V	0.04		0.3	μ A	
			- 40°C to 85°C				3		
			85°C to 105°C				5		

- (1) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.6 Electrical Characteristics for 2.5-V Supply

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 105^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Analog Switch									
ON-state resistance	r _{on}	0 ≤ (V _{NC} or V _{NO}) ≤ V ₊ , I _{COM} = - 32 mA,	Switch ON, See 图 7-1	25°C	2.3 V	5.5		9.6	Ω
				Full					
ON-state resistance match between channels	Δ r _{on}	V _{NC} or V _{NO} = 1.6 V, I _{COM} = - 32 mA,	Switch ON, See 图 7-1	25°C	2.3 V	0.3		0.8	Ω
				Full					
ON-state resistance flatness	r _{on(flat)}	0 ≤ (V _{NC} or V _{NO}) ≤ V ₊ , I _{COM} = - 32 mA,	Switch ON, See 图 7-2	25°C	2.3 V	0.91		2.2	Ω
				Full					
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 0.5 V, V _{COM} = 2.3 V, or V _{NC} or V _{NO} = 2.3 V, V _{COM} = 0.5 V,	Switch OFF, See 图 7-2	25°C	2.7 V	- 0.3	0.04	0.3	μ A
		Full				- 6		6	
	I _{NC(PWROFF)} , I _{NO(PWROFF)}	V _{NC} or V _{NO} = 0 to 2.7 V, V _{COM} = 2.7 V to 0, or V _{NC} or V _{NO} = 2.7 V to 0, V _{COM} = 0 to 2.7 V,		25°C	0 V	- 0.6	0.02	0.6	
		Full				- 10		10	
COM OFF leakage current	I _{COM(OFF)}	V _{NC} or V _{NO} = 0.5 V, V _{COM} = 2.3 V, or V _{NC} or V _{NO} = 2.3 V, V _{COM} = 0.5 V,	Switch OFF, See 图 7-2	25°C	2.7 V	- 0.7	0.02	0.7	μ A
		Full				- 1		1	
	I _{COM(PWROFF)}	V _{NC} or V _{NO} = 2.7 V to 0, V _{COM} = 0 to 2.7 V, or V _{NC} or V _{NO} = 0 to 2.7 V, V _{COM} = 2.7 V to 0,		25°C	0 V	- 0.7	0.02	0.7	
		Full				- 7.2		7.2	
NC, NO ON leakage current	I _{NO(ON)} , I _{NC(ON)}	V _{NC} or V _{NO} = 0.5 V or 2.3 V, V _{COM} = Open,	Switch ON, See 图 7-3	25°C	2.7 V	- 2.1	0.03	2.1	μ A
		Full				- 6		6	
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 0.5 V, or V _{NC} or V _{NO} = Open, V _{COM} = 2.3 V,	Switch ON, See 图 7-3	25°C	2.7 V	- 2	0.02	2	μ A
				Full			- 5.7		
Digital Control Inputs (IN1, IN2, EN) ⁽¹⁾									
Input logic high	V _{IH}	V _I = V ₊ or GND		Full	2.7 V	1.15		3.6	V
Input logic low	V _{IL}			Full	2.7 V	0		0.55	V
Input leakage current	I _{IH} , I _{IL}	V _I = V ₊ or 0		25°C	2.7 V	-0.1	0.01	0.1	μ A
				Full			- 2.1		
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See 图 7-5	25°C	2.5 V	17.2		36.8	ns
				Full	2.3 V to 2.7 V			42.5	
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See 图 7-5	25°C	2.5 V	17.1		29.8	ns
				- 40°C to 85°C	2.3 V to 2.7 V			34.4	
				85°C to 105°C				38.4	
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω,	C _L = 35 pF, See 图 7-6	25°C	2.5 V	4.5	13	30	ns
				Full	2.3 V to 2.7 V			33.3	
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0,	C _L = 0.1 nF, See 图 7-10	25°C	2.5 V		0.47		pC
NC, NO OFF capacitance	C _{NC(OFF)} , C _{NO(OFF)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF,	See 图 7-4	25°C	2.5 V		13.5		pF
COM OFF capacitance	C _{COM(OFF)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF,	See 图 7-4		2.5 V		9		pF

6.6 Electrical Characteristics for 2.5-V Supply (continued)

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 105^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
NC, NO ON capacitance	C _{NC(ON),} C _{NO(ON)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF,	See 图 7-4	25°C	2.5 V		22		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See 图 7-4	25°C	2.5 V		22		pF
Digital input capacitance	C _I	V _I = V ₊ or GND	See 图 7-4	25°C	2.5 V		2		pF
Bandwidth	BW	R _L = 50 Ω,	Switch ON, See 图 7-6	25°C	2.5 V		240		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 10 MHz,	Switch OFF, See 图 7-8	25°C	2.5 V		– 62		dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 10 MHz,	Switch ON, See 图 7-9	25°C	2.5 V		– 62		dB
Crosstalk adjacent	X _{TALK(ADJ)}	R _L = 50 Ω, f = 10 MHz,	Switch ON, See 图 7-9	25°C	2.5 V		– 71		dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 20 Hz to 20 kHz, See 图 7-11	25°C	2.5 V		0.06		%
Supply									
Positive supply current	I ₊	V _I = V ₊ or GND,	Switch ON or OFF	25°C	2.7 V	0.01		0.1	μ A
						2			
						3			

- (1) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.7 Electrical Characteristics for 1.8-V Supply

$V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }105^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Analog Switch									
ON-state resistance	r _{on}	0 ≤ (V _{NC} or V _{NO}) ≤ V ₊ , I _{COM} = − 32 mA, Switch ON, See 图 7-1	25°C	1.65 V	7.1	14.4	Ω		
			Full		16.3				
ON-state resistance match between channels	Δ r _{on}	V _{NC} or V _{NO} = 1.5 V, I _{COM} = − 32 mA, Switch ON, See 图 7-1	25°C	1.65 V	0.3	1	Ω		
			Full		1.2				
ON-state resistance flatness	r _{on(flat)}	0 ≤ (V _{NC} or V _{NO}) ≤ V ₊ , I _{COM} = − 32 mA, Switch ON, See 图 7-2	25°C	1.65 V	2.7	5.5	Ω		
			Full		7.3				
NC, NO OFF leakage current	I _{NC(OFF)} , I _{NO(OFF)}	V _{NC} or V _{NO} = 0.3 V, V _{COM} = 1.65 V, or V _{NC} or V _{NO} = 1.65 V, V _{COM} = 0.3 V Switch OFF, See 图 7-2	25°C	1.95 V	− 0.25	0.03	0.25	μ A	
			Full		− 5 5				
	I _{NC(PWROFF)} , I _{NO(PWROFF)}	V _{NC} or V _{NO} = 1.95 V to 0, V _{COM} = 0 to 1.95 V, or V _{NC} or V _{NO} = 0 to 1.95 V, V _{COM} = 1.95 V to 0,	25°C	0 V	− 0.4	0.01	0.4	μ A	
			Full		− 7.2 7.2				
COM OFF leakage current	I _{COM(OFF)} , I _{COM(OFF)}	V _{NC} or V _{NO} = 0.3 V, V _{COM} = 1.65 V, or V _{NC} or V _{NO} = 1.65 V, V _{COM} = 0.3 V Switch OFF, See 图 7-2	25°C	1.95 V	− 0.4	0.02	0.4	μ A	
			Full		− 0.9 0.9				
	I _{COM(PWROFF)} , I _{COM(PWROFF)}	V _{NC} or V _{NO} = 1.95 V to 0, V _{COM} = 0 to 1.95 V, or V _{NC} or V _{NO} = 0 to 1.95 V, V _{COM} = 1.95 V to 0,	25°C	0 V	− 0.4	0.02	0.4	μ A	
			− 40°C to 85°C		− 5 5				
85°C to 105°C	− 5.8 5.8								
NC, NO ON leakage current	I _{NO(ON)} , I _{NC(ON)}	V _{NC} or V _{NO} = 0.3 V, V _{COM} = Open, or V _{NC} or V _{NO} = 1.65 V, V _{COM} = Open, Switch ON, See 图 7-3	25°C	1.95 V	− 2	0.02	2	μ A	
			Full		− 5.2 5.2				
COM ON leakage current	I _{COM(ON)}	V _{NC} or V _{NO} = Open, V _{COM} = 0.3 V, or V _{NC} or V _{NO} = Open, V _{COM} = 1.65 V, Switch ON, See 图 7-3	25°C	1.95 V	− 2	0.02	2	μ A	
			Full		− 5.2 5.2				
Digital Control Inputs (IN1, IN2, EN) ⁽¹⁾									
Input logic high	V _{IH}	V _I = V ₊ or GND	Full	1.95 V	1			3.6	V
Input logic low	V _{IL}		Full	1.95 V	0			0.4	V
Input leakage current	I _{IH} , I _{IL}	V _I = V ₊ or 0	25°C	1.95 V	−0.1	0.01	0.1	μ A	
			Full		−2.1 2.1				
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω, C _L = 35 pF, See 图 7-5	25°C	1.8 V	14.1		49.3	ns	
			Full	1.65 V to 1.95 V			56.7		
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω, C _L = 35 pF, See 图 7-5	25°C	1.8 V	16.1		26.5	ns	
			− 40°C to 85°C	1.65 V to 1.95 V			31.2		
			85°C to 105°C				35.2		
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ /2, R _L = 50 Ω, C _L = 35 pF, See 图 7-6	25°C	1.8 V	5.3	18.4	58	ns	
			Full	1.65 V to 1.95 V			58		
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0, C _L = 1 nF, See 图 7-10	25°C	1.8 V		0.21		pC	

6.7 Electrical Characteristics for 1.8-V Supply (continued)

$V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }105^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
NC, NO OFF capacitance	$C_{NC(OFF)},$ $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF, See Figure 7-4	25°C	1.8 V		9		pF
NC, NO ON capacitance	$C_{NC(ON)},$ $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON, See Figure 7-4	25°C	1.8 V		22		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 7-4	25°C	1.8 V		22		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND See Figure 7-4	25°C	1.8 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON, See Figure 7-6	25°C	1.8 V		240		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch OFF, See Figure 7-8	25°C	1.8 V		-60		dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch ON, See Figure 7-9	25°C	1.8 V		-60		dB
Crosstalk adjacent	$X_{TALK(ADJ)}$	$R_L = 50\ \Omega$, $f = 10\text{ MHz}$, Switch ON, See Figure 7-9	25°C	1.8 V		-71		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 7-11	25°C	1.8 V		0.1		%
Supply								
Positive supply current	I_+	$V_I = V_+$ or GND, Switch ON or OFF	25°C	1.95 V		0.01	0.1	μA
			-40°C to 85°C				1.5	
			85°C to 105°C				2.5	

- (1) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.8 Typical Characteristics

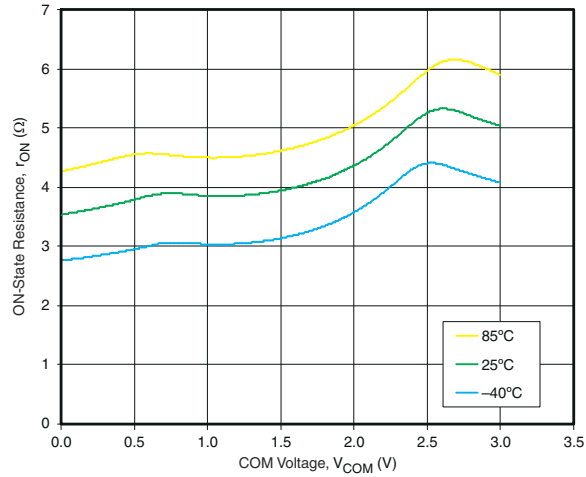


图 6-1. ON-State Resistance vs COM Voltage ($V_{CC} = 3\text{ V}$)

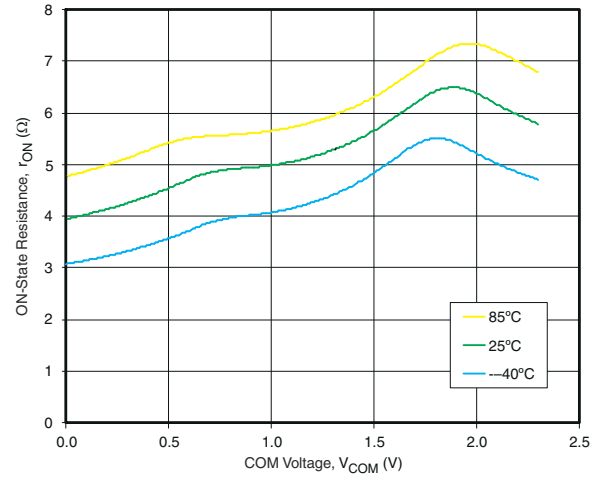


图 6-2. ON-State Resistance vs COM Voltage ($V_{CC} = 2.3\text{ V}$)

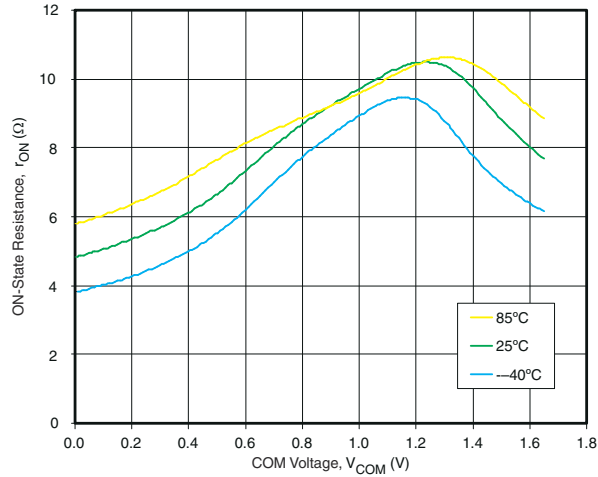


图 6-3. ON-State Resistance vs COM Voltage ($V_{CC} = 1.65\text{ V}$)

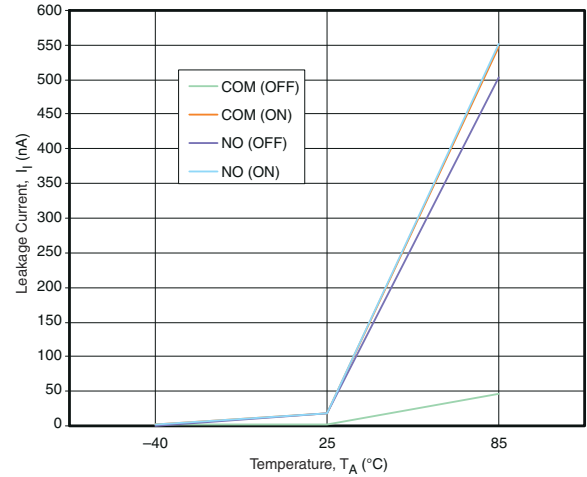


图 6-4. Leakage Current vs Temperature ($V_{CC} = 3.3\text{ V}$)

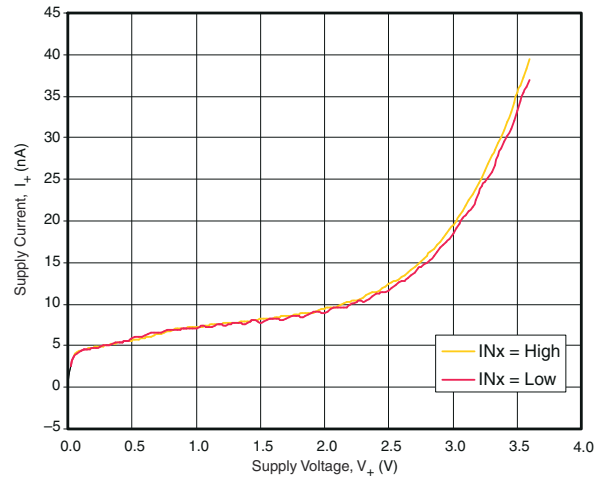


图 6-5. Supply Current vs Supply Voltage

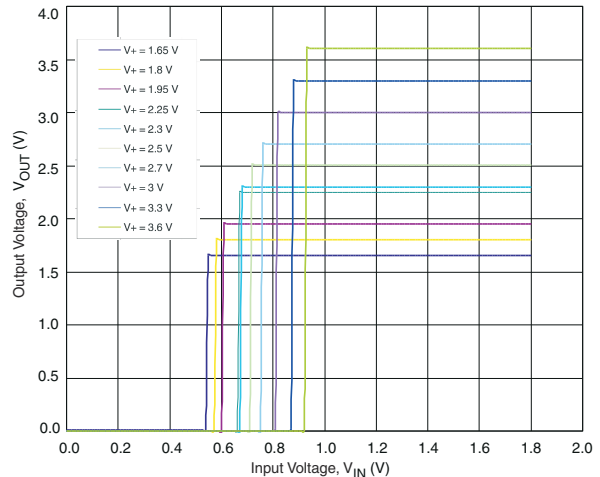


图 6-6. Control Input Thresholds (IN1, $T_A = 25^\circ\text{C}$)

6.8 Typical Characteristics (continued)

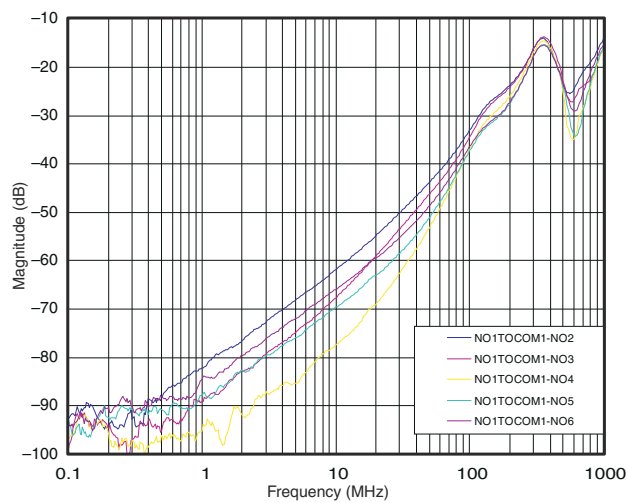


图 6-7. Crosstalk Adjacent

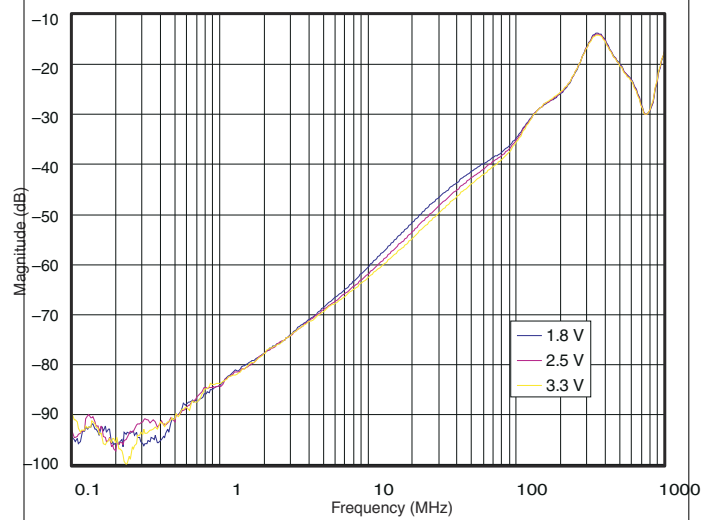


图 6-8. Crosstalk

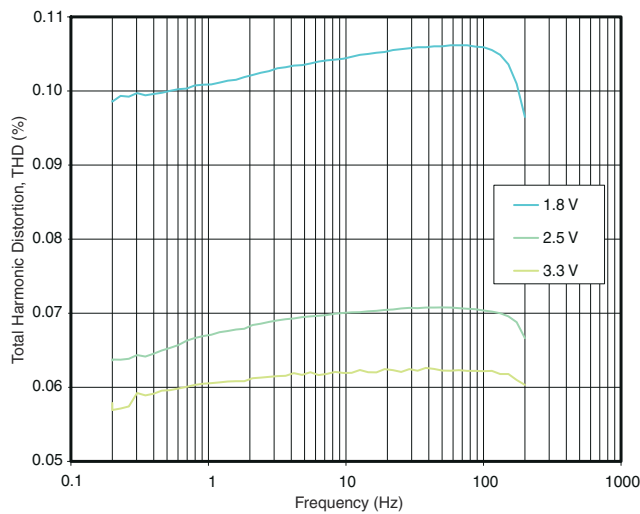


图 6-9. Total Harmonic Distortion vs Frequency

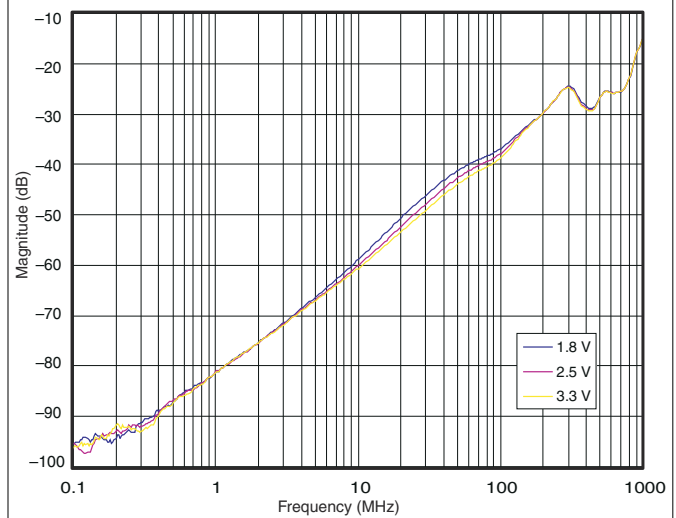


图 6-10. OFF Isolation

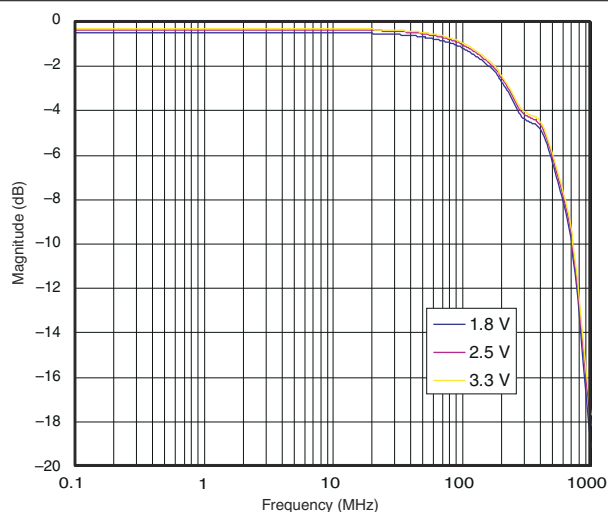


图 6-11. Insertion Loss

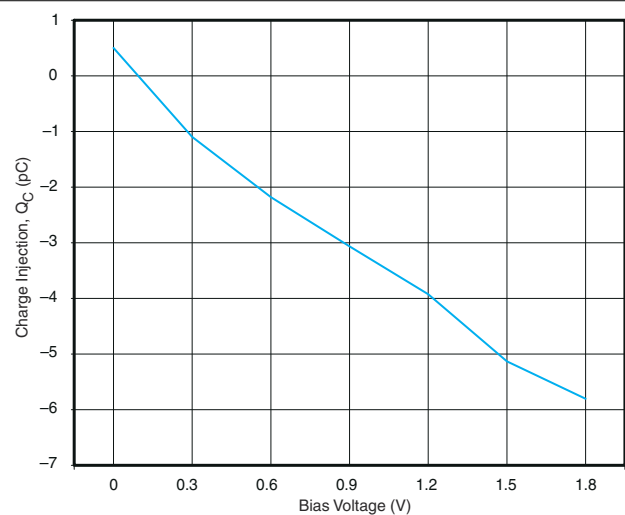


图 6-12. Charge Injection vs Bias Voltage (1.8 V)

6.8 Typical Characteristics (continued)

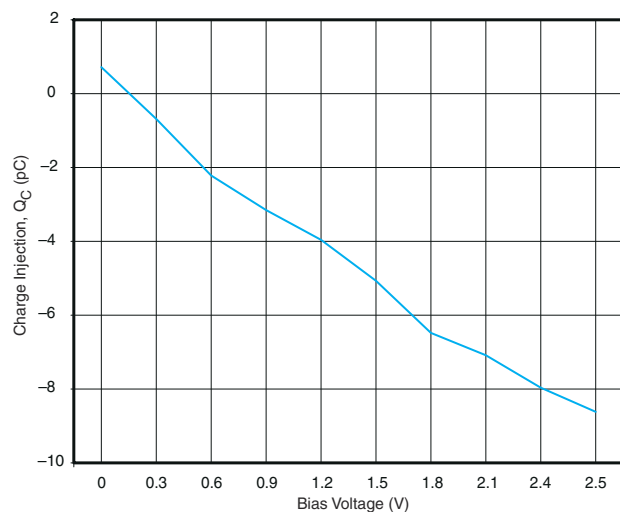


图 6-13. Charge Injection vs Bias Voltage (2.5 V)

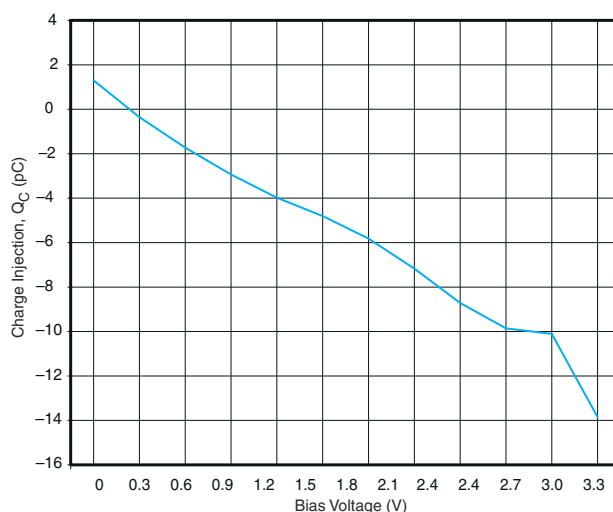


图 6-14. Charge Injection vs Bias Voltage (3.3 V)

7 Parameter Measurement Information

表 7-1. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the OFF state
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the ON state and the output (NC or NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN, $\overline{EN}$)
V_{IL}	Maximum input voltage for logic low for the control input (IN, $\overline{EN}$)
V_I	Voltage at the control input (IN, $\overline{EN}$)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN, $\overline{EN}$)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or NO) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is ON
C_I	Capacitance of control input (IN, $\overline{EN}$)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC1 to NO1). Adjacent crosstalk is a measure of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is – 3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND



$$r_{on} = \frac{V_{COM}}{I_{COM}} \frac{V_{NO}}{\Omega}$$

$$V_{IN} = V_{IH} \text{ or } V_{IL}$$

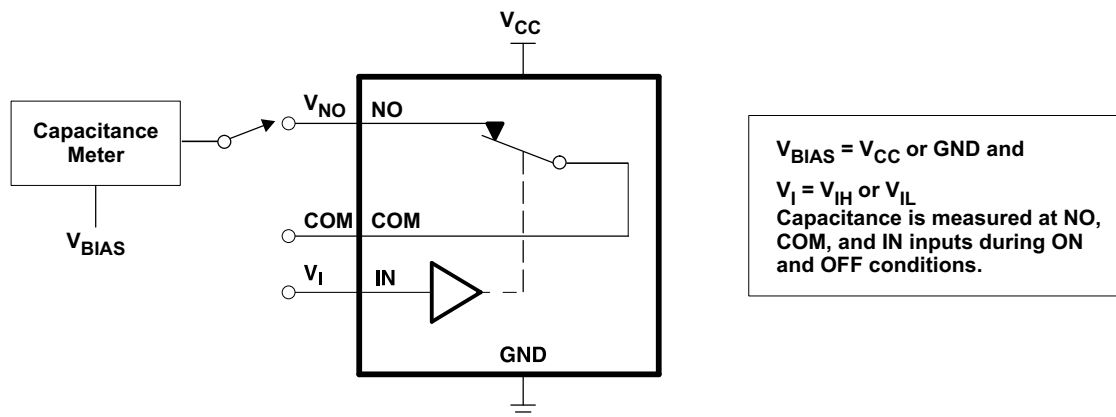
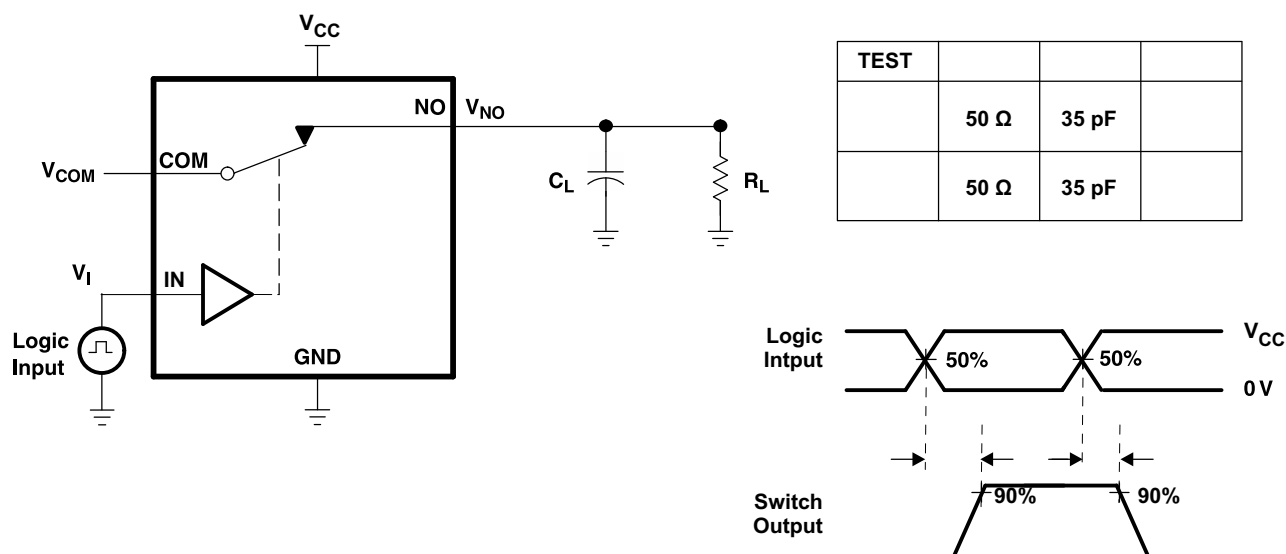
图 7-1. ON-state Resistance (r_{ON})



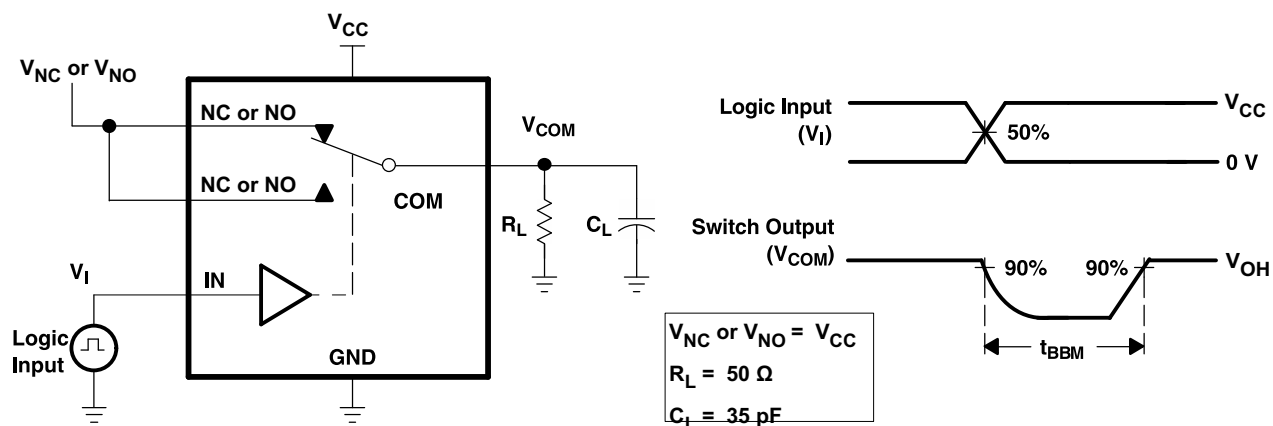
图 7-2. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWROFF)}$)



图 7-3. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

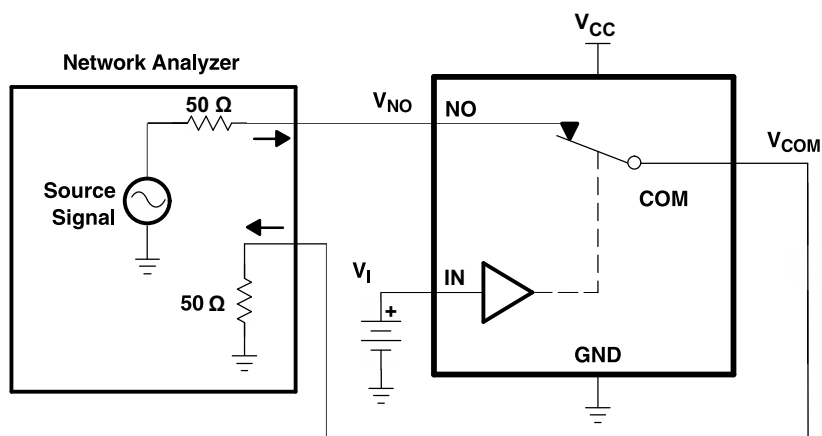
图 7-4. Capacitance (C_I , $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)

- A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
 B. C_L includes probe and jig capacitance.

图 7-5. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

- A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.

图 7-6. Break-Before-Make Time (t_{BBM})

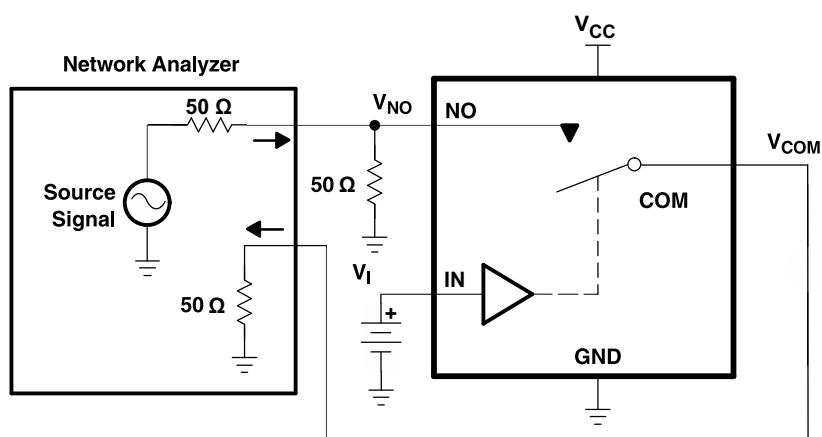


Channel ON: NO to COM
 $V_I = V_{IH}$ or V_{IL}

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)
DC Bias = 350 mV

图 7-7. Bandwidth (BW)

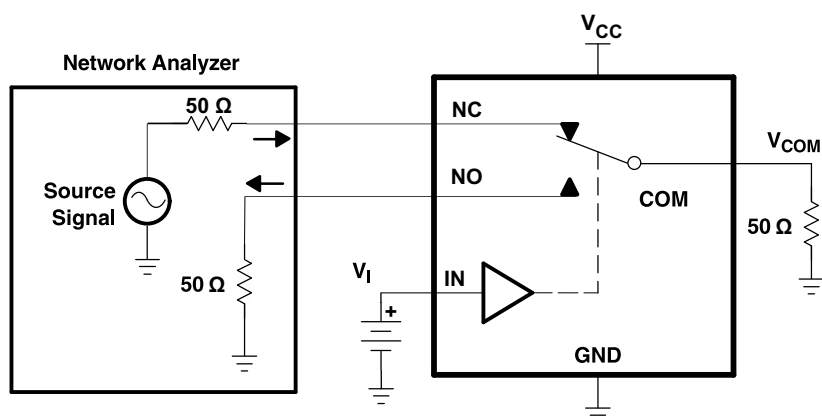


Channel OFF: NO to COM
 $V_I = V_{IH}$ or V_{IL}

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)
DC Bias = 350 mV

图 7-8. OFF Isolation (O_{ISO})

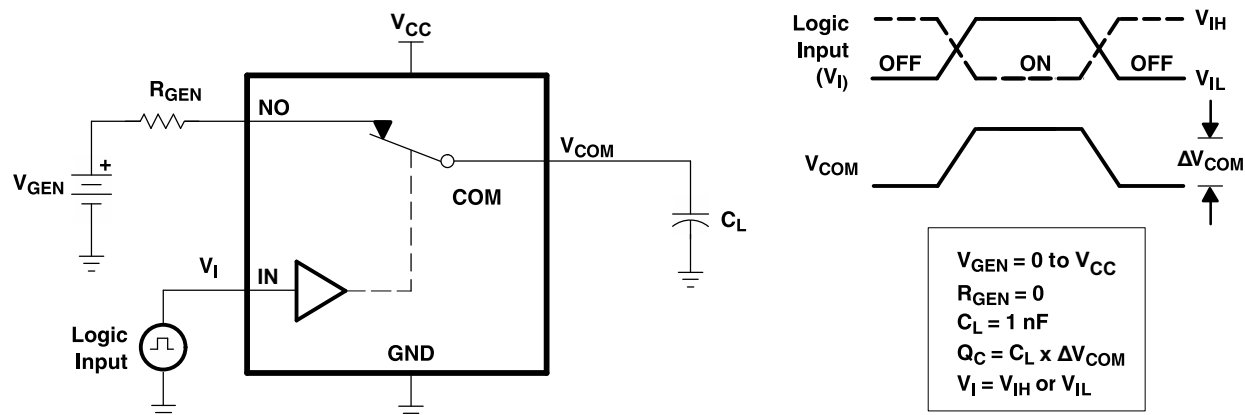


Channel ON: NC to COM
Channel OFF: NO to COM
 $V_I = V_{IH}$ or V_{IL}

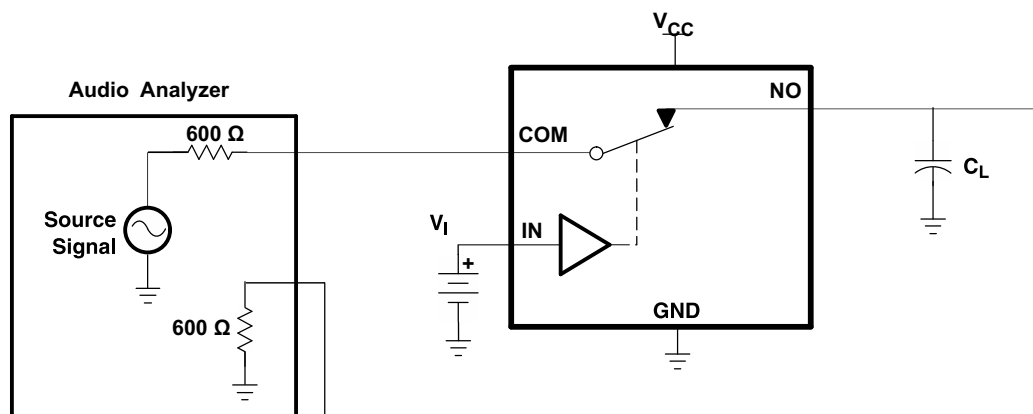
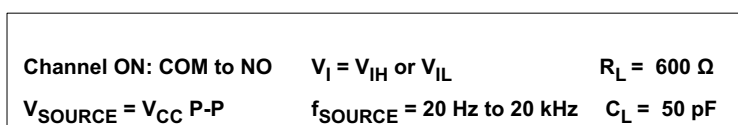
Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)
DC Bias = 350 mV

图 7-9. Crosstalk (X_{TALK})



- A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- B. C_L includes probe and jig capacitance.

图 7-10. Charge Injection (Q_C)

- A. C_L includes probe and jig capacitance.

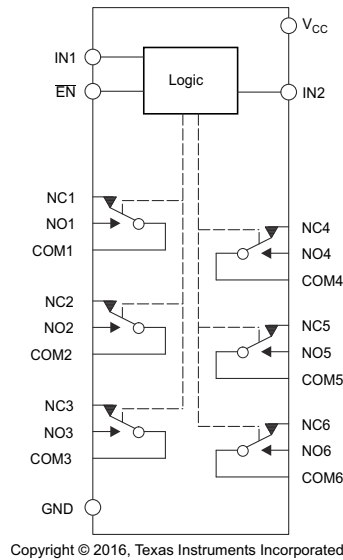
图 7-11. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS3A27518E-Q1 is a bidirectional, 6-channel, 1:2 multiplexer-demultiplexer designed to operate from 1.65 V to 3.6 V. This device can handle both digital and analog signals, and can transmit signals up to V_{CC} in either direction. The TS3A27518E-Q1 has two control pins, each controlling three 1:2 muxes at the same time, and an enable pin that puts all outputs in high-impedance mode. The control pins are compatible with 1.8-V logic thresholds and are backward compatible with 2.5-V and 3.3-V logic thresholds.

8.2 Functional Block Diagram



8.3 Feature Description

The isolation in power-down mode, $V_{CC} = 0$ feature places all switch paths in high-impedance state (High-Z) when the supply voltage equals 0 V.

8.4 Device Functional Modes

The TS3A27518E-Q1 is a bidirectional device that has two sets of three single-pole double-throw switches. Two digital signals control the 6 channels of the switch; one digital control for each set of three single-pole, double-throw switches. Digital input pin IN1 controls switches 1, 2, and 3, while pin IN2 controls switches 4, 5, and 6.

The TS3A27518E-Q1 has an $\overline{EN}$ pin that when set to logic high, it places all channels into a high-impedance or HIGH-Z state. 表 8-1 lists the functions of TS3A27518E-Q1.

表 8-1. Function Table

EN	IN1	IN2	NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6	NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

9.2 Typical Application

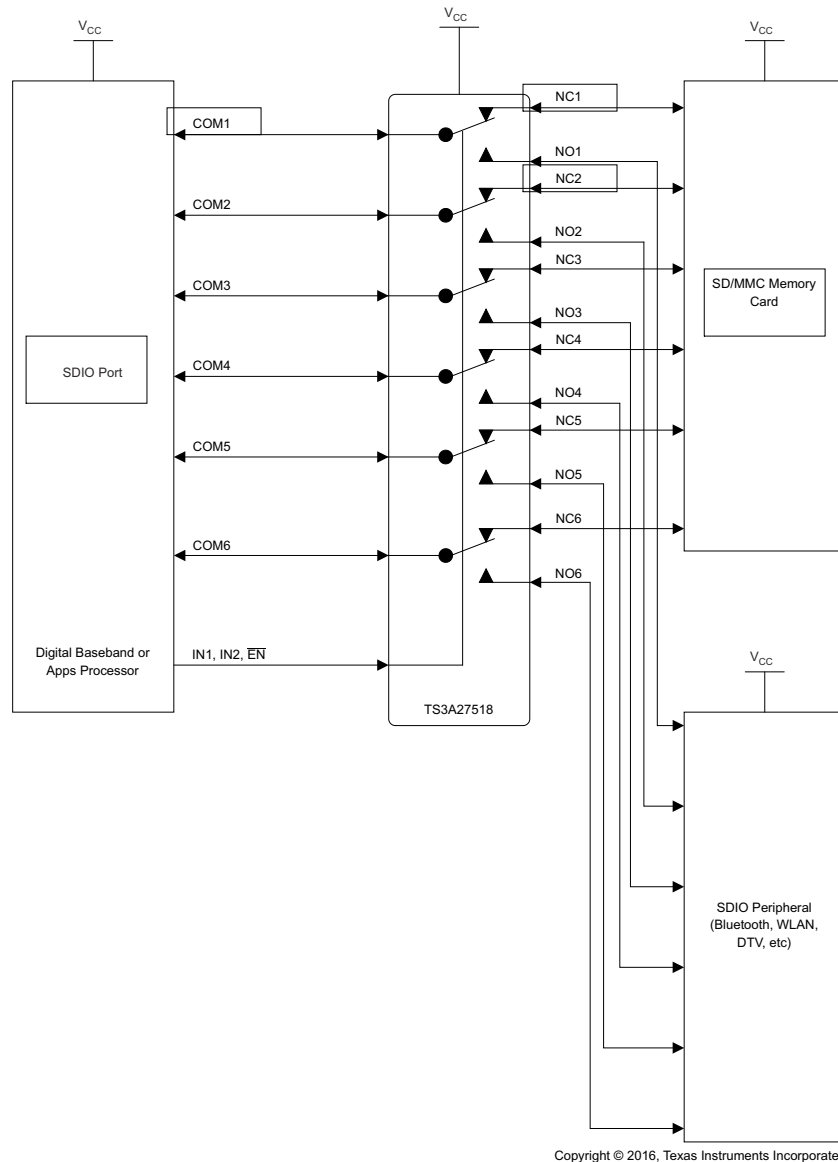


图 9-1. SDIO Expander Application Block Diagram

9.2.1 Design Requirement

Ensure that all of the signals passing through the switch are within the recommended operating ranges to ensure proper performance. For more information, see [节 6.3](#).

9.2.2 Detailed Design Procedure

The TS3A27518E-Q1 can operate properly without any external components. However, TI recommends connecting unused pins to the ground through a 50- Ω resistor to prevent signal reflections back into the device. TI also recommends that the digital control pins (INX) be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

For the RTW package connect the thermal pad to ground.

9.2.3 Application Curves

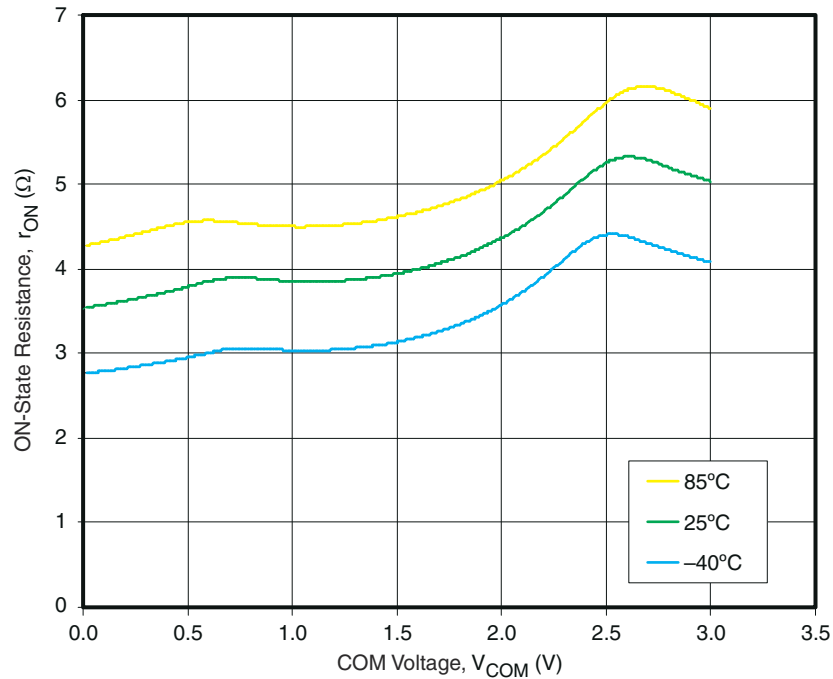


图 9-2. ON-State Resistance vs COM Voltage ($V_{CC} = 3$ V)

10 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence V_{CC} on first, followed by NO, NC, or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1- μ F capacitor is adequate for most applications, if connected from V_{CC} to GND.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, TI recommends following these common printed-circuit board layout guidelines:

- Bypass capacitors should be used on power supplies, and should be placed as close as possible to the V_{CC} pin
- Short trace-lengths should be used to avoid excessive loading
- For the RTW package, connect the thermal pad to ground

11.2 Layout Example

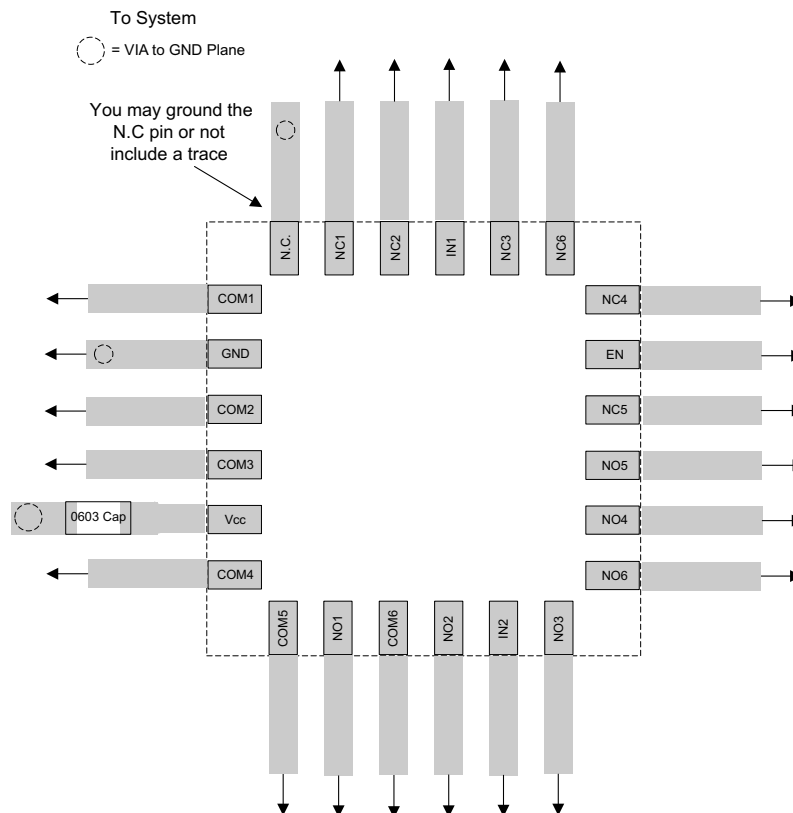


图 11-1. WQFN Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [TS3A27518E-Q1 Functional Safety FIT Rate, FMD and Pin FMA report](#)

12.2 接收文档更新通知

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12.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3A27518EIPWRQ1	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	YL518EQ1
TS3A27518EIRTWQR1	Active	Production	WQFN (RTW) 24	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	27518EI
TS3A27518ETRTWRQ1	Active	Production	WQFN (RTW) 24	3000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	27518ET

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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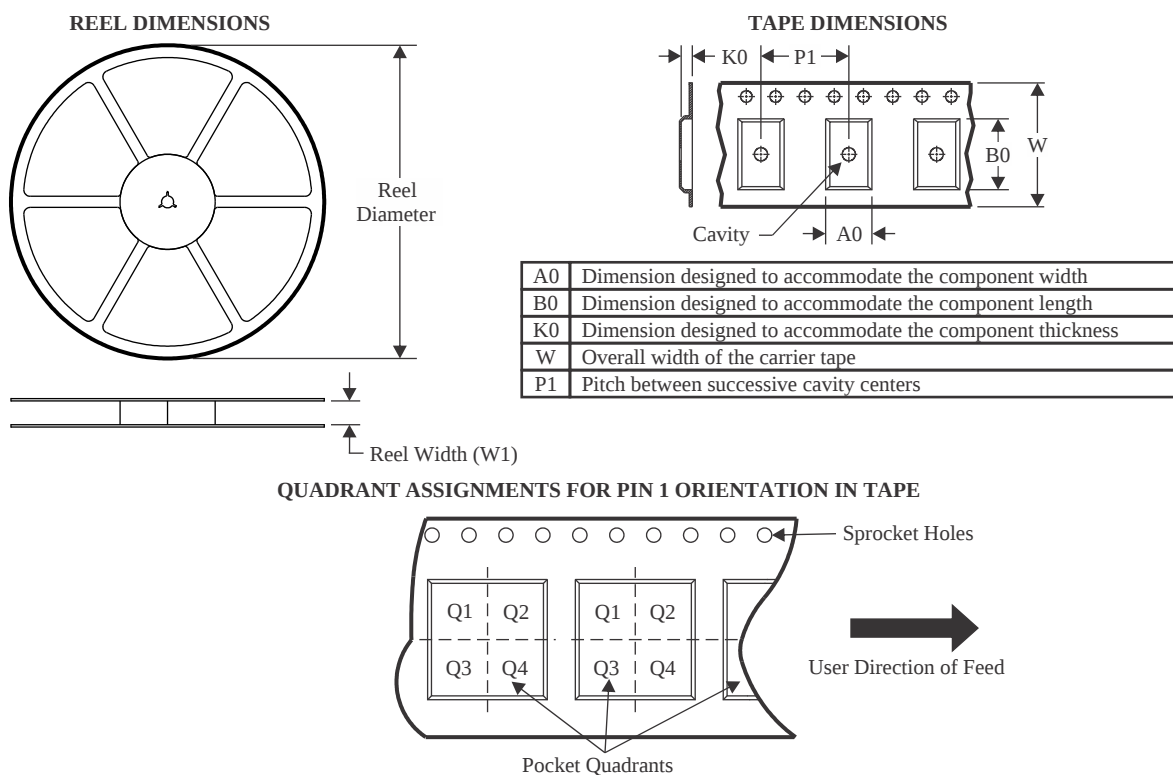
OTHER QUALIFIED VERSIONS OF TS3A27518E-Q1 :

- Catalog : [TS3A27518E](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

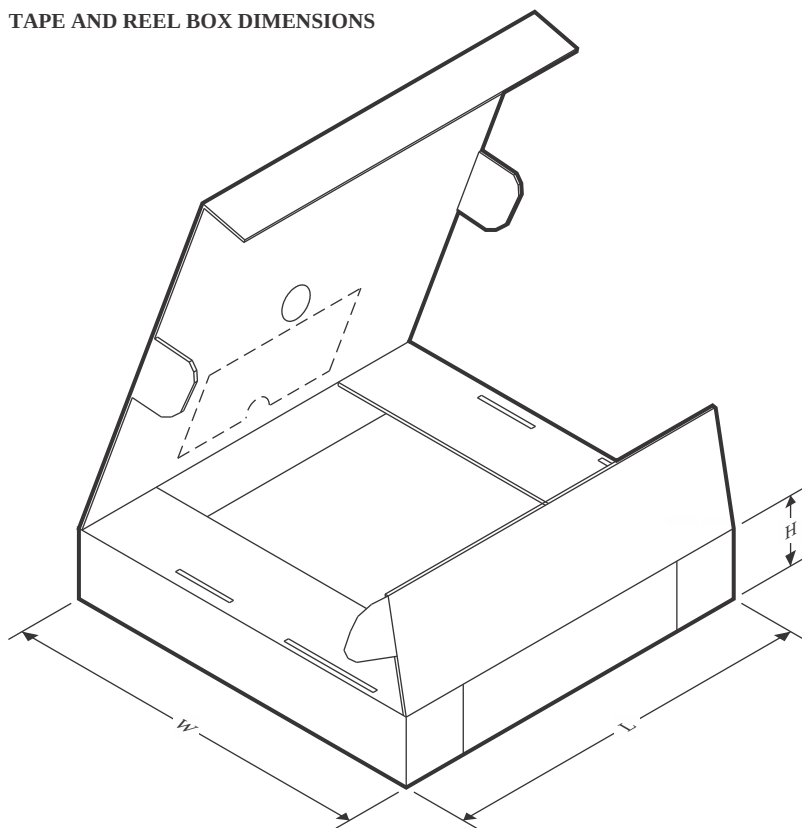
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A27518EIPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TS3A27518EIRTWRQ1	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TS3A27518ETRTWRQ1	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A27518EIPWRQ1	TSSOP	PW	24	2000	356.0	356.0	35.0
TS3A27518EIRTWRQ1	WQFN	RTW	24	3000	356.0	356.0	35.0
TS3A27518ETRTWRQ1	WQFN	RTW	24	3000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

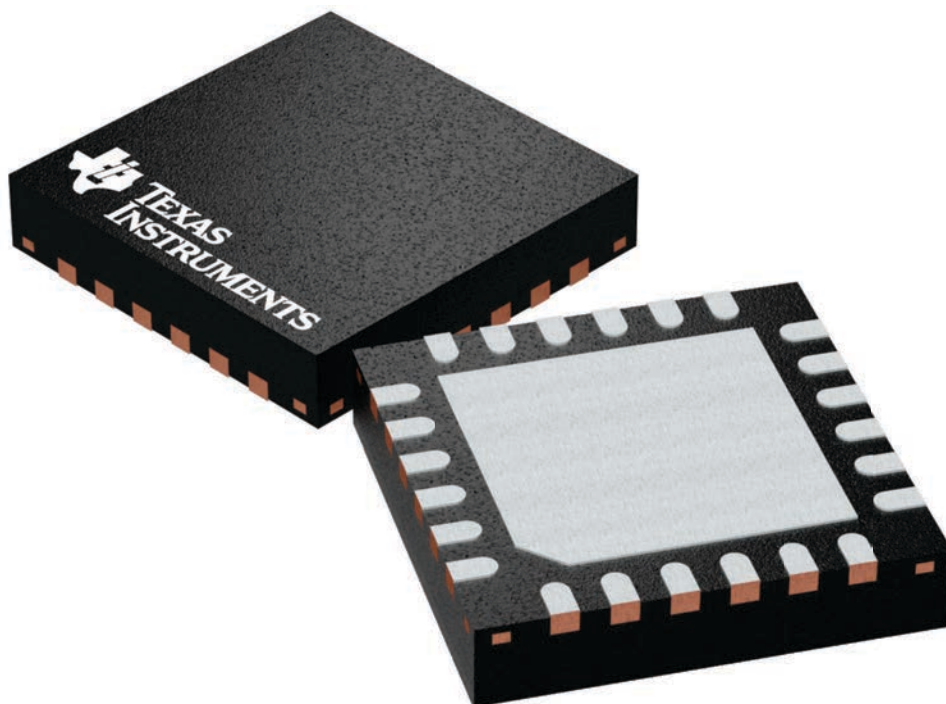
RTW 24

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224801/A

PACKAGE OUTLINE

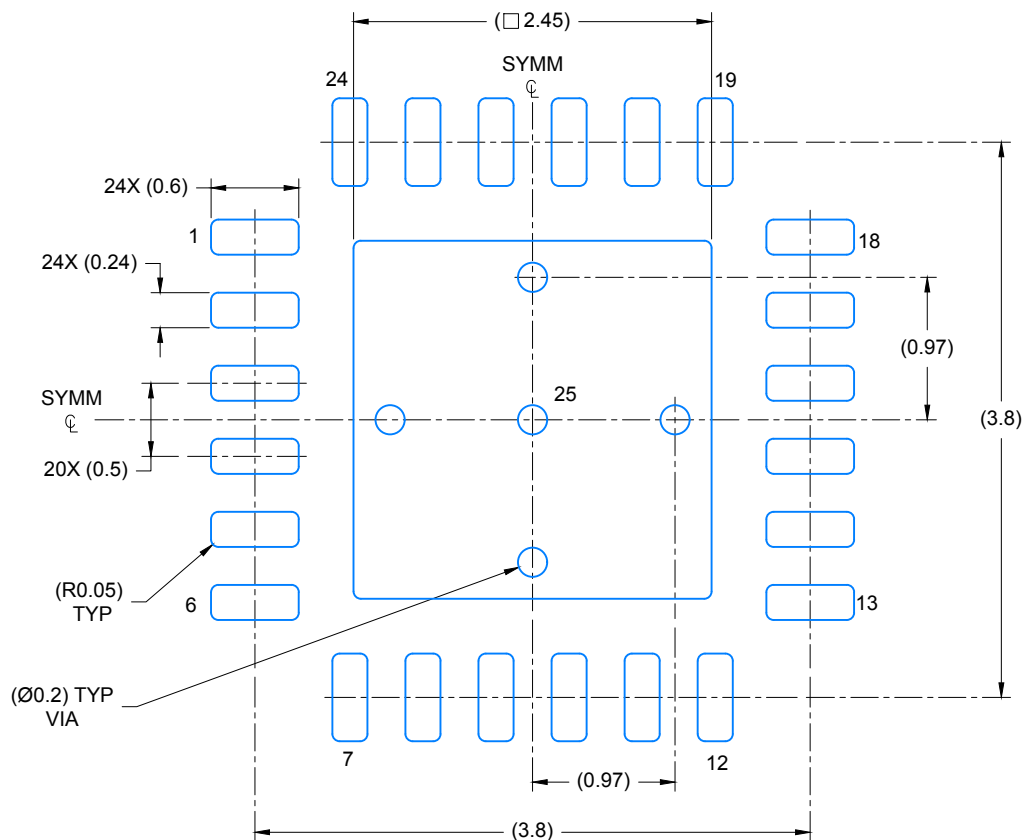
WQFN - 0.8 mm max height

The drawing illustrates the mechanical specifications of the QFN package across three views:

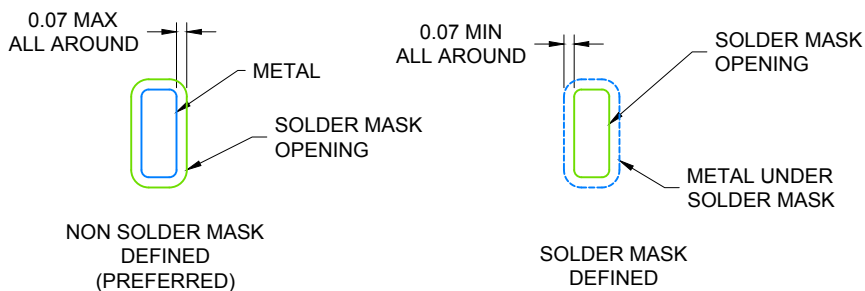
- Top View:** Shows a square package with a side length of 4.15 mm (3.85 mm BSC). A shaded region on the left is designated as the "PIN 1 INDEX AREA".
- Side View:** Shows the package height with a maximum of 0.8 mm. The bottom surface features a "SEATING PLANE" with a flatness tolerance of 0.08 mm. The solder mask thickness is specified as 0.05 mm to 0.00 mm.
- Detail View:** Provides a close-up of the package perimeter, showing 24 pins (12 on each long side) with a pitch of 0.5 mm. The central square area has a side length of 2.5 mm. The exposed thermal pad is 2.45 ± 0.1 mm square. The package is symmetrical (SYMM) about both horizontal and vertical centerlines. A "PIN 1 ID (OPTIONAL)" is indicated on the left side. A detail of the pin profile shows a width of 0.2 mm typical.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 20X

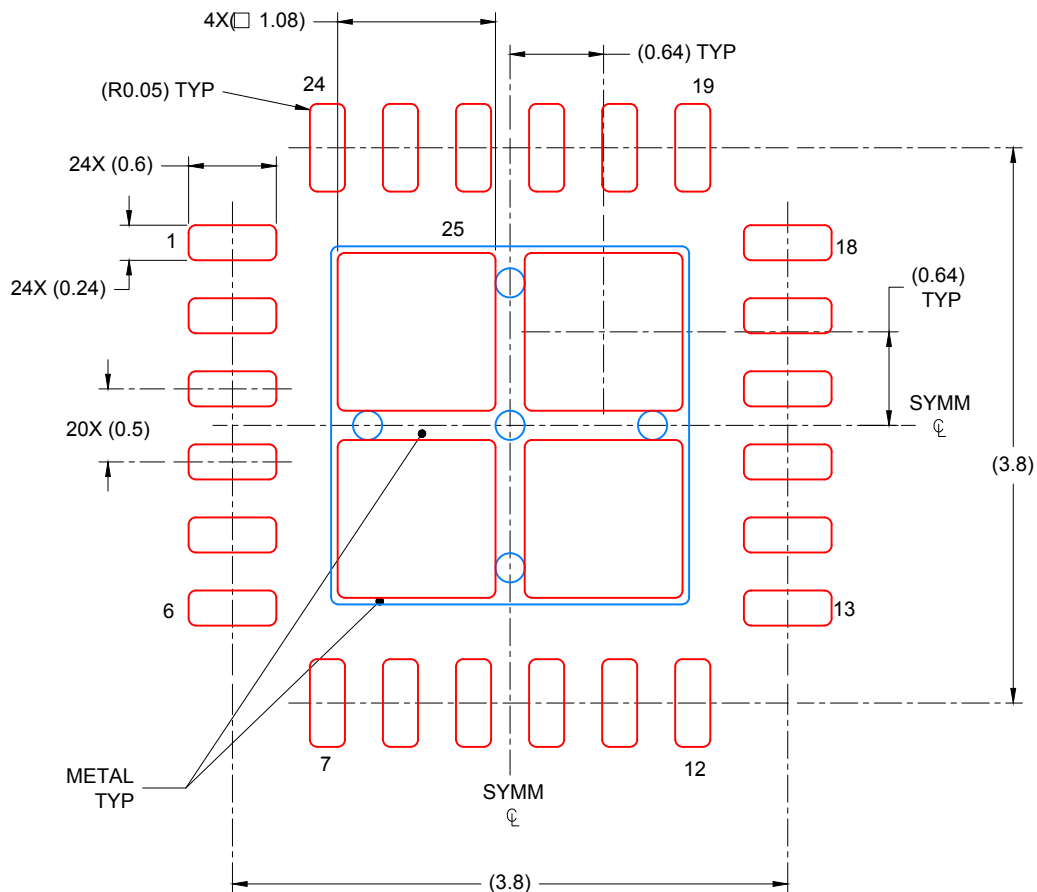


SOLDER MASK DETAILS

4219135/B 11/2016

NOTES: (continued)

- For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).



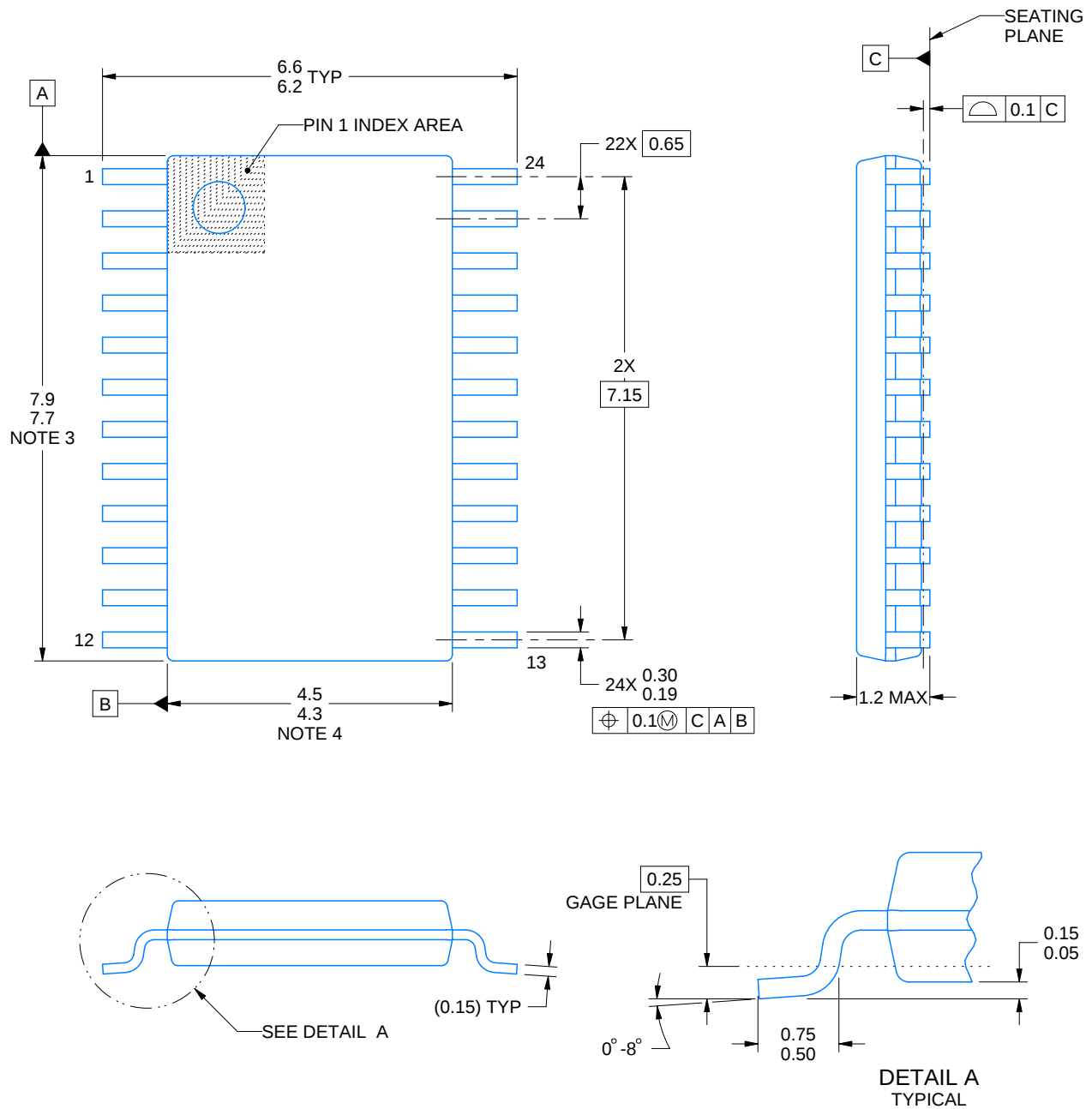
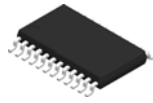
SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
 78% PRINTED COVERAGE BY AREA UNDER PACKAGE
 SCALE: 20X

4219135/B 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220208/A 02/2017

NOTES:

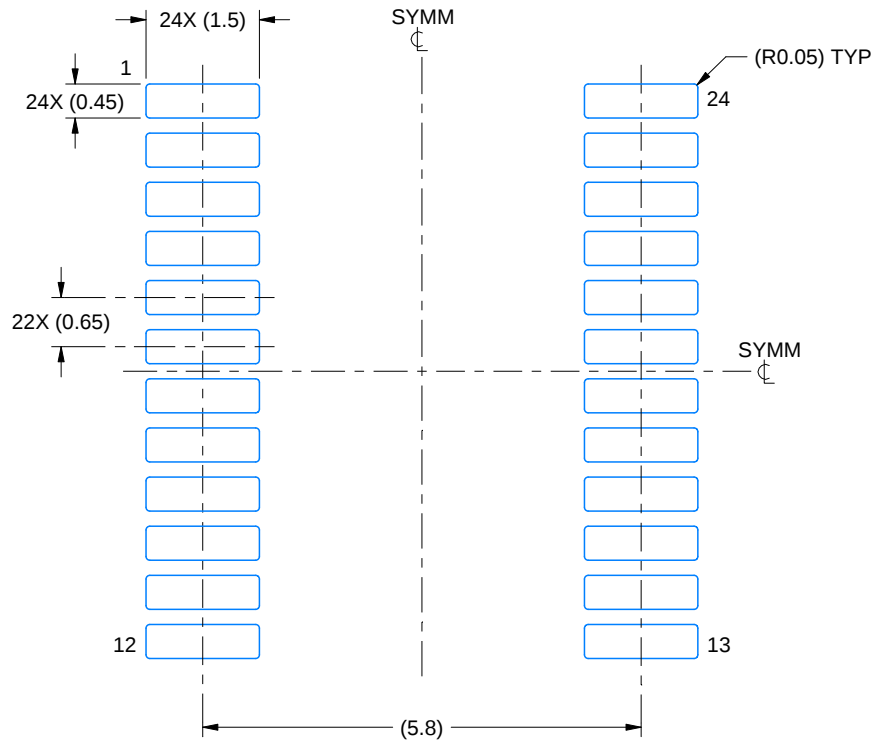
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

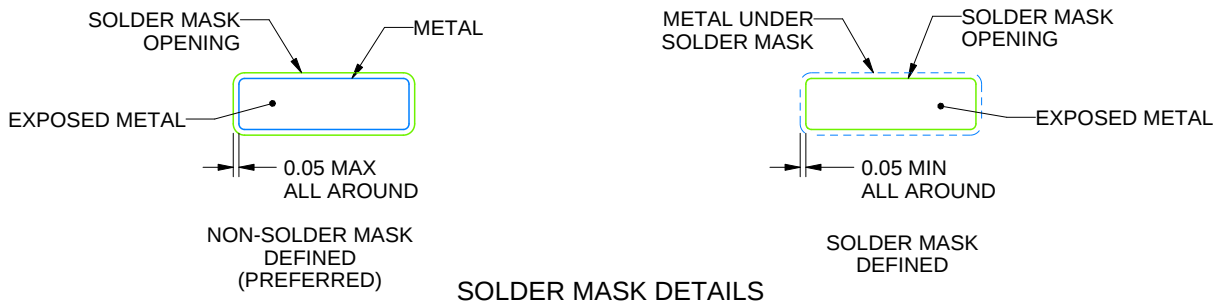
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

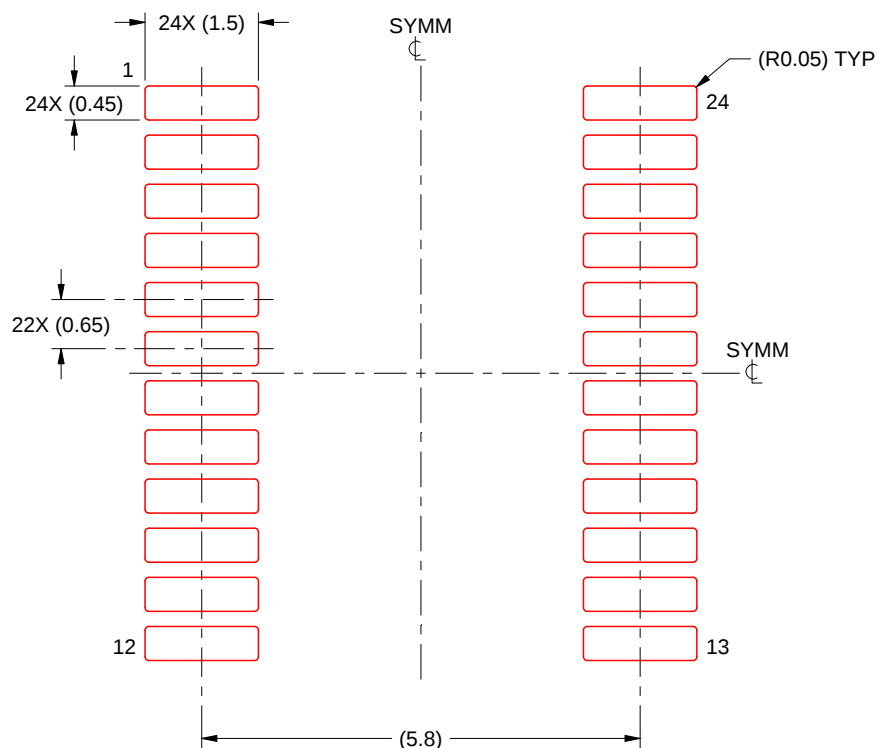
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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