具有可编程照明序列的四通道发光二极管 (LED) 驱动器

查询样片: LP5562

特性

- 具有 **8** 位电流设置（从 **0mA** 到 **25.5mA**，步长 **100μA**）和 **8** 位脉宽调制 **(PWM)** 控制的 **4** 个独立可编程 **LED** 输出
- 典型 **LED** 输出饱和电压 **60mV** 和 **1%** 电流匹配
- 针对 **LED** 输出的灵活 **PWM** 控制
- 具有外部时钟的自动节电模式
- **3** 个具有灵活指令集的程序执行引擎
- 具有程序执行引擎的自主运行
- 针对照明模式程序的 **SRAM** 程序存储器
- 芯片尺寸球栅阵列 **(DSBGA)**，**12** 焊锡凸点封装，**0.4mm** 焊球间距

应用范围

- 彩灯
- 指示器灯
- 袖珍键盘 **RGB** 背光和手机挂饰

描述

LP5562 是一款设计用于产生多种照明效果的四通道 LED 驱动器。 该器件具有一个产生多种照明序列的程序存储器。 当程序存储器已被载入时，LP5562 能够在无需处理器控制的情况下独立运行。

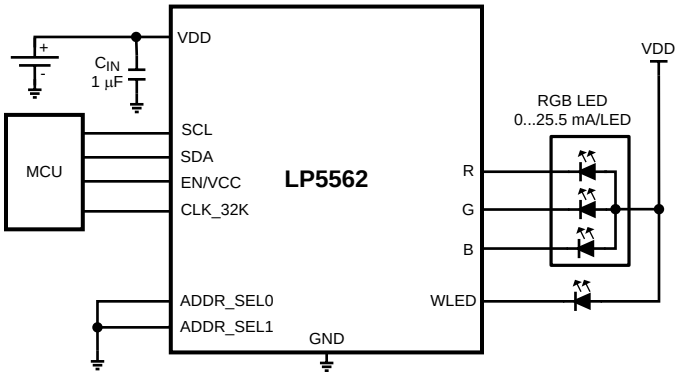
LP5562 能够自动进入省电模式，此时 LED 输出未被激活，从而降低流耗。

四个独立的 LED 通道具有准确的可编程电流吸收能力，从 0mA 到 25.5mA（步长 100μA），以及灵活的 PWM 控制。 每个通道可被配置为三个程序后执行引擎中的任何一个。 程序执行引擎具有使用 PWM 控制来产生所需照明序列的程序存储器。

LP5562 具有四个引脚可选 I²C™ 地址。 这可以在一条 I²C 总线内连接多达四个并联器件。 此器件只需一个小型、低成本陶瓷电容器。

LP5562 采用 DSBGA 封装。

TYPICAL APPLICATION



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Connection Diagrams

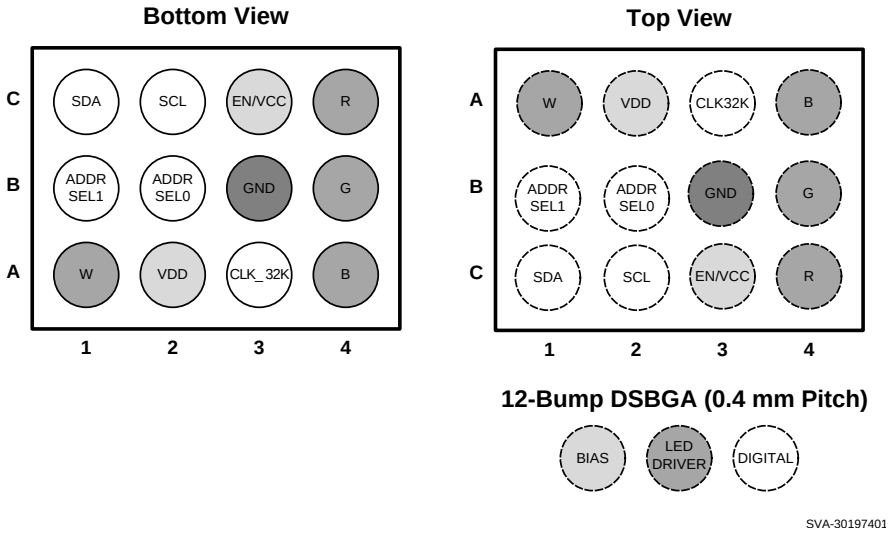

Figure 1. Top and Bottom View

PIN DESCRIPTIONS

Pin #	Name	Type	Description
A1	W	A	LED driver current sink terminal
B1	ADDR_SEL1	I	I^2C address selection pin
C1	SDA	I/O	I^2C serial interface data input/output
A2	VDD		Power Supply
B2	ADDR_SEL0	I	I^2C address selection pin
C2	SCL	I	I^2C serial interface clock
A3	CLK_32K	I	External 32 kHz clock input
B3	GND		Ground
C3	EN/VCC		Enable/Logic power supply
A4	B	A	LED driver current sink terminal
B4	G	A	LED driver current sink terminal
C4	R	A	LED driver current sink terminal

A: Analog Pin, I/O: Digital Bidirectional Pin, I: Digital Input Pin

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ABSOLUTE MAXIMUM RATINGS(1)

V(V_{DD} , $V_{EN/VCC}$, R, G, B, W)	−0.3V to +6.0V
Voltage on Logic Pins	−0.3V to V_{DD} +0.3V with 6.0V max
Continuous Power Dissipation(2)	Internally Limited
Junction Temperature (T_{J-MAX})	125°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering)	see(3)

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).
(3) For detailed soldering specifications and information, please refer to Texas Instruments Application Note AN1112 : DSBGA Wafer Level Chip Scale Package.

RECOMMENDED OPERATING CONDITIONS(1)(2)

V_{DD}	2.7V to 5.5V
$V_{EN/VCC}$	1.65V to V_{DD}
Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range(3)	−40°C to +85°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (TJ-MAX-OP = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θJA), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

THERMAL PROPERTIES(1)

Junction-to-Ambient Thermal Resistance (θ_{JA}), YQE0012ABAB Package(2)	68°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. Number given here is based on 4-layer standard JEDEC thermal test board or 4LJEDEC 4"x3" in size. The board has 2 embedded copper layers which cover roughly the same size as the board. The copper thickness for the four layers, starting from the top one, is 2 oz./1oz./1oz./2 oz. Detailed description of the board can be found in JESD 51-7. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (TJ-MAX-OP = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θJA), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

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ELECTRICAL CHARACTERISTICS(1)(2)(3)

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (−40°C < T_A < +85°C). Unless otherwise specified: V_{IN} = 3.6V, $V_{EN/VCC}$ = 1.8V.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Current Consumption and Oscillator electrical Characteristics						
I_{VDD}	Standby supply current	EN = 0 (pin), CHIP_EN = 0 (bit), external 32 kHz clock running or not running		0.2	2	µA
		EN = 1 (pin), CHIP_EN = 0 (bit), external 32 kHz clock not running		2		µA
		EN = 1 (pin), CHIP_EN = 0 (bit), external 32 kHz clock running		2.4		µA
	Normal mode supply current	LED drivers disabled		0.25		mA
		LED drivers enabled		1		mA
	Powersave mode supply current	External 32 kHz clock running		10		µA
		Internal oscillator running		0.25		mA
f_{OSC}	Internal oscillator frequency accuracy		–4		4	%
			–7		**7**	
LED Driver Electrical Characteristics (R, G, B, W Outputs)						
$I_{LEAKAGE}$	R, G, B, W pin leakage current			0.1	1	µA
I_{MAX}	Maximum source current	Outputs R, G, B, W		25.5		mA
I_{OUT}	Accuracy of output current(4)	Output current set to 17.5 mA, VDD = 3.6V	–4		4	%
			–5		**5**	
I_{MATCH}	Matching(4)	Output current set to 17.5 mA, VDD = 3.6V		1	**2**	%
f_{LED}	LED PWM switching frequency	PWM_HF = 1		558		Hz
		PWM_HF = 0		256		
V_{SAT}	Saturation voltage(5)	Output current set to 17.5 mA		60	100	mV

(1) The Electrical characteristics tables list ensured specifications under the listed Recommended Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not verified by production testing.
(2) All voltages are with respect to the potential at the GND pins.
(3) Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not verified by production, but do represent the most likely norm.
(4) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current outputs on the part, the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN)/AVG. The largest number of the two (worst case) is considered the matching figure. Note that some manufacturers have different definitions in use.
(5) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the set value.

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Logic Interface Characteristics

V(EN) = 1.65V unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LOGIC INPUT EN						
V_{IL}	Input Low Level				**0.5**	V
V_{IH}	Input High Level		**1.2**			V
I_I	Logic Input Current		**–1.0**		**1.0**	µA
t_{DELAY}	Input delay(1)			2		µs
LOGIC INPUT SCL, SDA, CLK_32K, ADDR_SEL0, ADDR_SEL1, V_{EN} = 1.8V						
V_{IL}	Input Low Level				**0.2xV(EN)**	V
V_{IH}	Input High Level		**0.8xV(EN)**			
I_I	Input Current		**–1.0**		**1.0**	µA
f_{CLK_32K}	Clock frequency			32		kHz
f_{SCL}	Clock frequency				**400**	kHz
LOGIC OUTPUT SDA						
V_{OL}	Output Low Level	I_{OUT} = 3 mA (pull-up current)		0.3	**0.5**	V
I_L	Output Leakage Current				**1.0**	µA

(1) The I^2C host should allow at least 1ms before sending data to the LP5562 after the rising edge of the enable line.

Recommended External Clock Source Conditions(2)(3)

Symbol	Parameter	Condition	Min	Typ	Max	Units
LOGIC INPUT CLK_32K						
f_{CLK_32K}	Clock Frequency			32.7		kHz
t_{CLKH}	High Time		6			µs
t_{CLKL}	Low Time		6			
t_r	Clock Rise Time	10% to 90%			2	
t_f	Clock Fall Time	90% to 10%			2	

(2) Specification is ensured by design and is not tested in production. V_{EN} = 1.65V to V_{DD}.
(3) The ideal external clock signal for the LP5562 is a 0V to VEN 25% to 75% duty-cycle square wave. At frequencies above 32.7kHz, program execution will be faster and at frequencies below 32.7 kHz program execution will be slower.

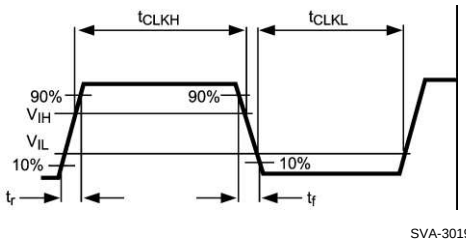

Figure 2. External Clock Timing

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I²C Timing Parameters (SDA, SCL)(1)

Symbol	Parameter	Limit		Units
		Min	Max	
f_{SCL}	Clock Frequency		400	kHz
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		
5	Data Hold Time	50		
6	Data Setup Time	100		
7	Rise Time of SDA and SCL	20+0.1Cb	300	
8	Fall Time of SDA and SCL	15+0.1Cb	300	
9	Set-up Time for STOP condition	600		
10	Bus Free Time between a STOP and a START Condition	1.3		µs
Cb	Capacitive Load for Each Bus Line	10	200	pF

(1) Specification is ensured by design and is not tested in production. V_{EN} = 1.65V to V_{DD}.

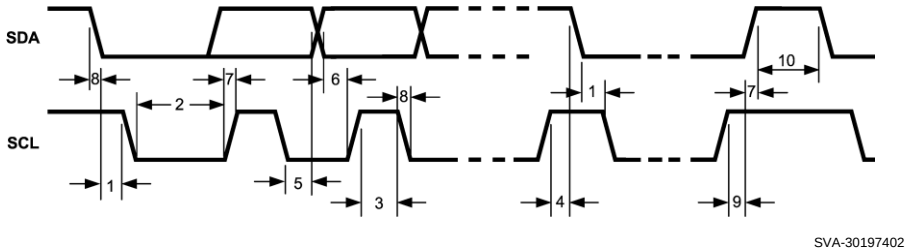

Figure 3. I²C Timing Parameters

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TYPICAL CURRENT CONSUMPTION PERFORMANCE CHARACTERISTICS

Unless otherwise specified: VDD = 3.6V, VEN = 3.3V.

Here are presented input current consumption measurements. Current consumption is measured during a LED blink program execution. Program code sets every LED output to full PWM value for 2 seconds and then PWM is set to 0 for 2 seconds. This is looped endlessly. 750 measurements are taken during one measurement cycle.

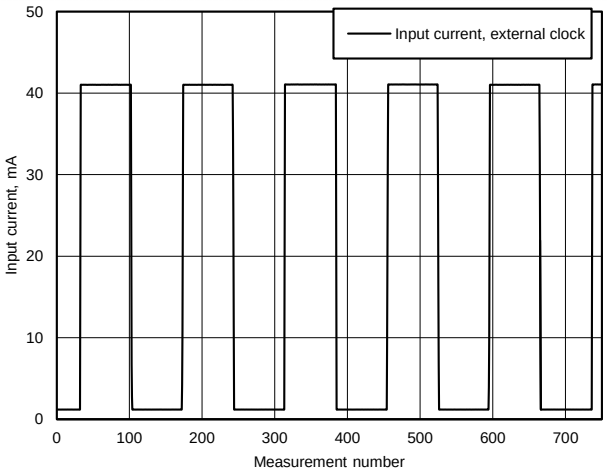

Figure 4. Input Current Consumption in Normal Mode With External Clock Running. 4 LEDs (RGBW) Set as Load. Every LED Driver Current Value Is Set to 10 mA.

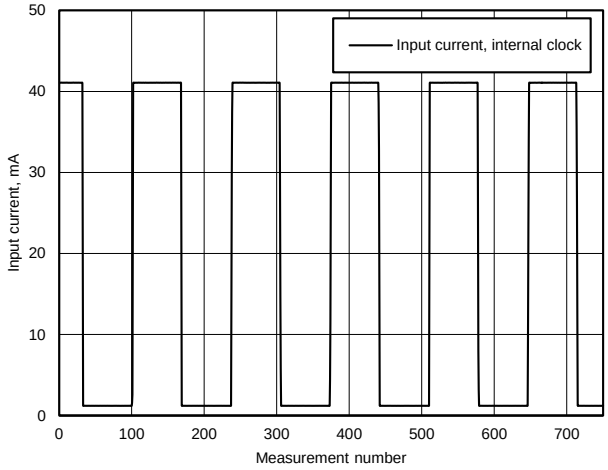

Figure 5. Input Current Consumption in Normal Mode With Internal Clock Running. 4 LEDs (RGBW) Set as Load. Every LED Driver Current Value Is Set to 10 mA.

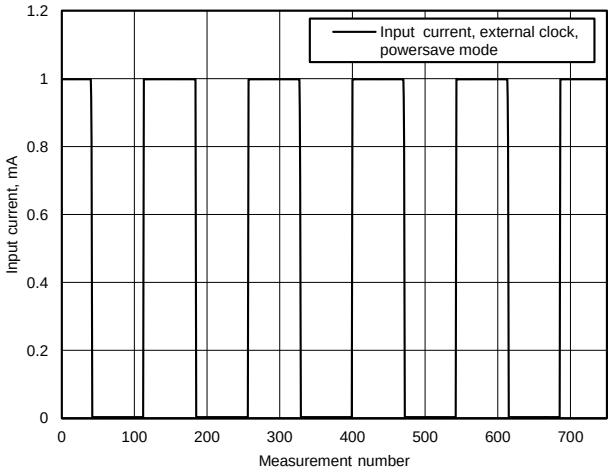

Figure 6. Input Current Consumption in Power Save Mode With External Clock Running. Here Is No LEDs as Load. All 4 LED Drivers Are Enabled During Program Execution.

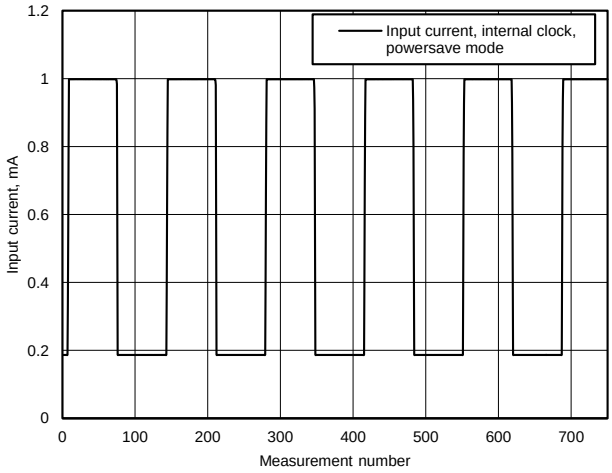

Figure 7. Input Current Consumption in Power Save Mode With Internal Clock Running. Here Is No LEDs as Load. All 4 LED Drivers Are Enabled During Program Execution.

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TYPICAL CURRENT CONSUMPTION PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: VDD = 3.6V, VEN = 3.3V.

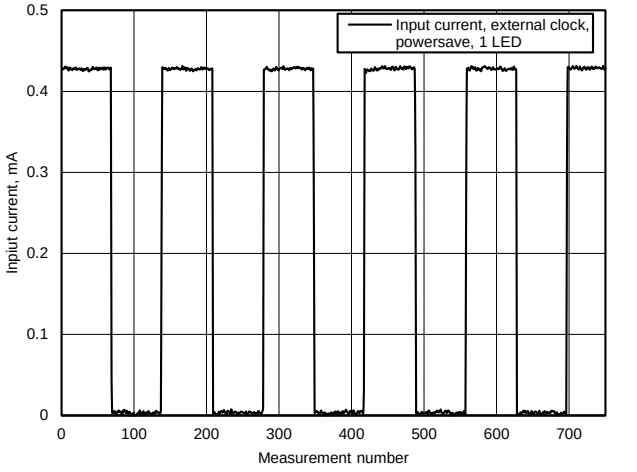

Figure 8. Input Current Consumption in Power Save Mode With External Clock Running. Here Is No LEDs as Load. Only 1 LED Driver Is Enabled During Program Execution.

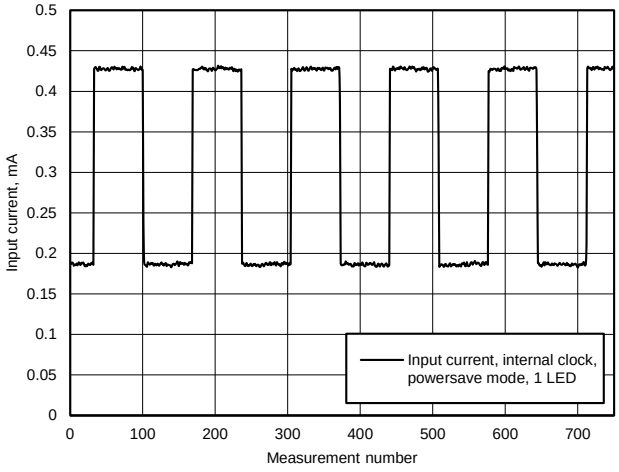

Figure 9. Input Current Consumption in Power Save Mode With Internal Clock Running. Here Is No LEDs as Load. Only 1 LED Driver Is Enabled During Program Execution.

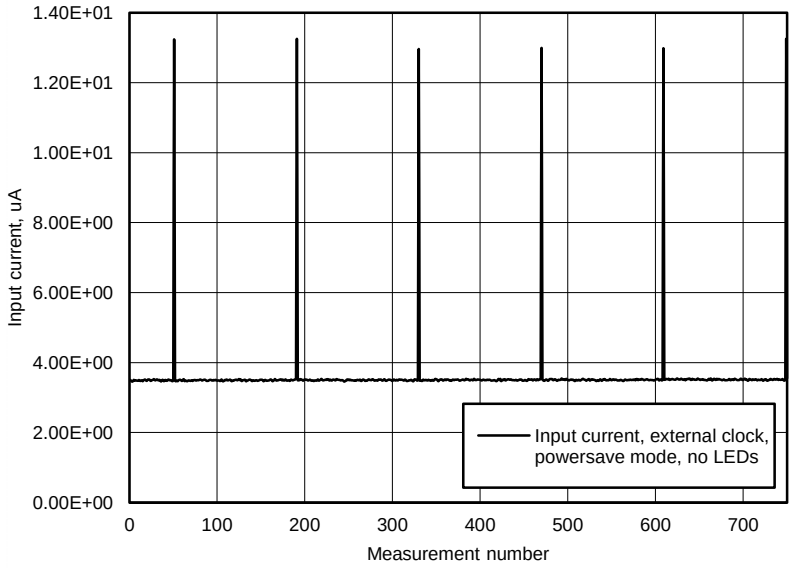

Figure 10. Input Current Consumption in Power Save Mode With External Clock Running. Here Is No LEDs as Load. No LED Drivers Are Enabled During Program Execution.

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TYPICAL LED OUTPUT PERFORMANCE CHARACTERISTICS

LED driver typical performance images.

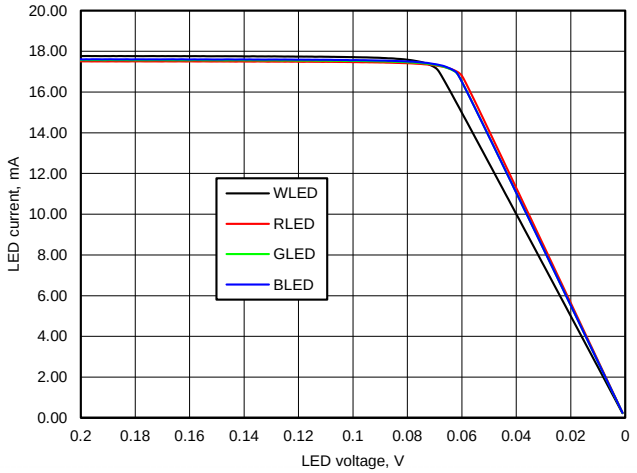

Figure 11. Every LED Driver Saturation Voltage, When Current Setting Is 17.5 mA.

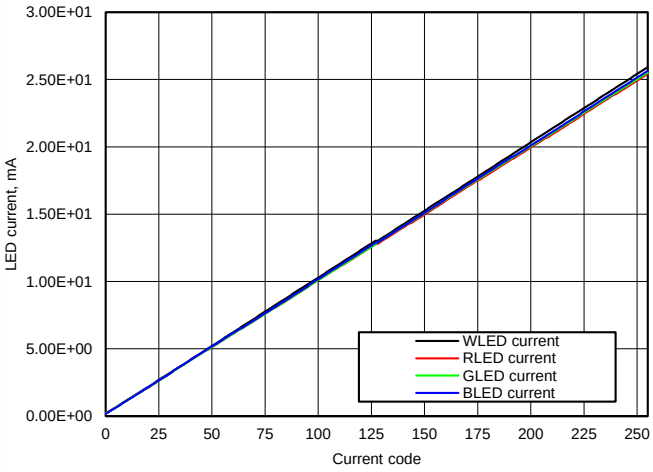

Figure 12. LED Driver Currents Compared to Current Setting Code.

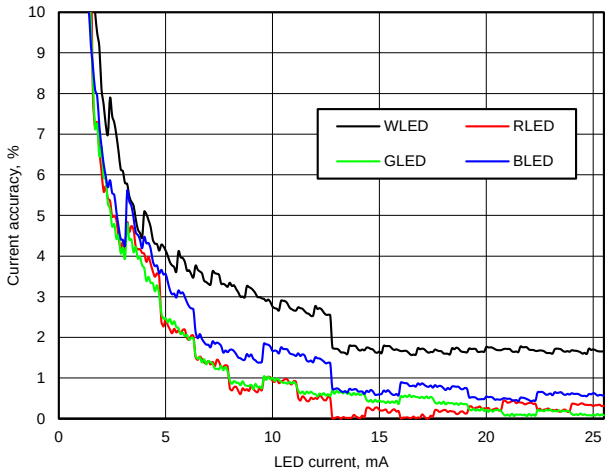

Figure 13. LED Driver Current Accuracy With Different Current Setting.

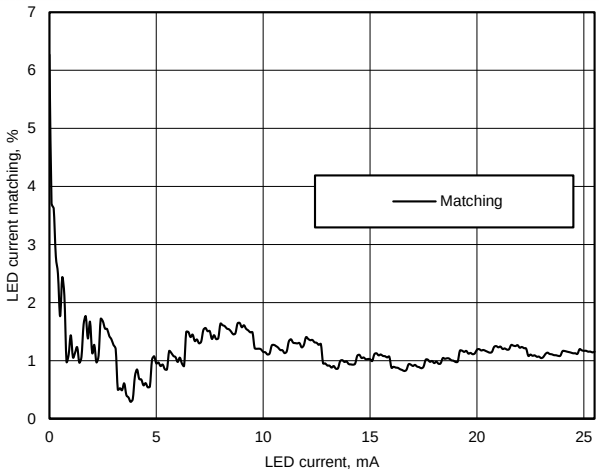

Figure 14. LED Driver Current Matching Between All LED Drivers With Different Current Setting.

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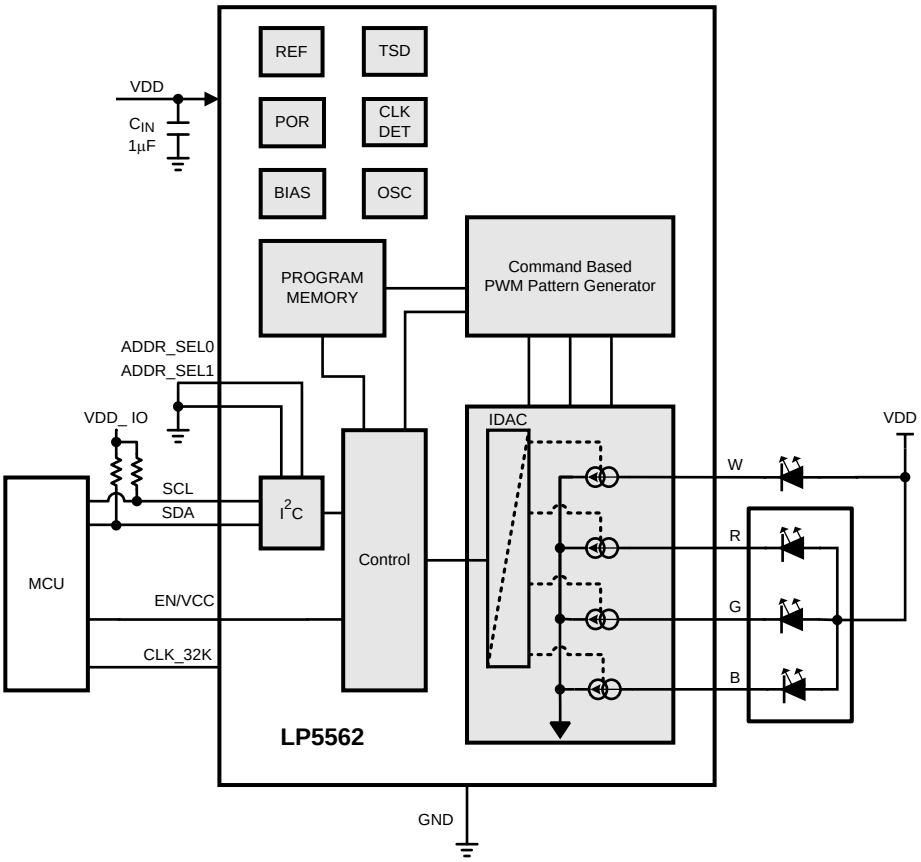
FUNCTIONAL BLOCK DIAGRAM



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MODES OF OPERATION

RESET: In the *reset* mode all the internal registers are reset to the default values. Reset is done always if FFh is written to Reset Register (0Dh) or internal Power On Reset is activated. Power On Reset (POR) will activate when supply voltage is connected or when the supply voltage V_{DD} falls below 1.5V (typ). Once V_{DD} rises above 1.9V (typ), POR will inactivate and the chip will continue to the *standby* mode. CHIP_EN control bit is low after POR by default.

STANDBY: The *standby* mode is entered if the register bit CHIP_EN or EN pin is *low* and Reset is not active. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode if EN pin is high. Control bits are effective after start up.

STARTUP: When CHIP_EN bit is written high and EN pin is high, the *internal startup sequence* powers up all the needed internal blocks (VREF, Bias, Oscillator etc.). Startup delay after setting EN pin *high* is 1 ms (typ.). Startup delay after setting chip_en bit to '1' is 500µs (typ.). If the device temperature rises too high, the Thermal Shutdown (TSD) disables the device operation and the device state is in *startup* mode, until no thermal shutdown event is present.

NORMAL: During *normal* mode the user controls the device using the Control Registers. If EN pin is set low, the CHIP_EN bit is reset to 0.

POWER SAVE: In *power save* mode analog blocks are disabled to minimize power consumption. See chapter Power Save Mode for further information.

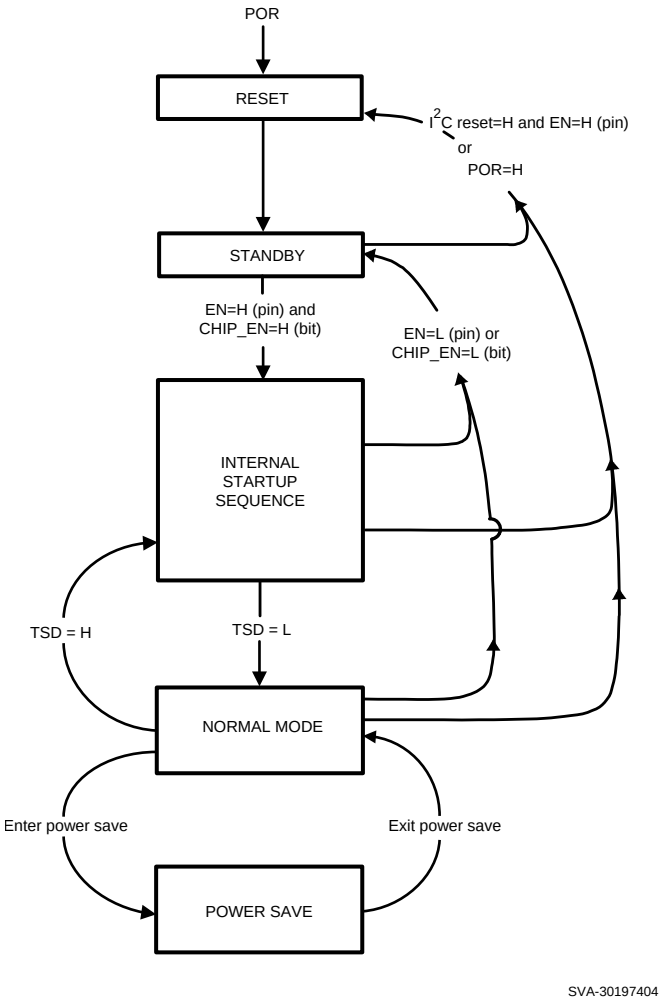

Figure 15. Modes of Operation

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FUNCTIONAL DESCRIPTION

LED Drivers Operational Description

The LP5562 have 4 LED drivers that are constant current sinks with 8-bit current and 8-bit PWM control. Current is controlled from I^2C registers. PWM can be controlled with program execution engines or direct I^2C register writes.

LED Driver Current Control

LED driver output current can be programmed with I^2C register from 0 mA up to 25.5 mA. Current setting resolution is 100 µA (8-bit control).

Table 1. B_CURRENT Register (05h), G_CURRENT Register (06h), R_CURRENT Register (07h), W CURRENT Register (0Fh):

Name	Bit(s)	Description			
		Current setting			
		bin	hex	dec	mA
CURRENT	7:0	0000 0000	00	0	0.0
		0000 0001	01	1	0.1
		0000 0010	02	2	0.2
		0000 0011	03	3	0.3
		0000 0100	04	4	0.4
		0000 0101	05	5	0.5
		0000 0110	06	6	0.6
		...	...	...	...
		1010 1111	**AF**	**175**	**17.5 (def)**
		...	...	...	...
		1111 1011	FB	251	25.1
		1111 1100	FC	252	25.2
		1111 1101	FS	253	25.3
		1111 1110	FE	254	25.4
		1111 1111	FF	255	25.5

Controlling LED Driver Output PWM

PWM can be controlled by either with program execution engines (1, 2 and 3) or via I^2C registers (02h for B, 03h for G, 04h for R and 0Eh for W).

Control of LED driver output PWM selection is managed with 2 bits for each LED output from register 70h. The Table 3 describes the selection options. With these bits for example all LED outputs can be controlled from one program execution engine.

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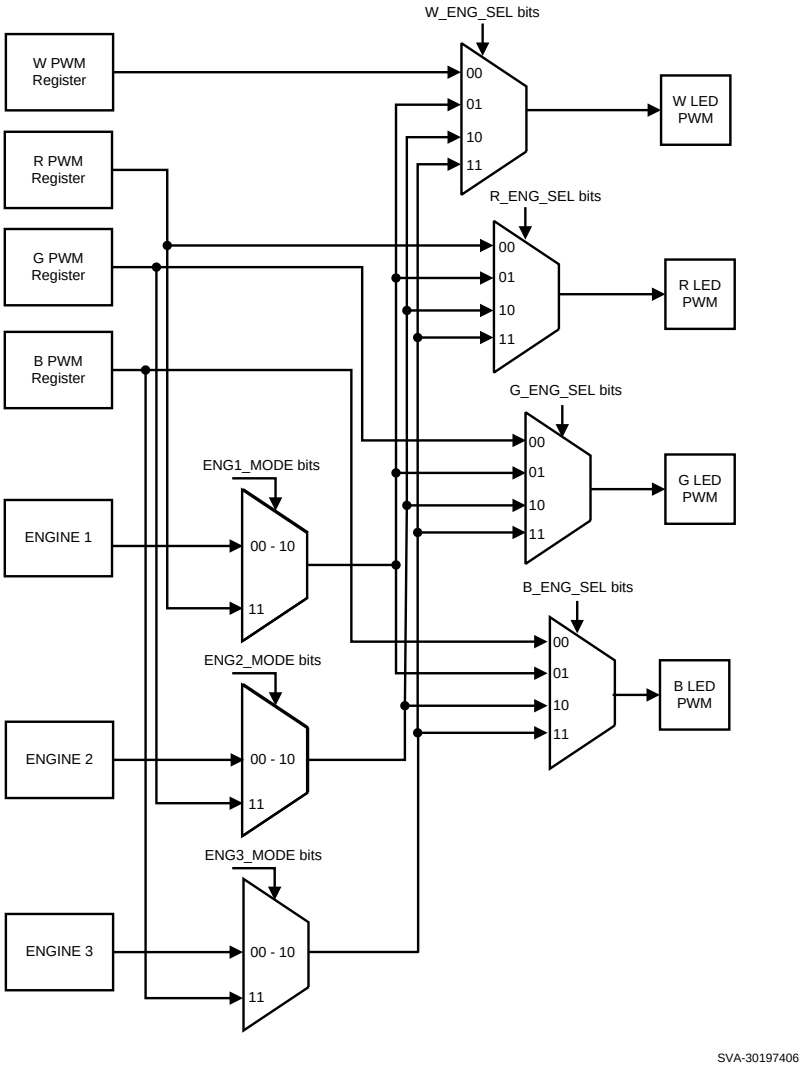

Figure 16. Controlling LED Outputs

The LED driver PWM control with 8-bit I²C register is defined in table Table 2.

Table 2. LED Driver PWM Control Bits Register 70h

Name	Bit(s)	Description
PWM	7:0	LED PWM value during I²C control operation mode
		0000 0000 = 0% PWM
		1111 1111 = 100% PWM

If the LED driver outputs are controlled with engines, the engine adjusts the PWM according to the program code. However, when the engine *mode* bits are set to '11', the engine is set to *direct* mode. In *direct* mode the PWM controls of engines comes:

- Engine 1 PWM control comes from B PWM I²C register (02h)
- Engine 2 PWM control comes from G PWM I²C register (03h)
- Engine 3 PWM control comes from R PWM I²C register (04h)

When the engine *mode* bits are set to '11' along with the LED PWM Output selection bits, it is possible to control all LED outputs from one I²C register.

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Table 3. LED PWM Output Selection Bits

B_ENG_SEL bits[1:0] G_ENG_SEL bits[3:2] R_ENG_SEL bits[5:4] W_ENG_SEL bits[7:6]	Description
00	Output is controlled via I^2C registers
01	ENG1_MODE and ENG1_EXEC register control LED output PWM instead of I^2C register
10	ENG2_MODE and ENG2_EXEC register control LED output PWM instead of I^2C register
11	ENG3_MODE and ENG3_EXEC register control LED output PWM instead of I^2C register

Direct I^2C Register PWM Control Example

- Device Start-up
  - Supply 3.6V to VDD
  - Supply 1.8V to EN
  - Wait 1 ms
  - Write to address 00h 0100 0000b (chip_en to '1')
  - Wait 500 µs (startup delay)
- Use internal clock
  - Write to address 08h 0000 0001b (enable internal clock)
- Direct PWM control
  - Write to address 70h 0000 0000b (Configure all LED outputs to be controlled from I^2C registers)
- Write PWM values
  - Write to address 02h 1000 0000b (B driver PWM 50% duty cycle)
  - Write to address 03h 1100 0000b (G driver PWM 75% duty cycle)
  - Write to address 04h 1111 1111b (R driver PWM 100% duty cycle)

LEDs are turned on after the PWM values are written. Changes to the PWM value registers are reflected immediately to the LED brightness. Default LED current (17.5mA) is used for LED outputs, if no other values are written.

PWM frequency is either 256 Hz or 558 Hz. Frequency is set with PWM_HF bit in register 08h. When PWM_HF is 0, the frequency is 256Hz. When the PWM_HF bit is 1, the PWM frequency is 558 Hz. Brightness adjustment is either linear or logarithmic. This can be set with LOG_EN bit in register 00h. When LOG_EN = 0 linear adjustment scale is used and when LOG_EN = 1 logarithmic scale is used. By using logarithmic scale the visual effect seems linear to the eye. Register control bits are presented in following tables:

Table 4. ENABLE Register (00h):

Name	Bit(s)	Description
LOG_EN	7	Logarithmic PWM adjustment enable bit 0 = Linear adjustment 1 = Logarithmic adjustment

Table 5. CONFIG Register (08h):

Name	Bit(s)	Description
PWM_HF	6	PWM clock frequency 0 = 256 Hz 1 = 558 Hz

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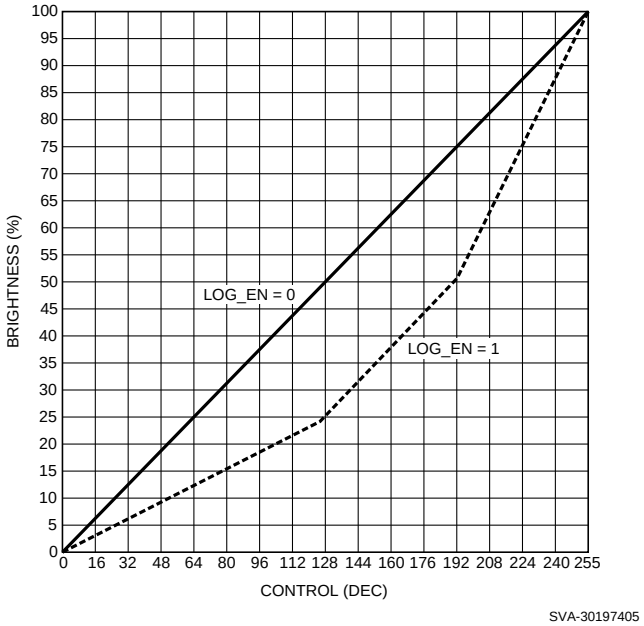

Figure 17. Logarithmic and Linear PWM Adjustment Curves

Program Execution Engines

Use of program execution engines is the other LED output PWM control method available in the LP5562. The device has 3 program execution engines. These engines create PWM controlled lighting patterns to the mapped LED outputs according to program codes developed by the user. Program coding is done using programming commands (see Program Execution Engine Programming Commands.) Programs are loaded into SRAM memory and engine control bits are used to run these programs autonomously. LED outputs can be mapped into these 3 engines with register 70h bit settings (see Table 3). The engines have different operation modes, program execution states, and program counters. Each engine has its own section of the SRAM memory.

Program Execution Engine States

Engine program execution is controlled from ENABLE register (00h). There are four different states for each engine, and these states are described in Table 6.

Table 6. ENABLE register (00h)

Name	Bit	Description
ENG1_EXEC	5:4	Engine 1 program execution **00b** = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode. **01b** = Step: Execute instruction defined by current Engine 1 PC value, increment PC, and change ENG1_EXEC to 00b (Hold). **10b** = Run: Start at program counter value defined by current Engine 1 PC value. **11b** = Execute instruction defined by current Engine 1 PC value and change ENG1_EXEC to 00b (Hold).
ENG2_EXEC	3:2	Engine 2 program execution **00b** = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode. **01b** = Step: Execute instruction defined by current Engine 2 PC value, increment PC, and change ENG2_EXEC to 00b (Hold). **10b** = Run: Start at program counter value defined by current Engine 2 PC value. **11b** = Execute instruction defined by current Engine 2 PC value and change ENG2_EXEC to 00b (Hold).

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Table 6. ENABLE register (00h) (continued)

Name	Bit	Description
ENG3_EXEC	1:0	Engine 3 program execution **00b** = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode. **01b** = Step: Execute instruction defined by current engine 3 PC value, increment PC, and change ENG3_EXEC to 00b (Hold). **10b** = Run: Start at program counter value defined by current engine 3 PC value. **11b** = Execute instruction defined by current engine 3 PC value and change ENG3_EXEC to 00b (Hold).

Program Execution Engine Operation Modes

Operation modes are defined in register address 01h. Each engine (1, 2, 3) operation mode can be configured separately. *Mode* registers are synchronized to a 32 kHz clock. Delay between consecutive I^2C writes to OP_MODE register (01h) need to be longer than 153 µs (typ).

Table 7. Operation Mode Register (OP_MODE (01h)):

Name	Bit	Description
ENG1_MODE	5:4	Engine 1 operation mode **00b** = Disabled, reset engine 1 PC **01b** = Load program to SRAM, reset engine 1 PC **10b** = Run program defined by ENG1_EXEC **11b** = Direct control from B PWM I^2C register, reset engine 1 PC
ENG2_MODE	3:2	Engine 2 operation mode **00b** = Disabled, reset engine 2 PC **01b** = Load program to SRAM, reset engine 2 PC **10b** = Run program defined by ENG2_EXEC **11b** = Direct control from G PWM I^2C register, reset engine 2 PC
ENG3_MODE	1:0	Engine 3 operation mode **00b** = Disabled, reset engine 3 PC **01b** = Load program to SRAM, reset engine 3 PC **10b** = Run program defined by ENG3_EXEC **11b** = Direct control from R PWM I^2C register, reset engine 3 PC

Operation Modes

- ***Disabled***
  - Each channel can be configured to disabled mode. For the current engine mapped LED output brightness will be 0 during this mode. Disabled mode resets respective engine's PC.
- ***Load program***
  - LP5562 can store 16 commands for each engine (1, 2, 3). Each command consists of 16 bits. Because one register has only 8 bits, one command requires two I^2C register addresses. In order to reduce program load time the LP5562 supports address auto increment. Register address is incremented after each 8 data bits. The whole program memory can be written in one I^2C write sequence. Program memory is defined in the LP5562 register table, from address 10h to address 2Fh for engine 1, from address 30h to address 4Fh for engine 2, and from address 50h to address 6Fh for engine 3. In order to access program memory at least one channel operation mode needs to be *load program*.
  - SRAM memory writes are allowed only to the channel in *load program* mode. All engines are in hold while one or several engines are in *load program* mode, and PWM values are frozen for the engines which are not in *load program*mode. Program execution continues when all engines are out of *load program* mode. *Load program* mode resets respective engine's Program Counter (PC).
- ***Run program***
  - *Run program* mode executes the commands defined in program memory for respective engine (1, 2, 3). Execution register bits in ENABLE register (00h) define how the program is executed. The program start position can be programmed to Program Counter register (see Table 8). By manually selecting the PC start value, user can write different lighting sequences to the SRAM memory, and select appropriate sequence with the PC register. If program counter runs to end (15), next command will be executed from program location 0. If internal clock is used in the *run program* mode, operation mode needs to be written disabled (00b) before disabling the chip (with CHIP_EN bit or EN pin) to ensure that the sequence starts

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from the correct program counter (PC) value when restarting the sequence. PC registers are synchronized to 32 kHz clock. Delay between consecutive I^2C writes to Program Counter (PC) registers (09h, 0Ah, 0Bh) need to be longer than 153µs (typ.).

- Execution registers are synchronized to 32kHz clock. Delay between consecutive I^2C writes to ENABLE register (00h) need to be longer than 488µs (typ.).
- Note that entering LOAD program or Direct Control Mode from RUN PROGRAM mode is not allowed. Engine execution mode should be set to Hold, and Operation Mode to disabled, when changing operation mode from RUN mode.

- ***Direct control***
  - In *Direct control* mode the engine PWM output is controlled by R, G and B PWM I^2C registers.
  - When engine 1 is in *Direct control* mode, the engine 1 PWM output is controlled by B PWM I^2C register (02h).
  - When engine 2 is in *Direct control* mode, the engine 2 PWM output is controlled by G PWM I^2C register (03h).
  - When engine 3 is in *Direct control* mode, the engine 3 PWM output is controlled by R PWM I^2C register (04h).

Program Execution Engine Program Counter (PC)

Program execution engine Program Counter tells the current program code command, which engine is executing. By setting the program counter value before starting the engine execution, user can set the starting point of the program execution.

Table 8. Engine1 PC Register (09h), Engine2 PC Register (0Ah), Engine3 PC Register (0Bh)

Name	Bit	Description
PC	3:0	Program counter value from 0 to 15d

Program Execution Engine Programming Commands

The LP5562 has three independent programmable engines (1, 2, 3). Trigger connections between engines are common for all engines. All engines have own program memory sections for storing LED lighting patterns. Brightness control and patterns are done with 8-bit PWM control (256 steps) to get accurate and smooth color control. Program execution is timed with 32.7 kHz clock. This clock can be generated internally or an external 32kHz clock can be connected to the CLK_32K pin. Using an external clock enables synchronization of LED timing to this clock rather than an internal clock. Selection of the clock is made with address 08H bits INT_CLK_EN and CLK_DET_EN. See External Clock for details. Supported commands are listed in the table below.

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Table 9. LED Controller Programming Commands(1)

Command	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RampWait	0	Pre-scale	Step time						Sign	Increment (number of steps)						
Set PWM	0	1	0						PWM Value							
Go to Start	0	0	0						0	0	0	0	0	0	0	0
Branch	1	0	1	Loop count						x	Step / command number					
End	1	1	0	Int	Reset	X										
Trigger	1	1	1	X	X	X	Wait for trigger on engines 1, 2, 3			X	X	X	Send trigger to engines 1,2, 3			X

(1) X means do not care whether 1 or 0.

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Ramp/Wait

The ramp command generates a PWM ramp starting from current value. At each ramp step the output is incremented by one. Time for one step is defined with Prescale and Step time bits. Minimum time for one step is 0.49 ms and maximum time is 63 x 15.6 ms = 1 second/step, so it is possible to program very fast and also very slow ramps. Increment value defines how many steps are taken in one command. Number of actual steps is Increment + 1. Maximum value is 127d, which corresponds to half of full scale (128 steps). If during ramp command PWM reaches minimum/maximum (0/255) ramp command will be executed to the end and PWM will stay at minimum/maximum. This enables the ramp command to be used as combined ramp and wait command in a single instruction.

The ramp command can be used as wait instruction when increment is zero.

Setting register 00h bit LOG_EN sets the scale as either linear to logarithmic. When LOG_EN = 0, linear scale is used, and when LOG_EN = 1, logarithmic scale is used. By using logarithmic scale the visual effect of the ramp command seems linear to the eye.

Table 10. Ramp/Wait Command

Ramp/Wait command															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pre-scale	Step time						Sign	Increment						

Table 11. Ramp/Wait Command Bits

Name	Value(d)	Description
Prescale	0	Divides master clock (32.768 Hz) by 16 = 2048 Hz, 0.49 ms cycle time
	1	Divides master clock (32.768 Hz) by 512 = 64 Hz, 15.6 ms cycle time
Step time	1-63	One ramp increment done in (step time) x (clock after prescale) Note: 0 means set PMW command.
Sign	0	Increase PWM output
	1	Decrease PWM output
Increment	0-127	The number of steps is Increment + 1. Note: 0 is a wait instruction.

Application Example:

For example if following parameters are used for ramp:

- Prescale = 1 => cycle time = 15.6 ms
- Step time = 2 => time = 15.6 ms x 2 = 31.2 ms
- Sign = 0 => rising ramp Increment = 4 => 5 cycles

Ramp command will be: 0100 0010 0000 0100b = 4204h

If current PWM value is 3, and the first command is as described above, the next command is a ramp with otherwise same the parameters, but with Sign = 1 (Command = 4284h), the result will be like in the following figure:

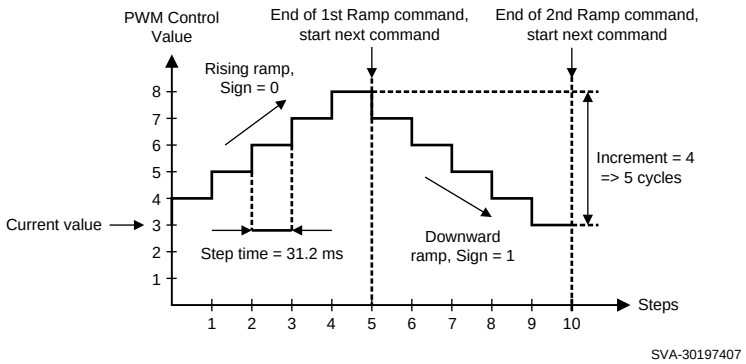

Figure 18. Example of 2 sequential ramp commands

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Set PWM

Set PWM output value from 0 to 255. Command takes sixteen 32 kHz clock cycles (= 488 µs). Setting register 00h bit LOG_EN sets the scale from linear to logarithmic.

Table 12. Set PWM command bits

Set PWM command															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0	PWM value							

Go-to-Start

Go-to-start command resets the Program Counter register and continues executing program from the 00h location. Command takes sixteen 32 kHz clock cycles. Note that default value for all program memory registers is 0000h, which is Go-to-Start command.

Table 13. Go-to-Start Command Bits

Go-to-Start command															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Branch

When branch command is executed, the 'step number' value is loaded to PC, and program execution continues from this location. Looping is done by the number defined in loop count parameter. Nested looping is supported (loop inside loop). The number of nested loops is not limited. Command takes sixteen 32 kHz clock cycles.

Table 14. Branch Command (1)

Branch command															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	Loop count						X	X	X	Step number			

(1) X means do not care whether 1 or 0

Table 15. Branch Command Bits

Name	Value(d)	Description
loop count	0-63	The number of loops to be done. 0 means infinite loop.
step number	0-15	The step number to be loaded to program counter.

End

End program execution resets the program counter and sets the corresponding EXEC register to 00b (hold). Command takes sixteen 32 kHz clock cycles.

Table 16. End Command (1)

End command															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	int	reset	X	X	X	X	X	X	X	X	X	X	X

(1) X means do not care whether 1 or 0.

Table 17. End Command Bits

Name	Value	Description
int	0	No interrupt will be sent.
	1	Send interrupt by setting corresponding status register bit high to notify that program has ended. Interrupt can only be cleared by reading interrupt status register 0Ch.

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Table 17. End Command Bits (continued)

Name	Value	Description
reset	0	Keep the current PWM value.
	1	Set PWM value to 0.

Trigger

Wait or send triggers can be used to synchronize operation between different engines. The send-trigger command takes sixteen 32 kHz clock cycles; the wait-for-trigger command takes at least sixteen 32 kHz clock cycles. The receiving engine stores sent triggers. Received triggers are cleared by wait for trigger command if received triggers match to engines defined in the command. Engine waits until all defined triggers have been received.

Table 18. Trigger Command(1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	X	X	X	wait trigger <2:0>			X	X	X	send trigger <2:0>			X
						ENG3	ENG2	ENG1				ENG3	ENG2	ENG1	

(1) X means do not care whether 1 or 0.

Table 19. Trigger Command Bits

Name	Value(d)	Description
wait trigger<2:0>	0-7	Wait for trigger for the engine(s) defined. Several triggers can be defined in the same command. Bit 0 is engine 1, bit 1 is engine2, bit 2 is engine 3.
send trigger<2:0>	0-7	Send trigger for the engine(s) defined. Several triggers can be defined in the same command. Bit 0 is engine 1, bit 1 is engine2, bit 2 is engine 3.

Program Load and Execution Example

- Start up device and configure device to SRAM write mode
  - Supply 3.6V to VDD
  - Supply 1.8V to EN
  - Wait 1 ms
  - Generate 32 kHz clock to CLK_32K pin
  - Write to address 00h 0100 0000b (enable device)
  - Wait 500 µs (startup delay)
  - Write to address 01h 0001 0000b (configure engine 1 into 'Load program to SRAM' mode)
- Program load to SRAM
  - Write to address 10h 0000 0011b (1st ramp command 8MSB)
  - Write to address 11h 0111 1111b (1st ramp command 8 LSB)
  - Write to address 12h 0100 1101b (1st wait command 8 MSB)
  - Write to address 13h 0000 0000b (1st wait command 8 LSB)
  - Write to address 14h 0000 0011b (2nd ramp command 8 MSB)
  - Write to address 15h 1111 1111b (2nd ramp command 8 LSB)
  - Write to address 16h 0110 0000b (2nd wait command 8 MSB)
  - Write to address 17h 0000 0000b (2nd wait command 8 LSB)
- Enable Power Save and use external 32 kHz clock
  - Write to address 08h 0010 0000b (enable powersave, use external clock)
- Run program
  - Write to address 01h 0010 0000b (Configure LED controller operation mode to "Run program" in engine 1)
  - Write to address 00h 0110 0000b (Configure program execution mode from "Hold" to "Run" in engine 1)

The LP5562 will generate a 1100 ms long LED pattern which will be repeated infinitely. The LED pattern is illustrated in the figure below.

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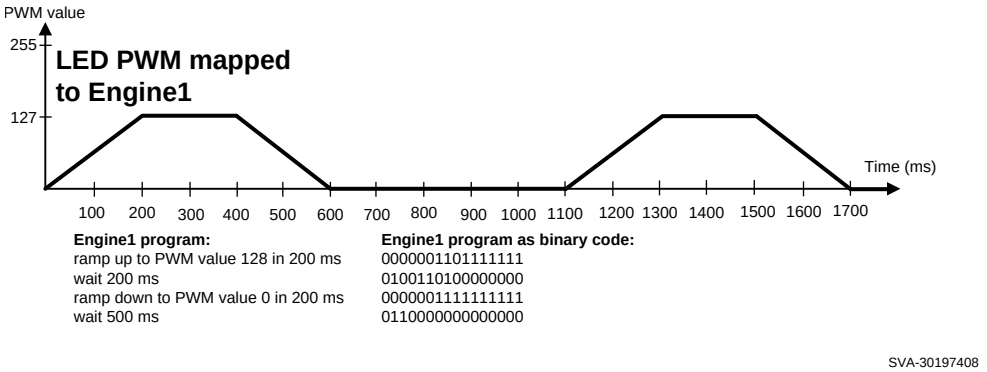

Figure 19. LED Lighting Pattern and Code for Program Load and Execution Example

SRAM Memory

In the LP5562 there is a SRAM memory reserved for storing the LED lighting programs. Each engine has its own section of the memory so that engine 1 has registers 10h to 2Fh, engine 2 has registers 30h to 4Fh, and engine 3 has registers 50h to 6Fh. For each engine 16 engine commands (16-bit) can be stored. Each 16-bit command takes up two I^2C registers.

Table 20. SRAM Memory Registers

Address	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	Prog mem ENG1	COMMAND1_ENG1[15:8]							
11h	Prog mem ENG1	COMMAND1_ENG1[7:0]							
...									
2Eh	Prog mem ENG1	COMMAND16_ENG1[15:8]							
2Fh	Prog mem ENG1	COMMAND16_ENG1[7:0]							
30h	Prog mem ENG2	COMMAND1_ENG2[15:8]							
31h	Prog mem ENG2	COMMAND1_ENG2[7:0]							
...									
4Eh	Prog mem ENG2	COMMAND16_ENG2[15:8]							
4Fh	Prog mem ENG2	COMMAND16_ENG2[7:0]							
50h	Prog mem ENG3	COMMAND1_ENG3[15:8]							
51h	Prog mem ENG3	COMMAND1_ENG3[7:0]							
...									
6Eh	Prog mem ENG3	COMMAND16_ENG3[15:8]							
6Fh	Prog mem ENG3	COMMAND16_ENG3[7:0]							

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When downloading a program to the SRAM engine modes need to be set to Load mode (see Table 6). While loading sequential I^2C writing can be used (repeated start see Figure 25). However, please note that sequential read of the SRAM is not possible.

Power Save Mode

Automatic power save mode is enabled when the PS_EN bit in register address 08h is 1. Almost all analog blocks are powered down in power save, if an external clock is used. However, if an internal clock has been selected, only the LED drivers are disabled during power save since the digital part of the LED controller need to remain active. During program execution the LP5562 can enter power-save mode if there is no PWM activity in engine controlled outputs. To prevent short power-save sequences during program execution, the LP5562 has a command look-ahead filter. In each instruction cycle every engine commands are analyzed, and if there is sufficient time left with no PWM activity, the device will enter power save. In power save program execution continues uninterruptedly. When a command that requires PWM activity is executed, fast internal startup sequence will be started automatically. The following tables describe commands and conditions that can activate power save. All engines need to meet power-save conditions in order to enable power save.

Table 21. Engine Operation Mode and Power Save

Engine operation mode	Power save condition
00b	Disabled mode enables power save
01b	Load program to SRAM mode prevents power save.
10b	Run program mode enables power save if there is no PWM activity and command look-ahead filter condition is met.
11b	Direct control mode enables power save if there is no PWM activity.

Table 22. Engine Commands and Power Save

Command	Power save condition
Wait	No PWM activity and current command wait time longer than 50 ms. If prescale = 1 then wait time needs to be longer than 80 ms.
Ramp	Ramp Command PWM value reaches minimum 0 and current command execution time left more than 50 ms. If prescale = 1 then time left needs to be more than 80 ms.
Trigger	No PWM activity during wait for trigger command execution.
End	No PWM activity or Reset bit = 1.
Set PWM	Enables power save if PWM set to 0 and next command generates at least 50 ms wait.
Other commands	No effect to power save.

External Clock

The presence of an external clock can be detected by the LP5562. Program execution is clocked with an internal 32 kHz clock or with an external clock. Clocking is controlled with register address 08h bits, INT_CLK_EN, and CLK_DET_EN as seen in Table 23.

An external clock can be used if clock is present at the CLK_32K pin. The external clock frequency must be 32 kHz for the program execution PWM timing to be as specified. If higher or lower frequency is used, it will affect the program engine execution speed. If a clock frequency other than 32kHz is used, the program execution timings must be scaled accordingly.

LP5562 has automatic external clock detection. The external clock detector block only detects too low clock frequency (<4 kHz), but it is recommended not to use external clock below 20kHz. If external clock frequency is higher than specified, the external clock detector notifies that external clock is present. External clock status can be checked with read only bit EXT_CLK_USED in register address 0Ch, when the external clock detection is enabled (CLK_DET_EN bit = high). If EXT_CLK_USED = 1, then the external clock is detected and it is used for timing, if automatic clock selection is enabled.

If an external clock is stuck-at-zero or stuck-at-one, or the clock frequency is too low, the clock detector indicates that external clock is not present.

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If an external clock is not used on the application, CLK_32K pin should be connected to GND to prevent floating of this pin and extra current consumption.

Table 23. CONFIG Register (08h)

Name	Bit	Description
CLK_DET_EN, INT_CLK_EN	1:0	LED Controller clock source 00b = External clock source (CLK_32K) 01b = Internal clock 10b = Automatic selection 11b = Internal clock

Thermal Shutdown

If the LP5562 reaches thermal shutdown temperature (150°C typically) the device operation is disabled and the device state is in STARTUP mode, until no thermal shutdown event is present. Device will enter Normal mode when temperature drops below 130°C (typically) degrees.

Fault is cleared when thermal shutdown disappears.

Logic Interface Operational Description

The LP5562 features a flexible logic interface for connecting to processor and peripheral devices. Communication is done with the I^2C-compatible interface, and different logic input/output pins makes it possible to synchronize operation of several devices.

IO Levels

I^2C interface, CLK_32K. ADDR_SEL0, and ADDR_SEL1 pins input levels are defined by voltage in EN pin. Using the EN pin as a voltage reference for logic inputs simplifies PCB routing and eliminates the need for a dedicated VIO pin. The following block diagram describes EN pin connections.

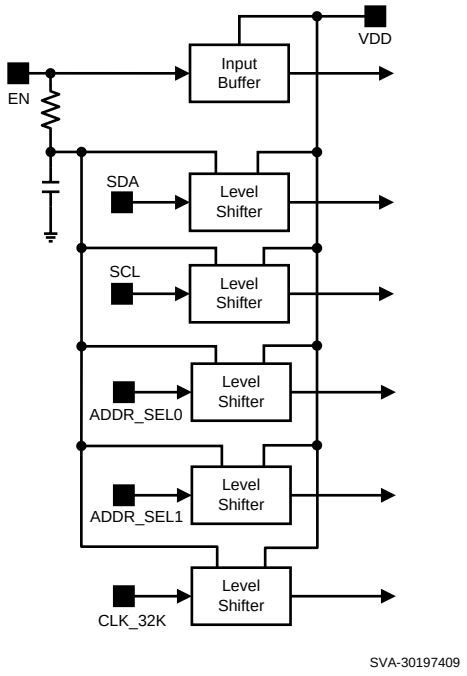

Figure 20. Using EN Pin as Digital IO Voltage Reference

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ADDR_SEL0, ADDR_SEL1 Pins

The ADDR_SEL0 and ADDR_SEL1 pins define the device I^2C address. Pins are referenced to EN pin signal level. See I^2C Addresses for I^2C address definitions.

CLK_32 Pin

The CLK_32K pin is used for connecting an external 32 kHz clock to LP5562. An external clock can be used to synchronize the sequence engines of several LP5562. Using an external clock can also improve automatic power save mode efficiency, because an internal clock can be switched off automatically when device has entered power-save mode, and an external clock is present. Device can be used without the external clock. If external clock is not used on the application, the CLK_32K pin should be connected to GND to prevent floating of this pin and extra current consumption.

I^2C-Compatible Serial Bus Interface

Interface Bus Overview

The I^2C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pullup resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

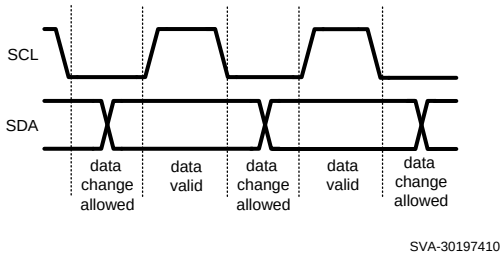

Figure 21. Data Validity

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

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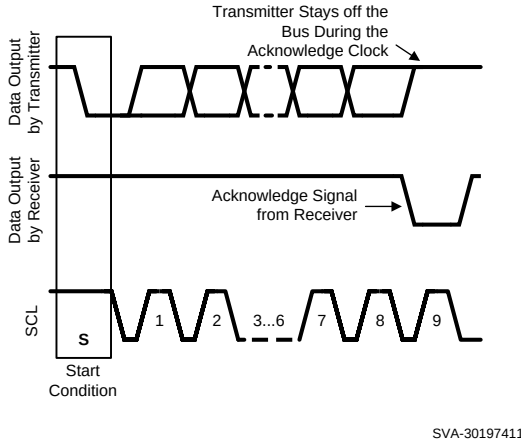

Figure 22. Acknowledge Signal

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

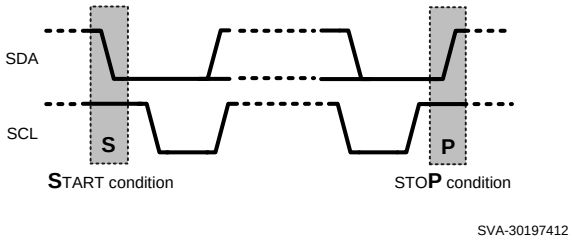

Figure 23. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

Acknowledge After Every Byte Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the “acknowledge after every byte” rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

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Addressing Transfer Formats

Each device on the bus has a unique slave address. The LP5562 operates as a slave device with the 7-bit address. LP5562 I^2C address is pin selectable from four different choices. If 8-bit address is used for programming, the 8th bit is 1 for read and 0 for write. In the following table is represented the 8-bit I^2C addresses.

Table 24. I^2C Addresses

ADDR_SEL [1:0]	I 2 C address write (8 bits)	I 2 C address read (8 bits)
00	0110 0000 = 60h	0110 0001 = 61h
01	0110 0010 = 62h	0110 0011 = 63h
10	0110 0100 = 64h	0110 0101 = 65h
11	0110 0110 = 66h	0110 0111 = 67h

Before any data is transmitted, the master transmits the address of the slave being addressed.

The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

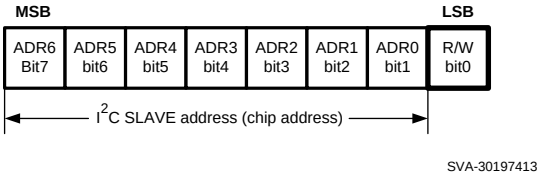

Figure 24. I^2C chip address

Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.

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- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

Table 25. I²C Data Read/Write Flow(1)

	Address Mode
Data Read	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = 1>[Ack] [Register Data]<Ack or NAck> ... additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w='0'>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] ... additional writes to subsequent register address possible <Stop Condition>

(1) <>Data from master [] Data from slave

Register Read/Write Format

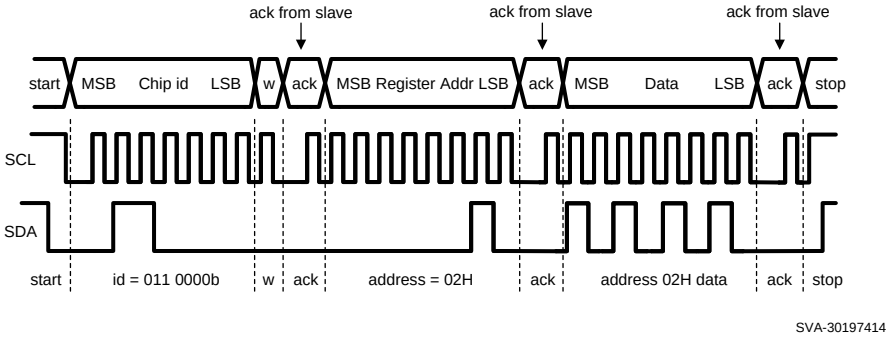

Figure 25. Register Write Format

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When a *read* function is to be accomplished, a *write* function must precede the *read* function, as show in the Read Cycle waveform

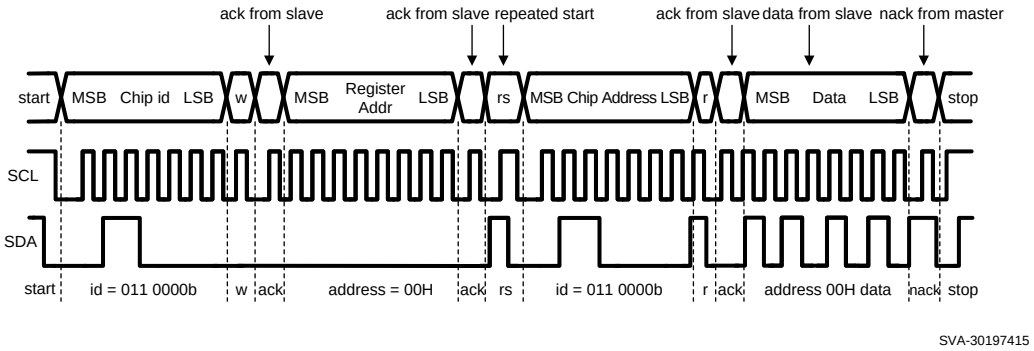

Figure 26. Register Read Format

w = write (SDA = 0)

r = read (SDA = 1)

ack = acknowledge (SDA pulled down by either master or slave)

rs = repeated start

id = 7-bit chip address

REGISTER TABLE

Table 26. LP5562 Control Register Names and Default Values

ADDR (HEX)	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00	ENABLE	LOG_EN	CHIP_EN	ENG1_EXEC[1:0]		ENG2_EXEC[1:0]		ENG3_EXEC[1:0]		0000 0000
01	OP MODE			ENG1_MODE[1:0]		ENG2_MODE[1:0]		ENG3_MODE[1:0]		0000 0000
02	B PWM	B_PWM[7:0]								0000 0000
03	G PWM	G_PWM[7:0]								0000 0000
04	R PWM	R_PWM[7:0]								0000 0000
05	B CURRENT	B_CURRENT[7:0]								1010 1111
06	G CURRENT	G_CURRENT[7:0]								1010 1111
07	R CURRENT	R_CURRENT[7:0]								1010 1111
08	CONFIG		PWM_HF	PS_EN				CLK_DET_EN	INT_CLK_EN	0000 0000
09	ENG1 PC					ENG1_PC[3:0]				0000 0000
0A	ENG2 PC					ENG2_PC[3:0]				0000 0000
0B	ENG3 PC					ENG3_PC[3:0]				0000 0000
0C	STATUS					EXT_CLK_USED	ENG1_INT	ENG2_INT	ENG3_INT	0000 0000
0D	RESET	RESET[7:0]								0000 0000
0E	W PWM	W_PWM[7:0]								00000000
0F	W CURRENT	W_CURRENT[7:0]								10101111
70	LED MAP	W_ENG_SEL		R_ENG_SEL		G_ENG_SEL		B_ENG_SEL		00111001
10	PROG MEM ENG1	CMD_1_ENG1[15:8]								0000 0000
11	PROG MEM ENG1	CMD_1_ENG1[7:0]								0000 0000
...										
2E	PROG MEM ENG1	CMD_16_ENG1[15:8]								0000 0000
2F	PROG MEM ENG1	CMD_16_ENG1[7:0]								0000 0000
30	PROG MEM ENG2	CMD_1_ENG2[15:8]								0000 0000
31	PROG MEM ENG2	CMD_1_ENG2[7:0]								0000 0000
...										
4E	PROG MEM ENG2	CMD_16_ENG2[15:8]								0000 0000
4F	PROG MEM ENG2	CMD_16_ENG2[7:0]								0000 0000
50	PROG MEM ENG3	CMD_1_ENG3[15:8]								0000 0000

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Table 26. LP5562 Control Register Names and Default Values (continued)

ADDR (HEX)	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
51	PROG MEM ENG3	CMD_1_ENG3[7:0]								0000 0000
...										
6E	PROG MEM ENG3	CMD_16_ENG3[15:8]								0000 0000
6F	PROG MEM ENG3	CMD_16_ENG3[7:0]								0000 0000

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REGISTER DETAILS

Enable Register (Enable)

Address 00h

Reset value 00h

Table 27. Enable Register

7	6	5	4	3	2	1	0
LOG_EN	CHIP_EN	ENG1_EXEC[1:0]		ENG2_EXEC[1:0]		ENG3_EXEC[1:0]	

Table 28. Enable Register Detailed Description

Name	Bit	Access	Active	Description
LOG_EN	7	R/W	High	Logarithmic PWM adjustment generation enable
CHIP_EN	6	R/W	High	Master chip enable. Enables device internal startup sequence. See MODES OF OPERATION for further information. Setting EN pin low resets the CHIP_EN state to 0. Allow 500 µs delay after setting chip_en bit to '1'
ENG1_EXEC	5:4	R/W		Engine 1 program execution. **00b** = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode. **01b** = Step: Execute instruction defined by current engine 1 PC value, increment PC and change ENG1_EXEC to 00b (Hold) **10b** = Run: Start at program counter value defined by current engine 1 PC value **11b** = Execute instruction defined by current engine 1 PC value and change ENG1_EXEC to 00b (Hold)
ENG2_EXEC	3:2	R/W		Engine 2 program execution **00b** = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode. **01b** = Step: Execute instruction defined by current engine 2 PC value, increment PC and change ENG2_EXEC to 00b (Hold) **10b** = Run: Start at program counter value defined by current engine 2 PC value **11b** = Execute instruction defined by current engine 2 PC value and change ENG2_EXEC to 00b (Hold)
ENG3_EXEC	1:0	R/W		Engine 3 program execution **00b** = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode. **01b** = Step: Execute instruction defined by current engine 3 PC value, increment PC and change ENG3_EXEC to 00b (Hold) **10b** = Run: Start at program counter value defined by current engine 3 PC value **11b** = Execute instruction defined by current engine 3 PC value and change ENG3_EXEC to 00b (Hold)

EXEC registers are synchronized to the 32 kHz clock. Delay between consecutive I^2C writes to ENABLE register (00h) need to be longer than 488 µs (typ).

Operation Mode Register (OP MODE)

Address 01h

Reset Value 00h

Table 29. OP Mode Register

7	6	5	4	3	2	1	0
		ENG1_MODE[1:0]		ENG1_MODE[1:0]		ENG1_MODE[1:0]	

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Table 30. OP Mode Register Detailed Description

Name	Bit	Access	Active	Description
ENG1_MODE	5:4	R/W		Engine 1 operation mode 00b = Disabled 01b = Load program to SRAM, reset engine 1 PC 10b = Run program defined by ENG1_EXEC 11b = Direct control
ENG2_MODE	3:2	R/W		Engine 2 operation mode 00b = Disabled 01b = Load program to SRAM, reset engine 2 PC 10b = Run program defined by ENG2_EXEC 11b = Direct control
ENG3_MODE	1:0	R/W		Engine 3 operation mode 00b = Disabled 01b = Load program to SRAM, reset engine 3 PC 10b = Run program defined by ENG3_EXEC 11b = Direct control

MODE registers are synchronized to 32 kHz clock. Delay between consecutive I^2C writes to OP_MODE register (01h) need to be longer than 153 µs (typ).

B LED Output PWM Control Register (B_PWM)

Address 02h

Reset value 00h

Table 31. B PWM Register

7	6	5	4	3	2	1	0
B_PWM[7:0]							

Table 32. B PWM Register Detailed Description

Name	Bit	Access	Active	Description
B_PWM	7:0	R/W		B LED output PWM value during direct control operation mode

G LED Output PWM Control Register (G_PWM)

Address 03h

Reset value 00h

Table 33. G PWM Register

7	6	5	4	3	2	1	0
G_PWM[7:0]							

Table 34. G PWM Register Detailed Description

Name	Bit	Access	Active	Description
G_PWM	7:0	R/W		G LED output PWM value during direct control operation mode

R LED Output PWM Control Register (R_PWM)

Address 04h

Reset value 00h

Table 35. R PWM Register

7	6	5	4	3	2	1	0
R_PWM[7:0]							

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Table 36. R PWM Register Detailed Description

Name	Bit	Access	Active	Description
R_PWM	7:0	R/W		R LED output PWM value during direct control operation mode

B LED Output Current Control Register (B_CURRENT)

Address 05h

Reset Value AFh

Table 37. B CURRENT Register

7	6	5	4	3	2	1	0
B_CURRENT[7:0]							

Table 38. B CURRENT Register Detailed Description

Name	Bit	Access	Active	Description
B_CURRENT	7:0	R/W		Current setting 0000 0000b = 0.0 mA 0000 0001b = 0.1 mA 0000 0010b = 0.2 mA 0000 0011b = 0.3 mA 0000 0100b = 0.4 mA 0000 0101b = 0.5 mA 0000 0110b = 0.6 mA ... **1010 1111b = 17.5 mA (default)** ... 1111 1011b = 25.1 mA 1111 1100b = 25.2 mA 1111 1101b = 25.3 mA 1111 1110b = 25.4 mA 1111 1111b = 25.5 mA

G LED Output Current Control Register (G_CURRENT)

Address 06h

Reset Value AFh

Table 39. G CURRENT Register

7	6	5	4	3	2	1	0
G_CURRENT[7:0]							

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Table 40. G CURRENT Register Detailed Description

Name	Bit	Access	Active	Description
G_CURRENT	7:0	R/W		Current setting 0000 0000b = 0.0 mA 0000 0001b = 0.1 mA 0000 0010b = 0.2 mA 0000 0011b = 0.3 mA 0000 0100b = 0.4 mA 0000 0101b = 0.5 mA 0000 0110b = 0.6 mA ... **1010 1111b = 17.5 mA (default)** ... 1111 1011b = 25.1 mA 1111 1100b = 25.2 mA 1111 1101b = 25.3 mA 1111 1110b = 25.4 mA 1111 1111b = 25.5 mA

R LED Output Current Control Register (R_CURRENT)

Address 07h

Reset Value AFh

Table 41. R CURRENT Register

7	6	5	4	3	2	1	0
R_CURRENT[7:0]							

Table 42. R CURRENT Register Detailed Description

Name	Bit	Access	Active	Description
R_CURRENT	7:0	R/W		Current setting 0000 0000b = 0.0 mA 0000 0001b = 0.1 mA 0000 0010b = 0.2 mA 0000 0011b = 0.3 mA 0000 0100b = 0.4 mA 0000 0101b = 0.5 mA 0000 0110b = 0.6 mA ... **1010 1111b = 17.5 mA (default)** ... 1111 1011b = 25.1 mA 1111 1100b = 25.2 mA 1111 1101b = 25.3 mA 1111 1110b = 25.4 mA 1111 1111b = 25.5 mA

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Configuration Control Register (CONFIG)

Address 08h

Reset value 00h

Table 43. CONFIG Register

7	6	5	4	3	2	1	0
	PWM_HF	PS_EN				CLK_DET_EN	INT_CLK_EN

Table 44. CONFIG Register Detailed Description

Name	Bit	Access	Active	Description
PWM_HF	6	R/W	High	PWM clock 0 = 256 Hz PWM clock used 1 = 558 Hz PWM clock used
PWRSAVE_EN	5	R/W	High	Power save mode enable
CLK_DET_EN, INT_CLK_EN	1:0	R/W		LED Controller clock source 00b = External clock source (CLK_32K) 01b = Internal clock 10b = Automatic selection 11b = Internal clock

Engine 1 Program Counter Value Register (Engine 1 PC)

Address 09h

Reset value 00h

Table 45. Engine 1 PC Register

7	6	5	4	3	2	1	0
				ENG1_PC[3:0]			

Table 46. Engine 1 PC Register Detailed Description

Name	Bit	Access	Active	Description
ENG1_PC	3:0	R/W		Engine 1 program counter value

PC registers are synchronized to 32 kHz clock. Delay between consecutive I^2C writes to PC registers needs to be longer than 153 µs (typ.). PC register can be read or written only when EXEC mode is *hold*.

Engine 2 Program Counter Value Register (Engine 2 PC)

Address 0Ah

Reset value 00h

Table 47. Engine 2 PC Register

7	6	5	4	3	2	1	0
				ENG2_PC[3:0]			

Table 48. Engine 2 PC Register Detailed Description

Name	Bit	Access	Active	Description
ENG2_PC	3:0	R/W		Engine 2 program counter value

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PC registers are synchronized to 32 kHz clock. Delay between consecutive I^2C writes to PC registers needs to be longer than 153 µs (typ.). PC register can be read or written only when EXEC mode is *hold*.

Engine 3 Program Counter Value Register (Engine 3 PC)

Address 0Ah

Reset value 00h

Table 49. Engine 3 PC Register

7	6	5	4	3	2	1	0
				ENG3_PC[3:0]			

Table 50. Engine 3 PC Register Detailed Description

Name	Bit	Access	Active	Description
ENG3_PC	3:0	R/W		Engine 3 program counter value

PC registers are synchronized to 32 kHz clock. Delay between consecutive I^2C writes to PC registers needs to be longer than 153 µs (typ.). PC register can be read or written only when EXEC mode is *hold*.

STATUS/INTERRUPT Register

Address 0Ch

Reset value 00h

Table 51. STATUS/INTERRUPT Register

7	6	5	4	3	2	1	0
				EXT_CLK USED	ENG1_INT	ENG2_INT	ENG3_INT

Table 52. STATUS/INTERRUPT Register Detailed Description

Name	Bit	Access	Active	Description
EXT_CLK USED	3	R		External clock state 0 = Internal clock used 1 = External 32kHz clock used
ENG1_INT	2	R	High	Interrupt from engine 1
ENG2_INT	1	R	High	Interrupt from engine 2
ENG3_INT	0	R	High	Interrupt from engine 3

Note: Register INT bits will be cleared when read operation to Status/Interrupt register occurs.

RESET Register

Address 0Dh

Reset value 00h

Table 53. RESET Register

7	6	5	4	3	2	1	0
RESET[7:0]							

Table 54. RESET Register Detailed Description

Name	Bit	Access	Active	Description
RESET	7:0	W		Reset all register values when FFh is written.

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WLED Output PWM Control Register (W_PWM)

Address 0Eh

Reset value 00h

Table 55. W PWM Register

7	6	5	4	3	2	1	0
W_PWM[7:0]							

Table 56. W PWM Register Detailed Description

Name	Bit(s)	Access	Active	Description
W_PWM	7:0	R/W		W LED Output PWM value during direct control operation mode

W LED Output Current Control Register (W_CURRENT)

Address 0Fh

Reset Value AFh

Table 57. W CURRENT Register

7	6	5	4	3	2	1	0
W_CURRENT[7:0]							

Table 58. W CURRENT Register Detailed Description

Name	Bit(s)	Access	Active	Description
W_CURRENT	7:0	R/W		Current setting 0000 0000b = 0.0 mA 0000 0001b = 0.1 mA 0000 0010b = 0.2 mA 0000 0011b = 0.3 mA 0000 0100b = 0.4 mA 0000 0101b = 0.5 mA 0000 0110b = 0.6 mA ... **1010 1111b = 17.5 mA (default)** ... 1111 1011b = 25.1 mA 1111 1100b = 25.2 mA 1111 1101b = 25.3 mA 1111 1110b = 25.4 mA 1111 1111b = 25.5 mA

LED Mapping Register (LED Map)

Address 70h

Reset value 39h

Table 59. LED MAP Register

7	6	5	4	3	2	1	0
W_ENG_SEL[1:0]		R_ENG_SEL[1:0]		G_ENG_SEL[1:0]		B_ENG_SEL[1:0]	

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Table 60. LED MAP Register Detailed Description

Name	Bit(s)	Access	Active	Description
W_ENG_SEL	7:6	R/W		Selection from where W LED output PWM is controlled, 00 = I^2C register 0Eh, 01 = Engine 1, 10 = Engine 2, 11 = Engine 3
R_ENG_SEL	5:4	R/W		Selection from where R LED output PWM is controlled 00 = I^2C register 04h, 01 = Engine 1, 10 = Engine 2, 11 = Engine 3
G_ENG_SEL	3:2	R/W		Selection from where G LED output PWM is controlled 00 = I^2C register 03h, 01 = Engine 1, 10 = Engine 2, 11 = Engine 3
B_ENG_SEL	1:0	R/W		Selection from where B LED output PWM is controlled 00 = I^2C register 02h, 01 = Engine 1, 10 = Engine 2, 11 = Engine 3

PROGRAM MEMORY

Address 10h – 6Fh

Reset values 00h

See chapter SRAM Memory for further information.

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Table 61. Program Execution Engine Commands

Command	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RampWait	0	Pre-scale	Step time						Sign	Increment						
Set PWM	0	1	0						PWM Value							
Go toStart	0	0	0						0	0	0	0	0	0	0	0
Branch	1	0	1	Loop Count						X	Step number					
End	1	1	0	Int	Reset	X										
Trigger	1	1	1	Wait for trigger on channels 5-0						Send trigger on channels 5-0						X

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LIST OF RECOMMENDED EXTERNAL COMPONENTS

Table 62. Recommended External Components

Model	Type	Vendor	Voltage Rating	Size inch (mm)
1 µF for C_{IN}				
C1005X5R1A105K	Ceramic X5R	TDK	10V	0402 (1005)
GRM155R61A105KE15D	Ceramic X5R	Murata	10V	0402 (1005)
LEDs	User Defined			

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP5562TME/NOPB	Active	Production	DSBGA (YQE) | 12	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D5
LP5562TMX/NOPB	Active	Production	DSBGA (YQE) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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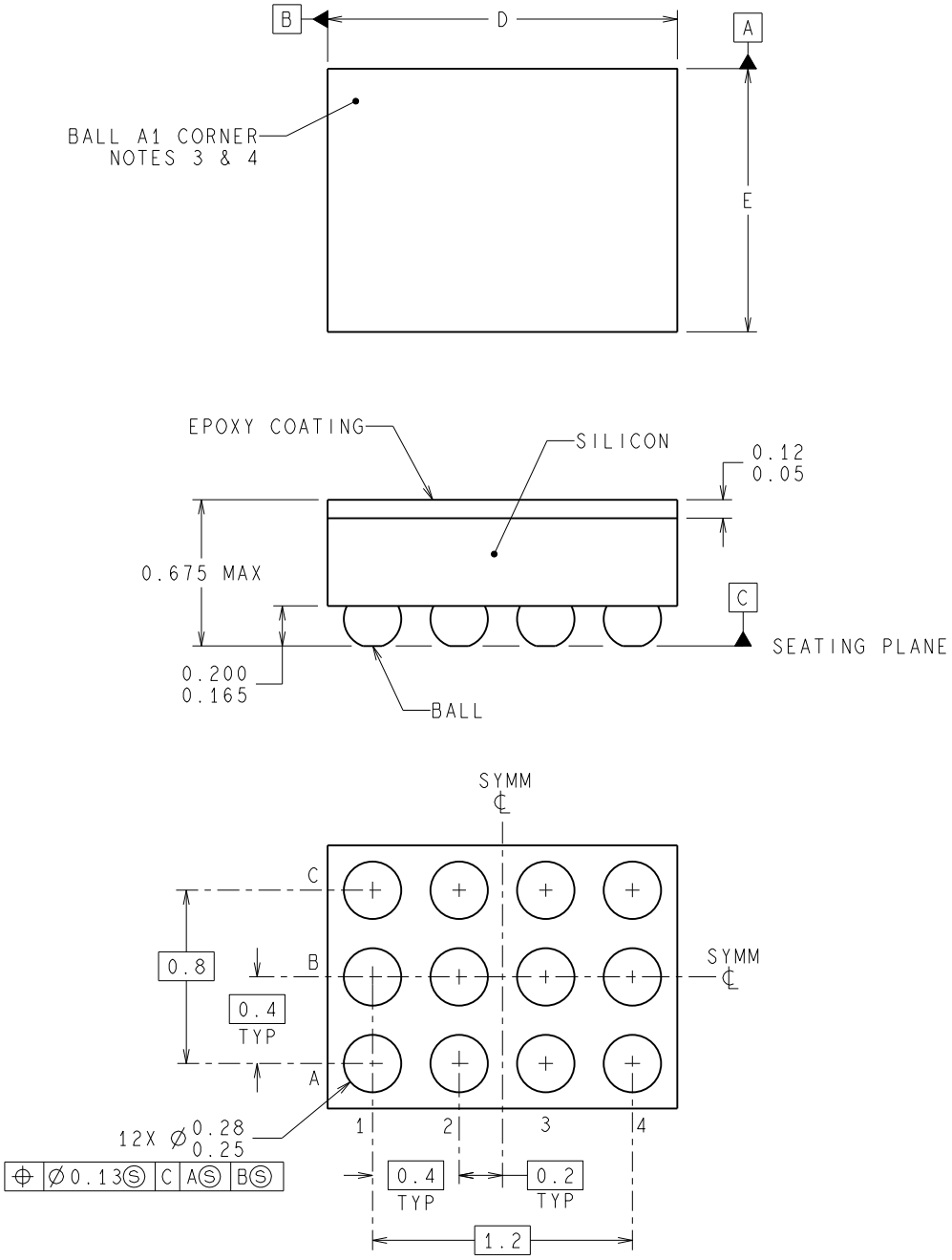
YQE0012

DSBGA - 0.675mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



4218314/A 02/2013

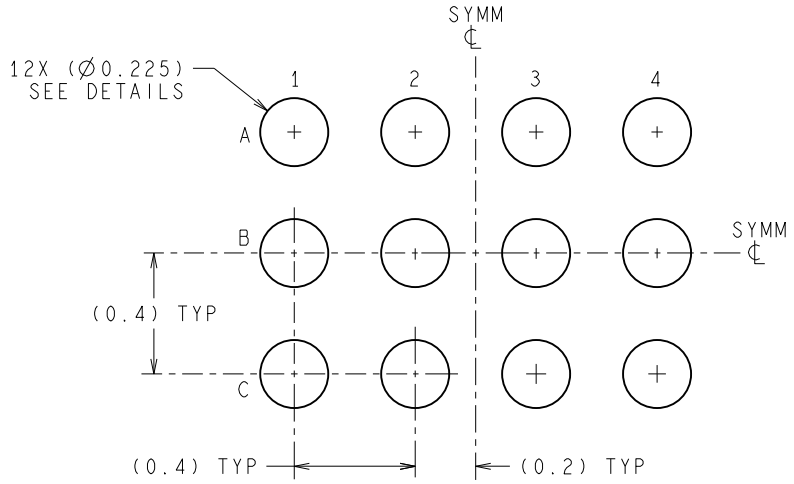
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN PARENTHESIS ARE FOR REFERENCE ONLY.
2. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
3. BALL A1 IS ESTABLISHED BY UPPER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION.
4. COLUMNS NOT ORIENTED PER STANDARD CONFIGURATION.

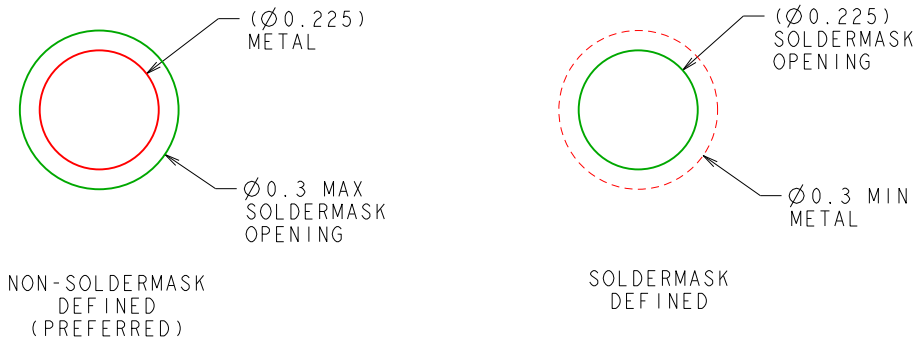
YQE0012

DSBGA - 0.675mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDERMASK DETAILS
NOT TO SCALE

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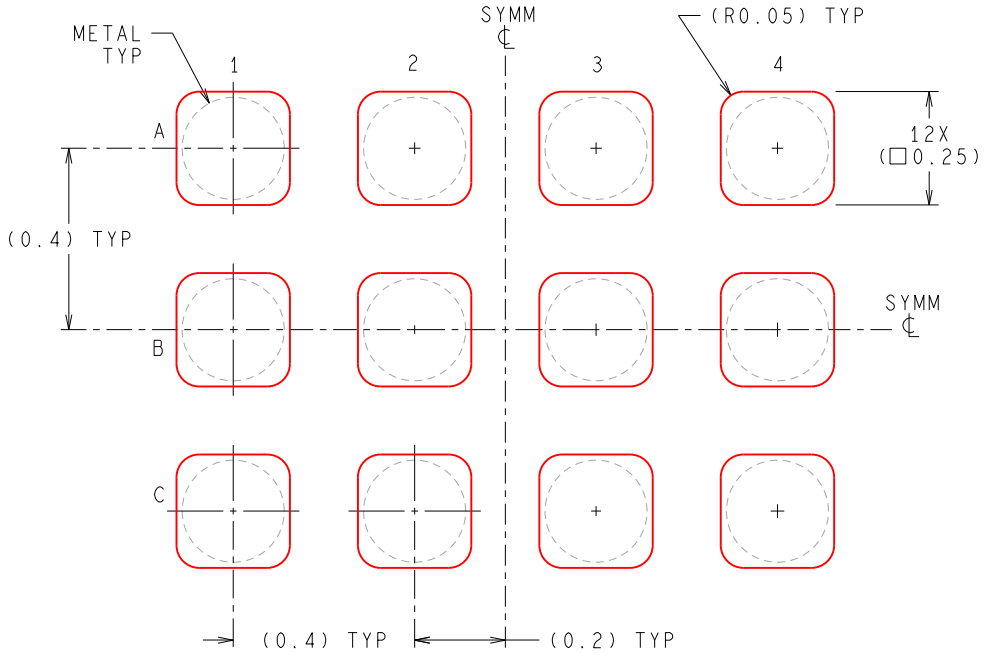
YQE0012

DSBGA - 0.675mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



SOLDERPASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL
SCALE:60X

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NOTES: (CONTINUED)

5. LASER CUT APERTURES WITH TRAPEZOIDAL WALLS AND ROUNDED CORNERS WILL OFFER BETTER PASTE RELEASE. REFER TO IPC-7525 FOR DESIGN CONSIDERATIONS.
6. NO SHARP EDGES ON OPENINGS - ELECTROPOLISH OPTIONAL TO ACCOMPLISH THIS.

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