RoHS

COMPLIANT

HALOGEN

FREE

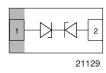
<u>GREEN</u>

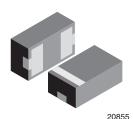


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Vishay Semiconductors

Bidirectional Symmetrical (BiSy) Low Capacitance, Single-Line ESD Protection Diode in LLP1006-2M





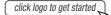
MARKING (example only)



Bar = pin 1 marking X = date code

Y = type code (see table below)

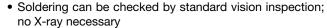
DESIGN SUPPORT TOOLS





FEATURES

- Ultra compact LLP1006-2M package
- Low package height < 0.4 mm
- 1-line ESD protection
- Working range ± 5.5 V
- Low leakage current I_R < 0.1 μA
- Very low load capacitance C_D = 0.3 pF
- ESD immunity acc. IEC 61000-4-2
- ± 15 kV contact discharge
- ± 16 kV air discharge



- Pin plating NiPdAu (e4) no whisker growth
- e4 precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- PATENT(S): www.vishav.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

ORDERING INFORMATION					
DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY		
VBUS05L1-DD1	VBUS05L1-DD1-G-08	8000	8000		

PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VBUS05L1-DD1	LLP1006-2M	R	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

ABSOLUTE MAXIMUM RATINGS VBUS05L1-DD1						
PARAMETER	TEST CONDITIONS	DITIONS SYMBOL		UNIT		
Peak pulse current	Acc. IEC 61000-4-5; $t_p = 8/20 \mu s$; single shot	I _{PPM}	2	Α		
Peak pulse power	Pin 1 to pin 2, acc. IEC 61000-4-5; $t_p = 8/20 \mu s$; single shot	P _{PP}	34	W		
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	\/	± 15	kV		
	Air discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 16	kV		
Operating temperature	Junction temperature	TJ	-40 to +125	°C		
Storage temperature		T _{STG}	-40 to +150	°C		

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.

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ELECTRICAL CHARACTERISTICS VBUS05L1-DD1 (T _{amb} = 25 °C, unless otherwise specified)							
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Protection paths	Number of lines which can be protected	N _{channel}	-	-	1	lines	
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	5.5	V	
Reverse voltage	at I _R = 0.05 μA	V _R	5.5	-	-	V	
Reverse current	at V _{RWM} = 5.5 V	I _R	-	-	0.05	μA	
Reverse breakdown voltage	at I _R = 1 mA	V_{BR}	7	8.4	9.5	V	
Reverse clamping voltage	at I _{PP} 1 A	V _C	-	11.5	14	V	
	at I _{PP} = I _{PPM} = 2 A	V _C	-	14	17	V	
Capacitance	at V _R = 0 V, f = 1 MHz	C _D	-	0.33	0.4	pF	
	at V _R = 2.5 V, f = 1 MHz	C _D	-	0.34	-	pF	

VBUS05L1-DD1: ESD PROTECTION WITH LOWEST LOAD CAPACITANCE

The VBUS05L1-DD1 is a bidirectional and symmetrical (BiSy) ESD protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VBUS05L1-DD1 offers a high isolation (low leakage current, lowest capacitance) within the specified working range. Due to the short leads and small package size of the tiny LLP1006-2M package the line inductance is very low, so that fast transients like an ESD strike can be clamped with minimal over- or undershoots.

TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

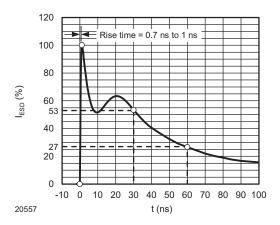


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω /150 pF)

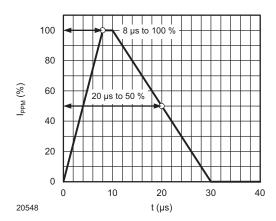


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

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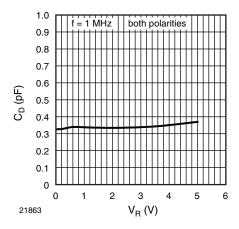


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

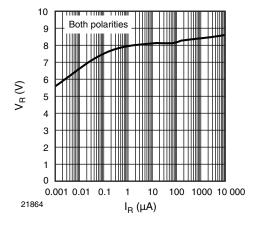


Fig. 4 - Typical Reverse Voltage V_R vs. Reverse Current I_R

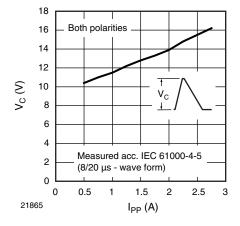


Fig. 5 - Typical Peak Clamping Voltage V_{C} vs. Peak Pulse Current I_{PP}

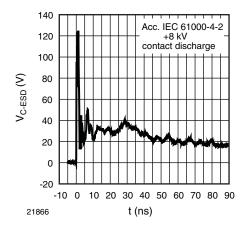


Fig. 6 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

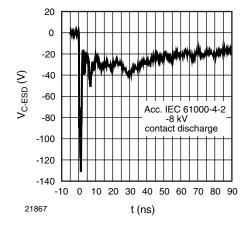


Fig. 7 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

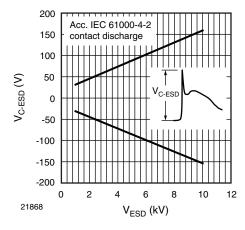
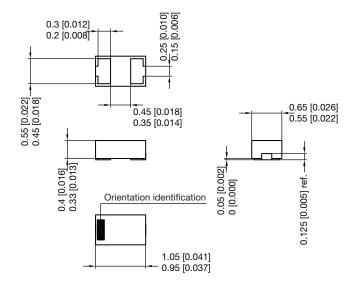


Fig. 8 - Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

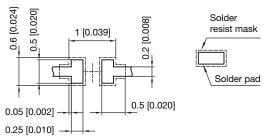
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PACKAGE DIMENSIONS in millimeters (inches): LLP1006-2M



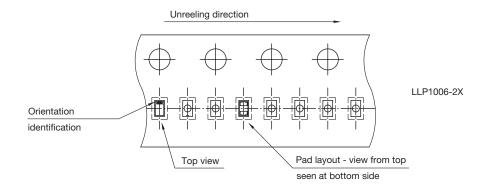
Foot print recommendation:



Pad Design Patented: (PUS 9.018.537 B2)

Document no.: S8-V-3906.04-005 (4) Rev. 7 - Date: 11.May 2016

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S8-V-3906.04-017 (4) 02.05.2017 22965



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