

### DESCRIPTION

The MP6902 is a Low-Drop Diode Emulator IC for Flyback converters which combined with an external switch replaces Schottky rectification diodes for high efficiency. The chip regulates the forward drop of an external switch to about 70mV and switches it off as soon as the voltage becomes negative. MP6902 has a light-load sleep mode that reduces the quiescent current to <300uA.

### FEATURES

- Supports DCM and Quasi-Resonant Flyback Converters
- Works with 12V Standard and 5V Logic Level FETS
- Compatible with Energy Star, 1W Standby Requirements
- V<sub>DD</sub> Range From 8V to 24V
- 70mV V<sub>DS</sub> Regulation Function <sup>(1)</sup>
- Fast Turn-off Total Delay of 20ns
- Max 400kHz Switching Frequency
- Light Load Mode Function <sup>(1)</sup> with <300µA Quiescent Current
- Supports High-side and Low-side Rectification
- Power Savings of Up to 1.5W in a Typical Notebook Adapter

### APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters

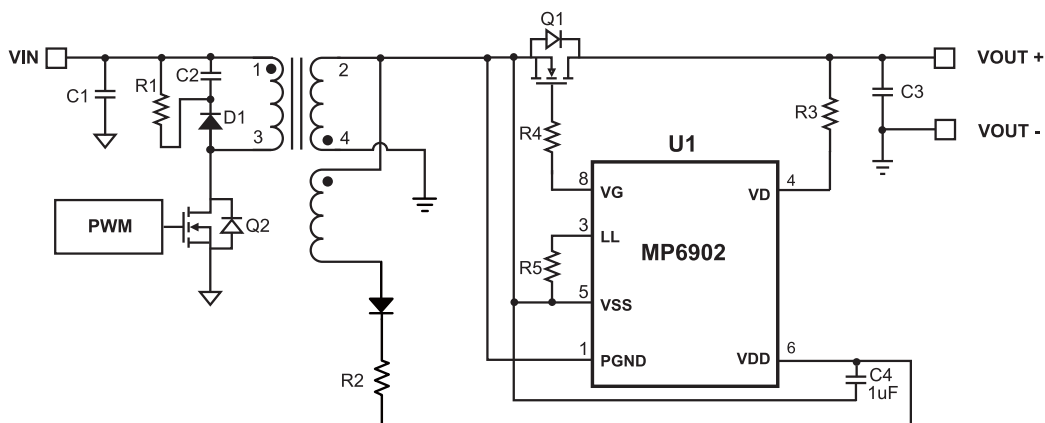
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**Notes:**

- 1) Related issued patent: US Patent US8,067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending.

### TYPICAL APPLICATION

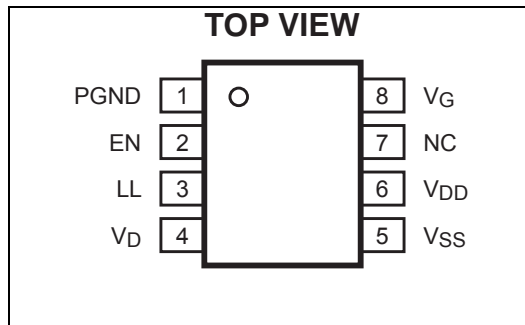


### ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6902DS	SOIC8	MP6902DS

\* For Tape & Reel, add suffix -Z (e.g. MP6902DS-Z);  
 For RoHS Compliant Packaging, add suffix -LF; (e.g. MP6902DS-LF-Z)

### PACKAGE REFERENCE



#### ABSOLUTE MAXIMUM RATINGS <sup>(2)</sup>

V <sub>DD</sub> to V <sub>SS</sub> .....	-0.3V to +27V
PGND to V <sub>SS</sub> .....	-0.3V to +0.3V
V <sub>G</sub> to V <sub>SS</sub> .....	-0.3V to V <sub>CC</sub>
V <sub>D</sub> to V <sub>SS</sub> .....	-0.7V to +180V
LL, EN to V <sub>SS</sub> .....	-0.3V to +6.5V
Maximum Operating Frequency .....	400 kHz
Continuous Power Dissipation (T <sub>A</sub> =+25°C) <sup>(3)</sup>	1.4W
Junction Temperature .....	150°C
Lead Temperature (Solder) .....	260°C
Storage Temperature .....	-55°C to +150°C

#### Recommended Operation Conditions <sup>(4)</sup>

V <sub>DD</sub> to V <sub>SS</sub> .....	8V to 24V
Operating Junction Temp. (T <sub>J</sub> ) .....	-40°C to +125°C

Thermal Resistance <sup>(5)</sup>	$\theta_{JA}$	$\theta_{JC}$
SOIC8 .....	90	45 ... °C/W

#### Notes:

- 2) Exceeding these ratings may damage the device.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub>(MAX)=(T<sub>J</sub>(MAX)-T<sub>A</sub>)/  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{DD} = 12V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
$V_{DD}$ Voltage Range			8		24	V
$V_{DD}$ UVLO Rising			5.0	6.0	7.0	V
$V_{DD}$ UVLO Hysteresis			0.8	1	1.2	V
Operating Current	$I_{CC}$	$C_{LOAD}=5nF$ , $F_{SW}=100kHz$		8	10	mA
Quiescent Current	$I_q$	$V_{SS}-V_D=0.5V$		2	3	mA
Shutdown Current		$V_{DD}=4V$		210	255	$\mu A$
		$V_{DD}=20V$ , $EN=0V$		375	440	
Light-load Mode Current				290	380	$\mu A$
Thermal Shutdown				150		$^\circ C$
Thermal Shutdown Hysteresis				30		$^\circ C$
Enable UVLO Rising			1.1	1.5	1.9	V
Enable UVLO Hysteresis				0.2	0.4	V
Internal Pull-up Current On EN Pin				10	15	$\mu A$
<b>CONTROL CIRCUITRY SECTION</b>						
$V_{SS}-V_D$ Forward Voltage	$V_{fwd}$		55	70	85	mV
Turn-on Delay	$T_{Don}$	$C_{LOAD} = 5nF$		150		ns
	$T_{Don}$	$C_{LOAD} = 10nF$		250		ns
Input Bias Current On $V_D$ Pin		$V_D = 180V$			1	$\mu A$
Minimum On-time <sup>(5)</sup>	$T_{MIN}$	$C_{LOAD} = 5nF$		1.6		$\mu s$
Light-load-enter Delay	$T_{LL-Delay}$	$R_{LL}=100k\Omega$		100		$\mu s$
Light-load-enter Pulse Width	$T_{LL}$	$R_{LL}=100k\Omega$	1.3	1.75	2.2	$\mu s$
Light-load-enter Pulse Width Hysteresis	$T_{LL-H}$	$R_{LL}=100k\Omega$		0.2		$\mu s$
Light-load Resistor Value	$R_{LL}$		30		300	k $\Omega$
Light-load Mode Exit Pulse Width Threshold ( $V_{DS}$ )	$V_{LL-DS}$		-400	-250	-150	mV
Light-load Mode Enter Pulse Width Threshold ( $V_{GS}$ ) <sup>(6)</sup>	$V_{LL-GS}$			1.0		V
<b>GATE DRIVER SECTION</b>						
$V_G$ (Low)		$I_{LOAD}=1mA$		0.05	0.1	V
$V_G$ (High)		$V_{DD} > 17V$	13	14	15	V
		$V_{DD} < 17V$	$V_{DD}-2.2$			
Turn-off Threshold ( $V_{SS}-V_D$ )				30		mV
Turn-off Propagation Delay		$V_D=V_{SS}$		15		ns
Turn-off Total Delay	$T_{Doff}$	$V_D = V_{SS}$ , $C_{LOAD}=5nF$ , $R_{GATE}=0\Omega$		35		ns
	$T_{Doff}$	$V_D = V_{SS}$ , $C_{LOAD}=10nF$ , $R_{GATE}=0\Omega$		45		ns
Pull Down Impedance				1	2	$\Omega$
Pull Down Current <sup>(6)</sup>		$3V < V_G < 10V$		2		A

**Notes:**

6) Guaranteed by Design and Characterization.

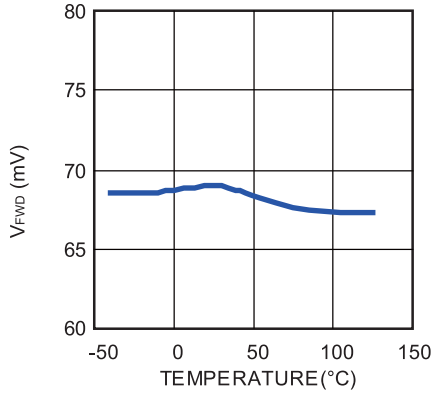
**PIN FUNCTIONS**

<b>Pin #</b>	<b>Name</b>	<b>Description</b>
1	PGND	Power Ground, return for driver switch
2	EN	Enable pin, active high
3	LL	Light load timing setting. Connect a resistor to set the light load timing.
4	VD	FET drain voltage sense
5	VSS	Ground, also used as reference for VD
6	VDD	Supply Voltage
7	NC	No connection
8	VG	Gate drive output

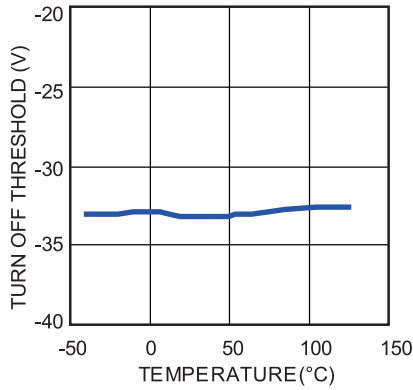
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 12V$ , unless otherwise noted.

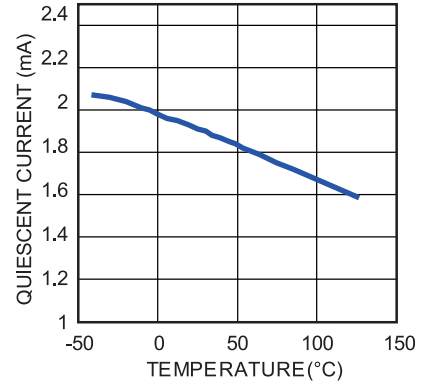
$V_{FWD}$  vs. Temperature



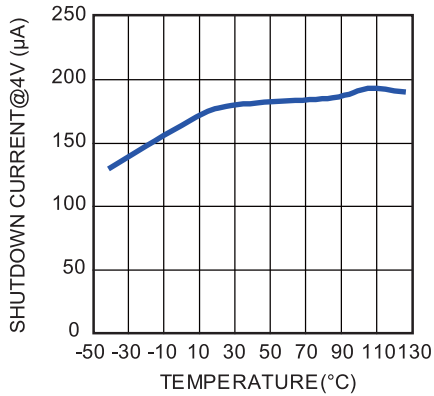
Turn off threshold vs. Temperature



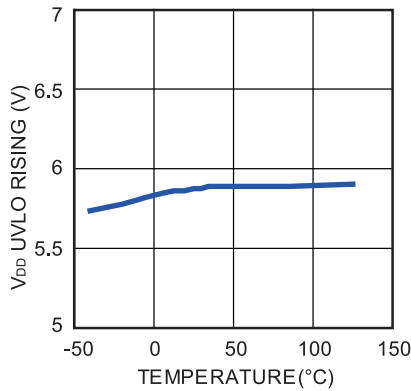
Quiescent Current vs. Temperature



Shutdown Current vs. Temperature

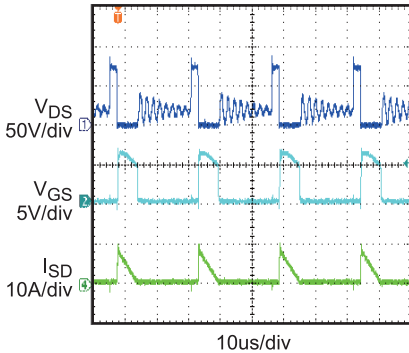


$V_{DD}$  UVLO Rising vs. Temperature



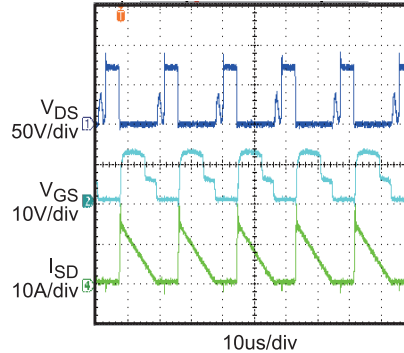
Operation in 90W Flyback Application

( $V_{IN}=250Vac$ ,  $I_{OUT}=1A$ )



Operation in 90W Flyback Application

( $V_{IN}=250Vac$ ,  $I_{OUT}=4.7A$ )



**Notes:**

7) See Figure 13 for the test circuit.

BLOCK DIAGRAM

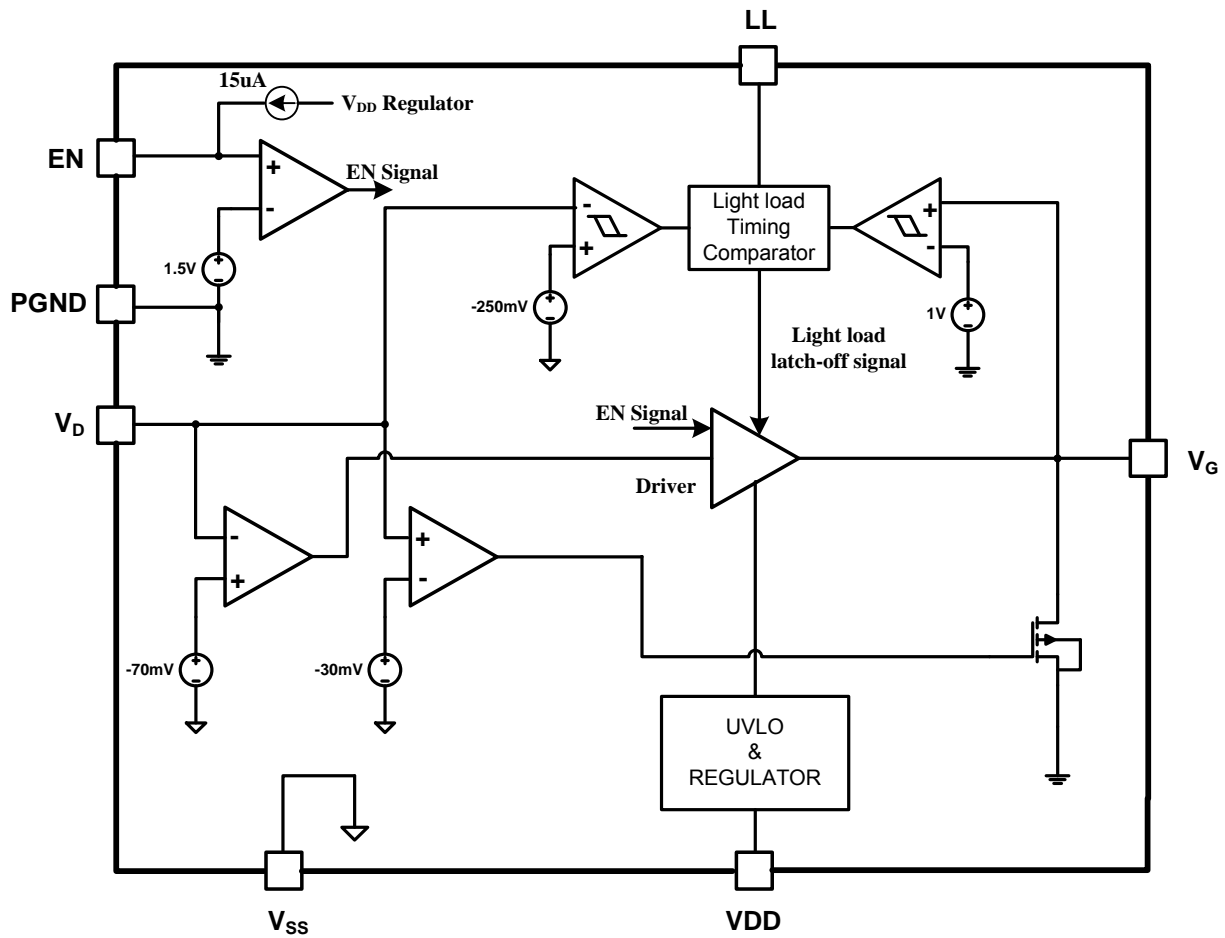


Figure 1—Function Block Diagram

## OPERATION

The MP6902 supports operation in DCM and Quasi-Resonant Flyback converters. The control circuitry controls the gate in forward mode and will turn the gate off when the MOSFET current is fairly low.

### Blanking

The control circuitry contains a blanking function. When it pulls the MOSFET on/off, it makes sure that the on/off state at least lasts for some time. The turn on blanking time is  $\sim 1.6\mu\text{s}$ , which determines the minimum on-time. During the turn on blanking period, the turn off threshold is not totally blanked, but changes the threshold voltage to  $\sim +50\text{mV}$  (instead of  $-30\text{mV}$ ). This assures that the part can always be turned off even during the turn on blanking period. (Albeit slower)

### VD Clamp

Because  $V_D$  can go as high as 180V, a High-Voltage JFET is used at the input. To avoid excessive currents when  $V_g$  goes below  $-0.7\text{V}$ , a small resistor is recommended between  $V_D$  and the drain of the external MOSFET.

### Under-Voltage Lockout (UVLO)

When the  $V_{DD}$  is below UVLO threshold, the part is in sleep mode and the  $V_g$  pin is pulled low by a  $10\text{k}\Omega$  resistor.

### Enable pin

If EN is pulled low, the part is in sleep mode.

### Thermal shutdown

If the junction temperature of the chip exceeds  $170^\circ\text{C}$ , the  $V_g$  will be pulled low and the part stops switching. The part will return to normal function after the junction temperature has dropped to  $120^\circ\text{C}$ .

### Thermal Design

If the dissipation of the chip is higher than  $100\text{mW}$  due to switching frequencies above  $100\text{kHz}$ .

### Turn-on Phase

When the synchronous MOSFET is conducting, current will flow through its body diode which generates a negative  $V_{ds}$  across it. Because this

body diode voltage drop ( $< -500\text{mV}$ ) is much smaller than the turn on threshold of the control circuitry ( $-70\text{mV}$ ), which will then pull the gate driver voltage high to turn on the synchronous MOSFET after about  $150\text{ns}$  turn on delay (Defined in Figure 2).

As soon as the turn on threshold ( $-70\text{mV}$ ) is triggered, a blanking time (Minimum on-time:  $\sim 1.6\mu\text{s}$ ) will be added during which the turn off threshold will be changed from  $-30\text{mV}$  to  $+50\text{mV}$ . This blanking time can help to avoid error trigger on turn on turn off threshold caused by the turn on ringing of the synchronous MOSFET.

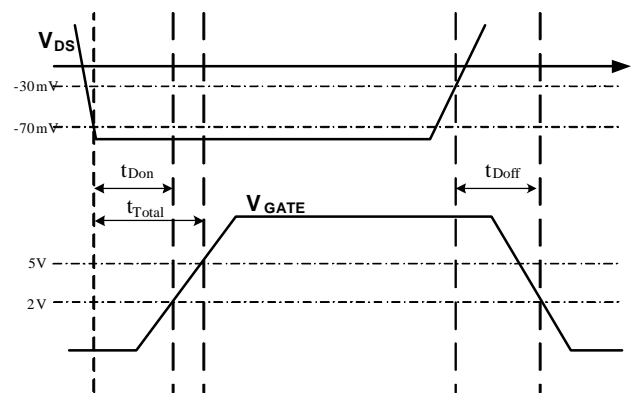


Figure 2—Turn on and Turn off delay

### Conducting Phase

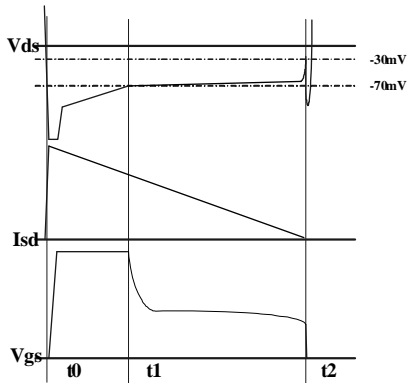
When the synchronous MOSFET is turned on,  $V_{ds}$  becomes to rise according to its on resistance, as soon as  $V_{ds}$  rises above the turn on threshold ( $-70\text{mV}$ ), the control circuitry stops pulling up the gate driver which leads the gate voltage is pulled down by the internal pull-down resistance ( $10\text{k}\Omega$ ) to larger the on resistance of synchronous MOSFET to ease the rise of  $V_{ds}$ . By doing that,  $V_{ds}$  is adjusted to be around  $-70\text{mV}$  even when the current through the MOS is fairly small, this function can make the driver voltage fairly low when the synchronous MOSFET is turned off to fast the turn off speed (this function is still active during turn on blanking time which means the gate driver could still be turned off even with very small duty of the synchronous MOSFET).

**Turn-off Phase**

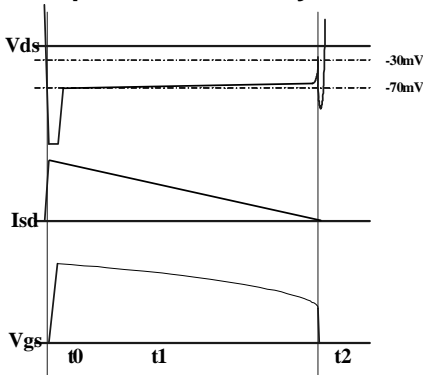
When  $V_{ds}$  rises to trigger the turn off threshold (-30mV), the gate voltage is pulled to low after about 20ns turn off delay (defined in Figure 2) by the control circuitry. Similar with turn-on phase, a 200ns blanking time is added after the synchronous MOSFET is turned off to avoid error trigger.

Figure 3 shows synchronous rectification operation at heavy load condition. Due to the high current, the gate driver will be saturated at first, during which the gate driver voltage is kept at ~2V lower than  $V_{DD}$  (when  $V_{DD} > 16V$ , gate driver will be internal clamped at 14V). After  $V_{ds}$  goes to above -70mV, gate driver voltage decreases to adjust the  $V_{ds}$  to typical -70mV.

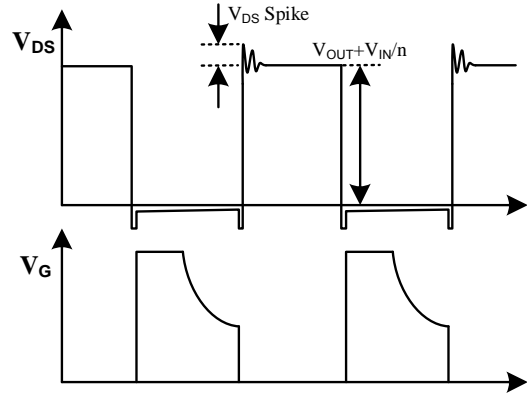
Figure 4 shows synchronous rectification operation at light load condition. Due to the low current, the gate driver voltage never saturates but begins to decrease as soon as the synchronous MOSFET is turned on and adjust the  $V_{ds}$ .



**Figure 3—Synchronous Rectification Operation at heavy load**



**Figure 4—Synchronous Rectification Operation at light load**



**Figure 5—Drain-Source and Gate Driver voltage on SR MOSFET**

Figure 5 shows the whole synchronous rectification waveform on drain-source voltage  $V_{DS}$  and gate driver signal  $V_{GS}$ . For safe operation of the IC, it is required:

$$V_{OUT} + V_{IN} / n + V_{DS\_Spike} < 180V * k$$

Where 180V is the maximum voltage rating on  $V_D$  pin of MP6902,  $V_{IN}/V_{OUT}$  is the input/output DC voltage,  $n$  is the turn ratio from primary to secondary of the power transformer,  $V_{DS\_Spike}$  is the spike voltage on drain-source which is lead by leakage inductance, while  $k$  is the de-rating factor which is usually selected as 0.7~0.8.

**Light-load Latch-off Function**

The gate driver of MP6902 is latched to save the driver loss at light-load condition to improve efficiency. When the synchronous MOSFET's conducting period keeps lower than light load timing ( $T_{LL}$ ) for longer than the light-load-enter delay ( $T_{LL-Delay}$ ), MP6902 enters light-load mode and latches off the gate driver. Here the synchronous MOSFET's conducting period is from turn on of the gate driver to the moment when  $V_{GS}$  drops to below 1V ( $V_{LL\_GS}$ ). During light-load mode, MP6902 monitors the synchronous MOSFET's body diode conducting period by sensing the time duration of the  $V_{DS}$  below -250mV ( $V_{LL\_DS}$ ). If it is longer than  $T_{LL} + T_{LL-H}$  ( $T_{LL-H}$ , light-load-enter pulse width hysteresis), the light-load mode is finished and gate driver of MP6902 is unlatched to restart the synchronous rectification.



For MP6902, the light load enter timing ( $T_{LL}$ ) is programmable by connecting a resistor ( $R_{LL}$ ) on LL pin, by monitoring the LL pin current (the LL pin voltage keeps at  $\sim 2V$  internally),  $T_{LL}$  is set as following:

$$T_{LL} \approx R_{LL} (k\Omega) \cdot \frac{2.2\mu s}{100k\Omega}$$

### SR MOSFET Selection and Driver Ability

The Power Mosfet selection proved to be a trade off between  $R_{on}$  and  $Q_g$ . In order to achieve high efficiency, the Mosfet with smaller  $R_{on}$  is always preferred, while the  $Q_g$  is usually larger with smaller  $R_{on}$ , which makes the turn-on/off speed lower and lead to larger power loss. For MP6902, because  $V_{ds}$  is regulated at  $\sim 70mV$  during the driving period, the Mosfet with too small  $R_{on}$  is not recommend, because the gate driver may be pulled down to a fairly low level with too small  $R_{on}$  when the Mosfet current is still fairly high, which make the advantage of the low  $R_{on}$  inconspicuous.

Figure 6 shows the typical waveform of QR flyback. Assume 50% duty cycle and the output current is  $I_{OUT}$ .

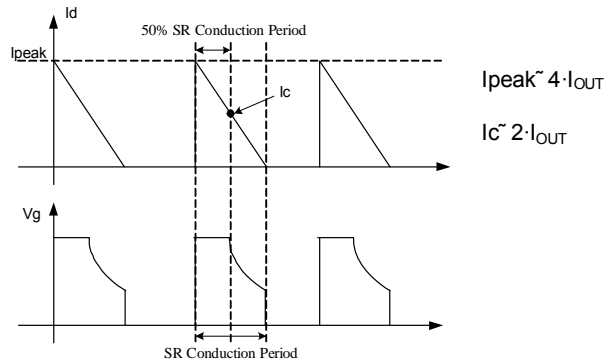
To achieve fairly high usage of the Mosfet's  $R_{on}$ , it is expected that the Mosfet be fully turned on at least 50% of the SR conduction period:

$$V_{ds} = -I_c \times R_{on} = -2 \cdot I_{OUT} \times R_{on} \leq -V_{fwd}$$

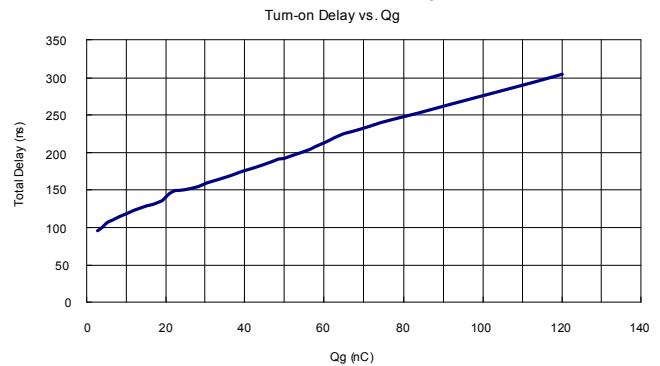
Where  $V_{ds}$  is Drain-Source voltage of the Mosfet and  $V_{fwd}$  is the forward voltage threshold of MP6902, which is  $\sim 70mV$ .

So the Mosfet's  $R_{on}$  is recommended to be no lower than  $\sim 35/I_{OUT}$  (m $\Omega$ ). (For example, for 5A application, the  $R_{on}$  of the Mosfet is recommended to be no lower than 7m $\Omega$ )

Figure 7 shows the corresponding total delay during turn-on period ( $t_{Total}$ , see Figure 2) with driving different  $Q_g$  Mosfet by MP6902. From Figure 7, with driving a 120nC  $Q_g$  Mosfet, the driver ability of MP6902 is able to pull up the gate driver voltage of the Mosfet to  $\sim 5V$  in 300ns as soon as the body diode of the Mosfet is conducting, which greatly save the turn-on power loss in the Mosfet's body diode.

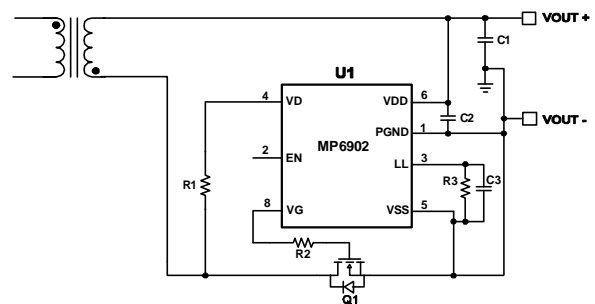


**Figure 6—Synchronous Rectification typical waveforms in QR Flyback**



**Figure 7—Total Turn-on Delay vs.  $Q_g$**

### Typical System Implementations



**Figure 8— IC Supply derived directly from Output Voltage**

Figure 8 shows the typical system implementation for the IC supply derived from output voltage, which is available in low-side rectification and the output voltage is recommended to be in the  $V_{DD}$  range of MP6902 (from 8V to 24V).

If output voltage is out of the  $V_{DD}$  range of MP6902 or high-side rectification is used, it is recommended to use an auxiliary winding from the power transformer for the IC supply, which is shown in Figure 9 and Figure.10.

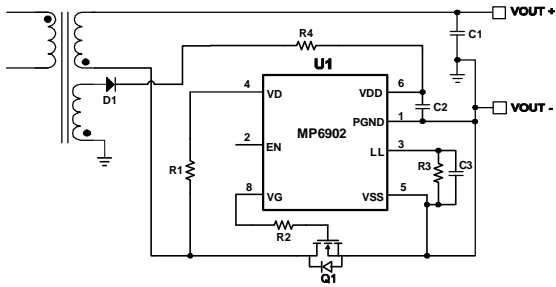


Figure 9— IC Supply derived from Auxiliary Winding in Low-Side Rectification

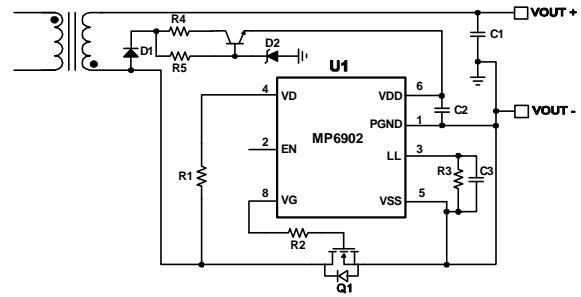


Figure 11— IC Supply derived from Secondary Winding through External LDO in Low-Side Rectification

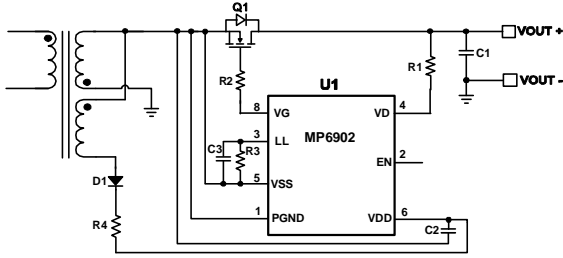


Figure 10— IC Supply derived from Auxiliary Winding in High-Side Rectification

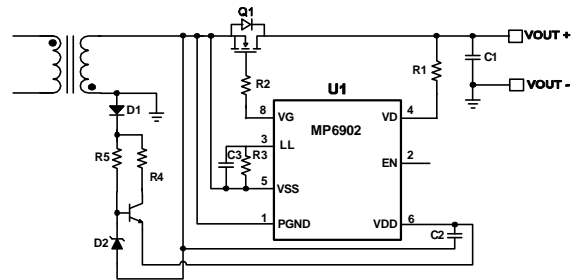
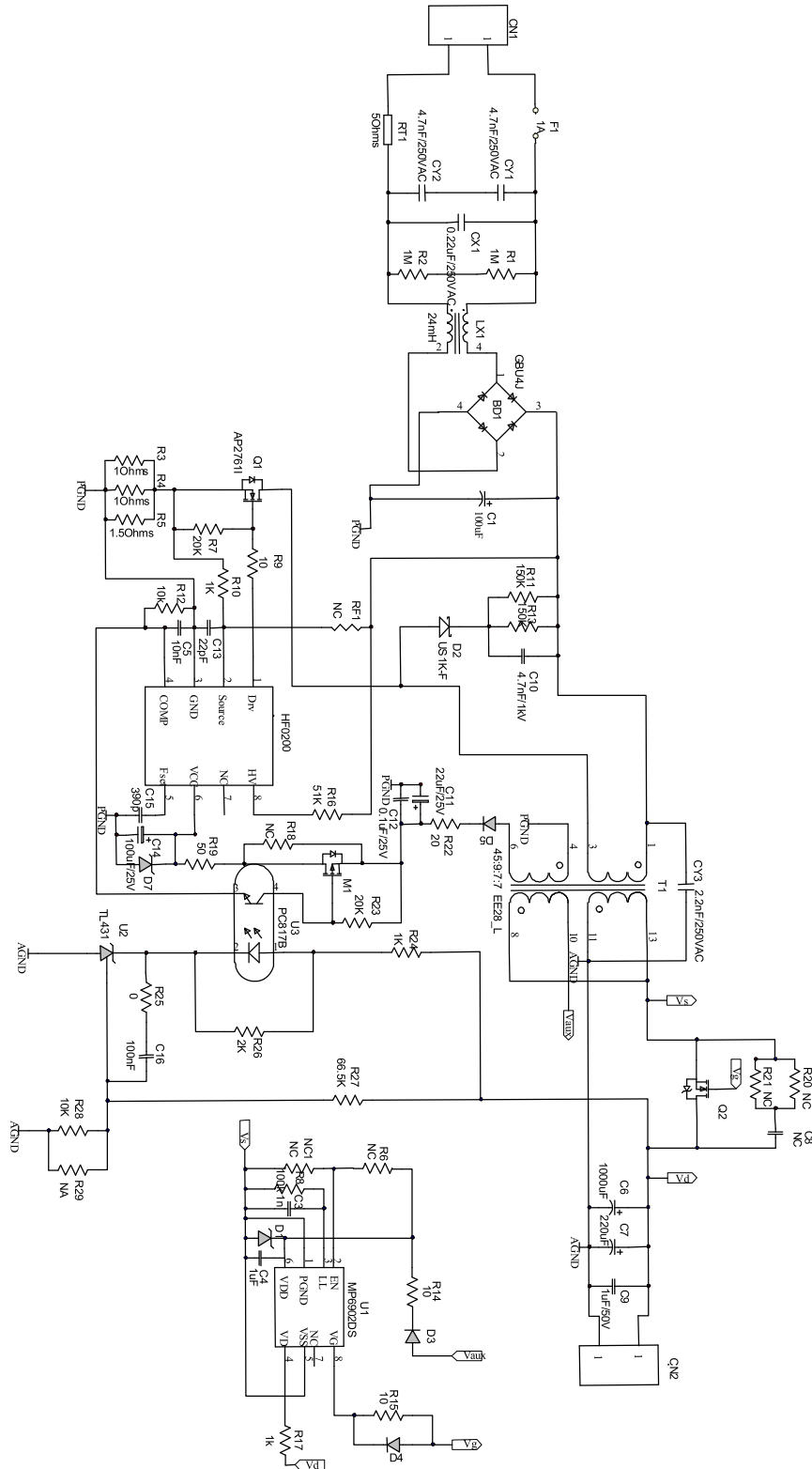
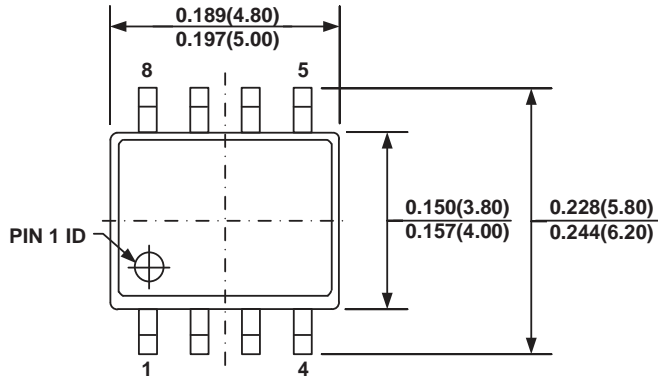
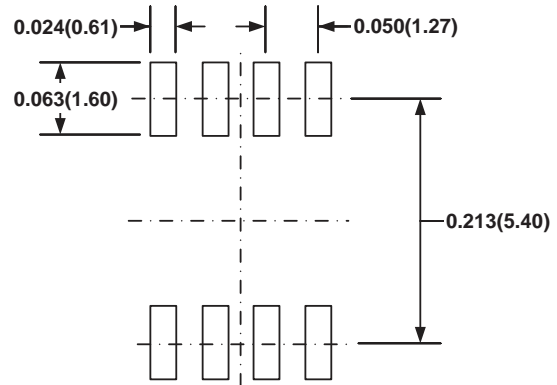
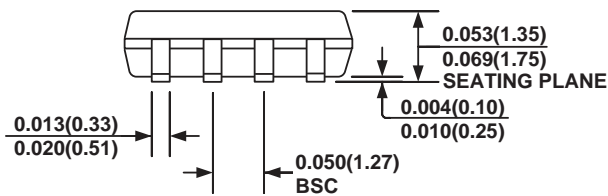
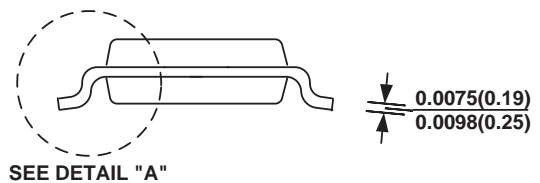
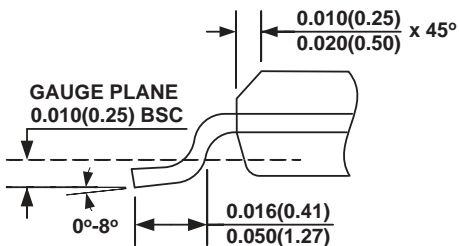


Figure 12— IC Supply derived from Secondary Winding through External LDO in High-Side Rectification

There is another non-auxiliary winding solution for the IC supply, which uses an external LDO circuit from the secondary transformer winding. See Figure.11 and Figure.12, compared with using auxiliary winding for IC supply, this solution has a bit higher power loss which is dissipate on the LDO circuit especially when the secondary winding voltage is high.

**TYPICAL APPLICATION CIRCUIT**

**Figure 13—MP6902 for Secondary Synchronous Controller in 90W Flyback Application**

**PACKAGE INFORMATION**
**SOIC8**

**TOP VIEW**

**RECOMMENDED LAND PATTERN**

**FRONT VIEW**

**SIDE VIEW**

**DETAIL "A"**
**NOTE:**

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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