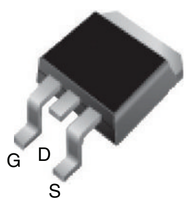
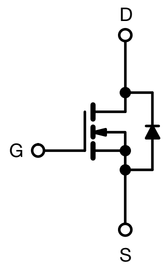
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.85
Q_g max. (nC)	63	
Q_{gs} (nC)	9.3	
Q_{gd} (nC)	32	
Configuration	Single	

D[2]PAK (TO-263)





N-Channel MOSFET

FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirement
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS* Available
HALOGEN FREE Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D[2]PAK (TO-263) is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D[2]PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION			
Package	D[2]PAK (TO-263)	D[2]PAK (TO-263)	D[2]PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF840S-GE3	SiHF840STRL-GE3 [a]	SiHF840STRR-GE3 [a]
Lead (Pb)-free	IRF840SPbF	IRF840STRLPbF [a]	IRF840STRRPbF [a]
	SiHF840S-E3	SiHF840STL-E3 [a]	SiHF840STR-E3 [a]

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	8.0	A
		T_C = 100 °C		5.1	
Pulsed Drain Current [a]			I_{DM}	32	
Linear Derating Factor				1.0	W/°C
Linear Derating Factor (PCB mount) [e]				0.025	
Single Pulse Avalanche Energy [b]			E_{AS}	510	mJ
Avalanche Current [a]			I_{AR}	8.0	A
Repetitive Avalanche Energy [a]			E_{AR}	13	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	125	W
Maximum Power Dissipation (PCB mount) [e]	T_A = 25 °C			3.1	
Peak Diode Recovery dV/dt [c]			dV/dt	3.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak temperature) [d]	for 10 s			300	

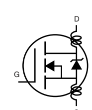
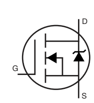
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 14 mH, R_g = 25 Ω, I_{AS} = 8.0 A (see fig. 12).
c. $I_{SD} \leq$ 8.0 A, dI/dt $\leq$ 100 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Ambient (PCB mount) [a]	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0, I_D = 250 μA	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.78	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 4.8 A [b]	-	-	0.85	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 4.8 A [b]	4.9	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	1300	-	pF
Output Capacitance	C_{oss}		-	310	-	
Reverse Transfer Capacitance	C_{rss}		-	120	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 8.0 A, V_{DS} = 400 V, see fig. 6 and 13 [b]	-	-	63	nC
Gate-Source Charge	Q_{gs}		-	-	9.3	
Gate-Drain Charge	Q_{gd}		-	-	32	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 8.0 A, R_g = 9.1 Ω, R_D = 31 Ω, see fig. 10 [b]	-	14	-	ns
Rise Time	t_r		-	23	-	
Turn-Off Delay Time	$t_{d(off)}$		-	49	-	
Fall Time	t_f		-	20	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain	0.6	-	2.8	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	8.0	A
Pulsed Diode Forward Current [a]	I_{SM}		-	-	32	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 8.0 A, V_{GS} = 0 V [b]	-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 8.0 A, dI/dt = 100 A/μs [b]	-	460	970	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	4.2	8.9	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

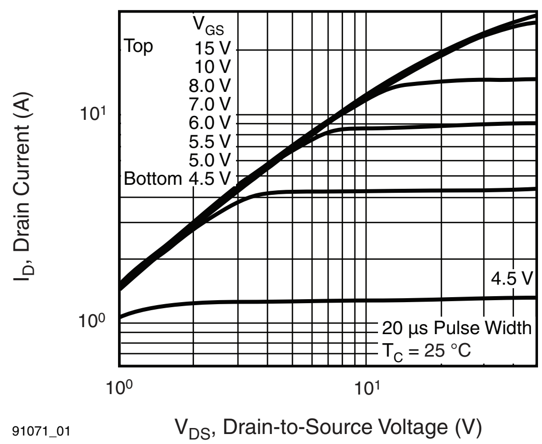


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

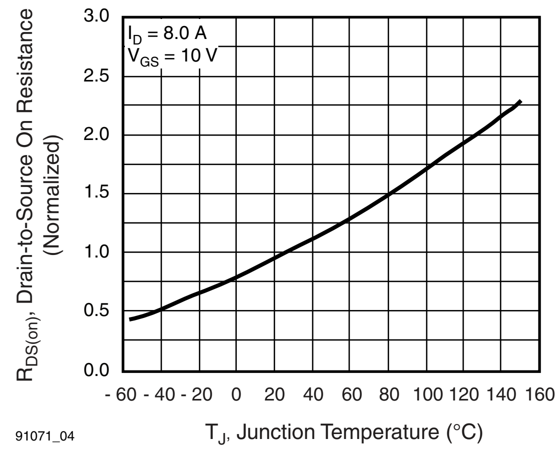


Fig. 4 - Normalized On-Resistance vs. Temperature

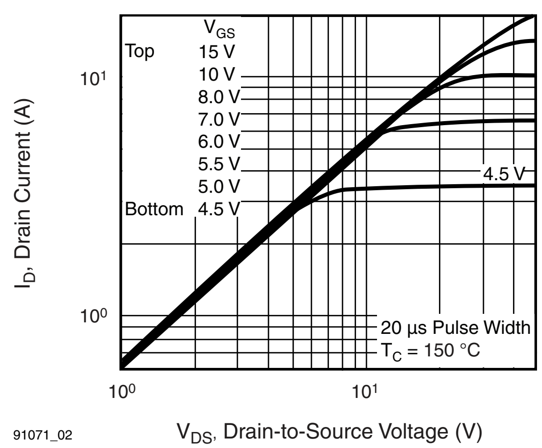


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

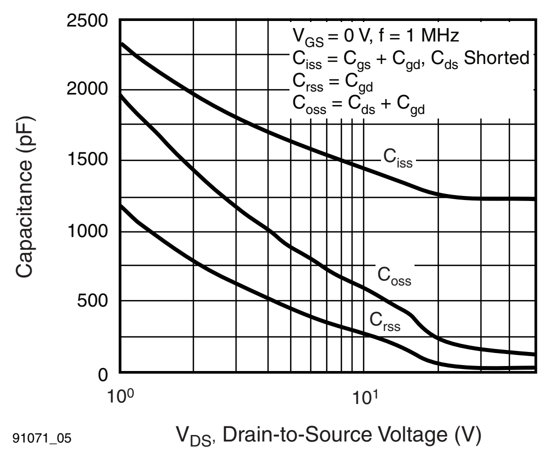


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

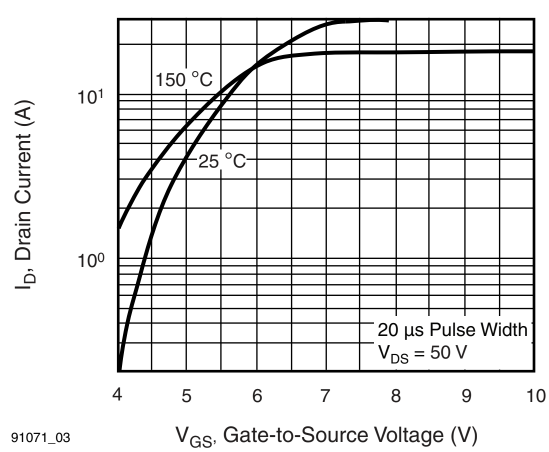


Fig. 3 - Typical Transfer Characteristics

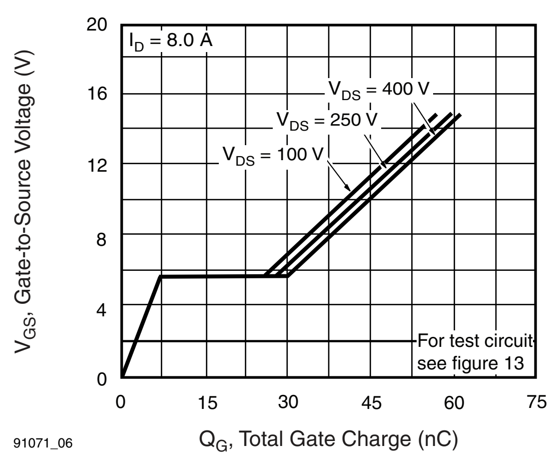


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

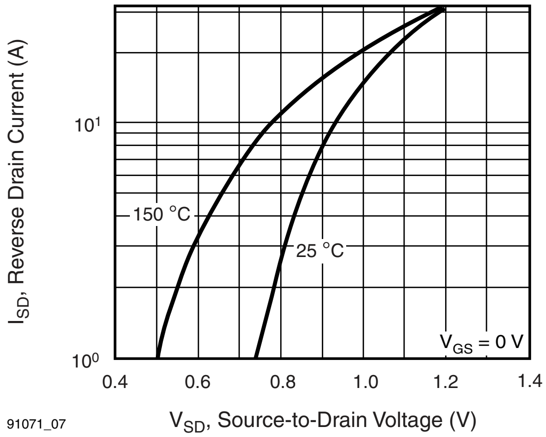


Fig. 7 - Typical Source-Drain Diode Forward Voltage

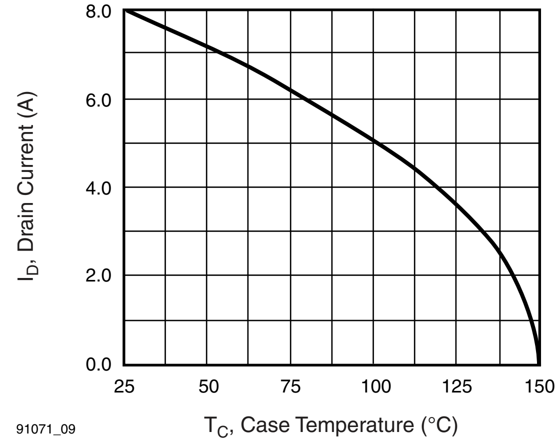


Fig. 9 - Maximum Drain Current vs. Case Temperature

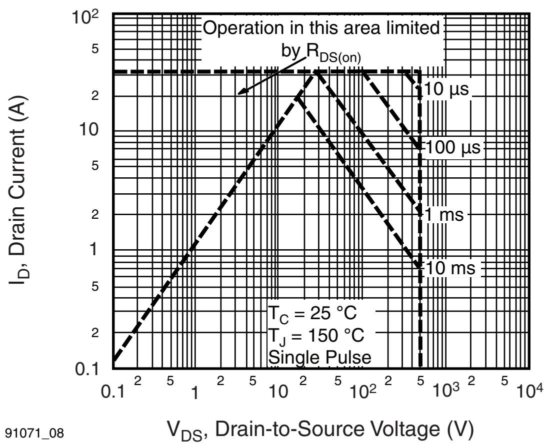


Fig. 8 - Maximum Safe Operating Area

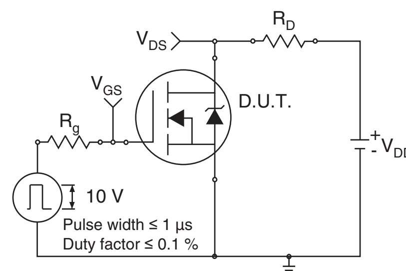


Fig. 10a - Switching Time Test Circuit

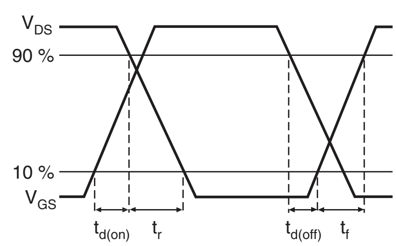


Fig. 10b - Switching Time Waveforms

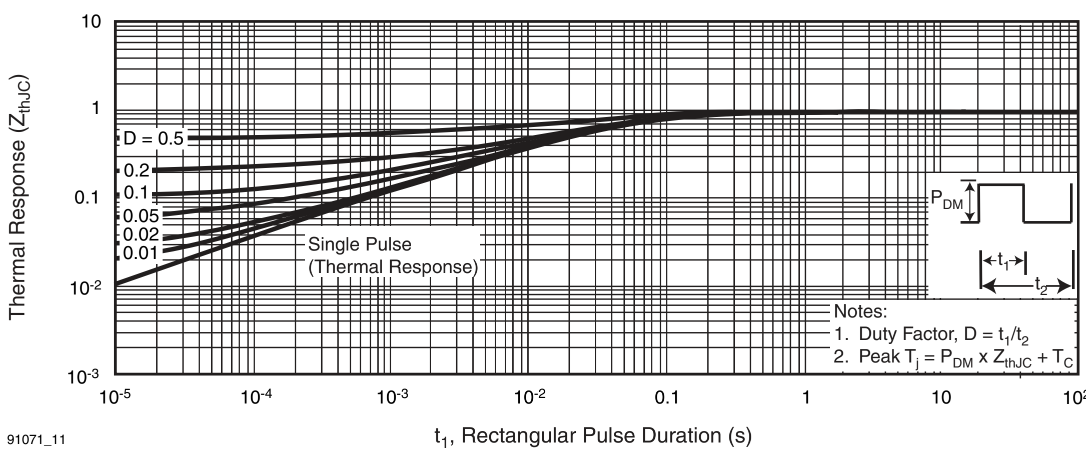


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

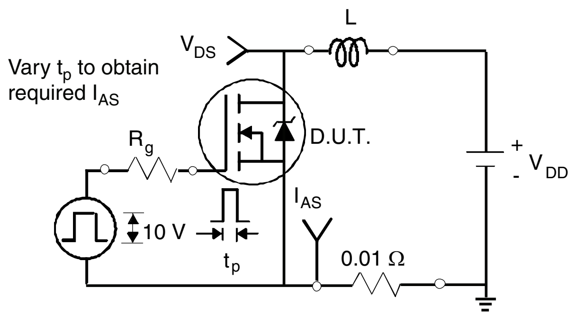


Fig. 12a - Unclamped Inductive Test Circuit

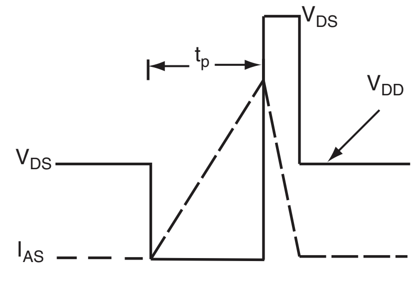


Fig. 12b - Unclamped Inductive Waveforms

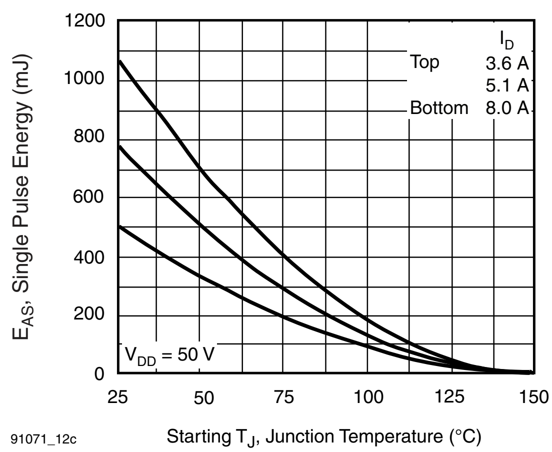


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

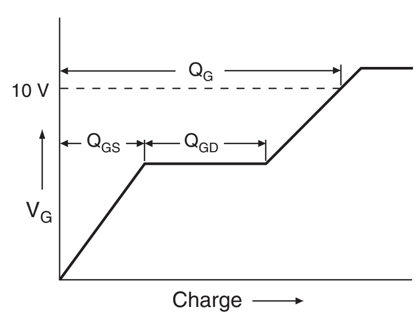


Fig. 13a - Basic Gate Charge Waveform

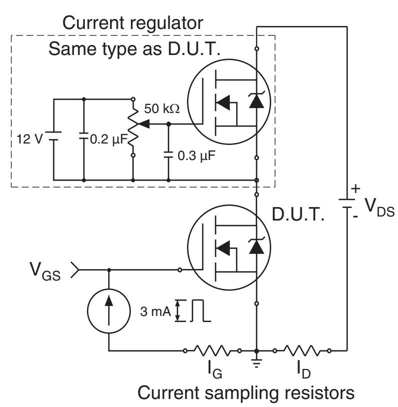
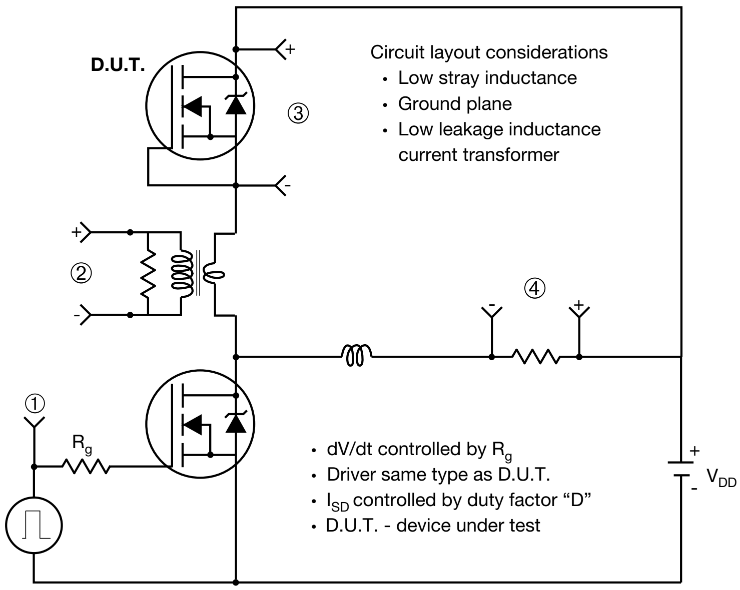
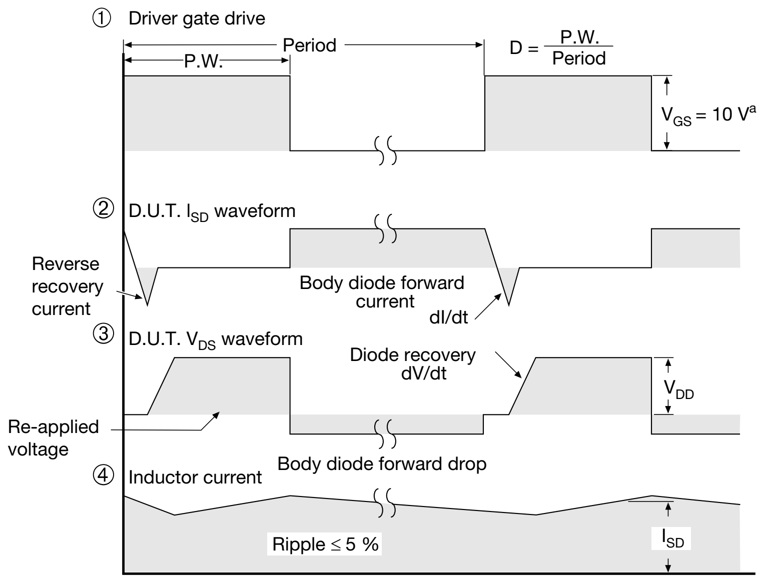


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





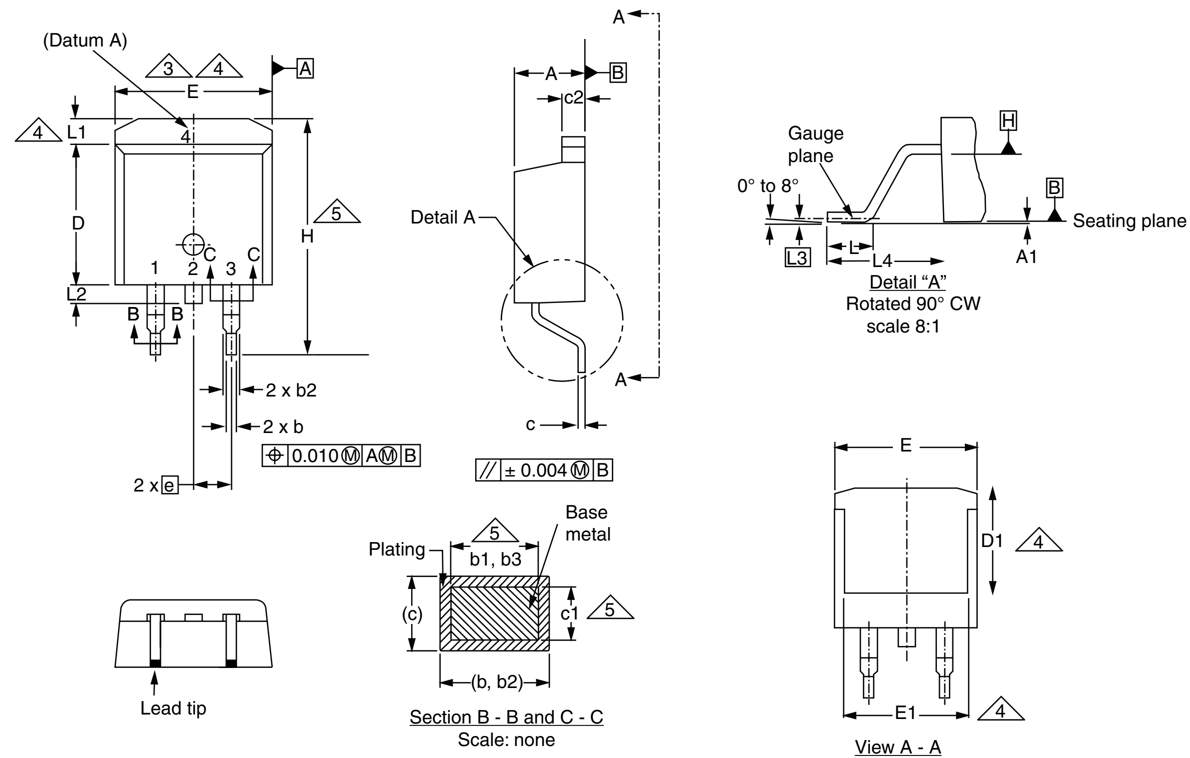
Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91071.

TO-263AB (HIGH VOLTAGE)

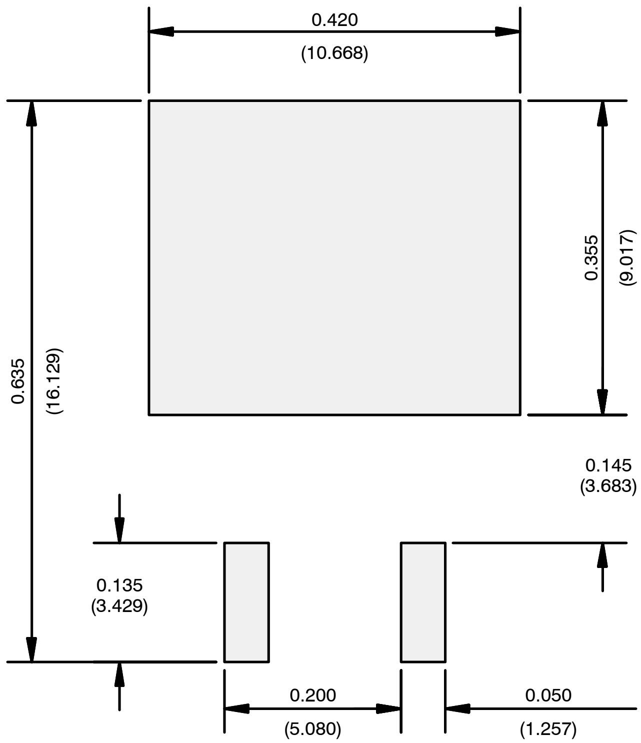


	MILLIMETERS		INCHES			MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.	DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190	D1	6.86	-	0.270	-
A1	0.00	0.25	0.000	0.010	E	9.65	10.67	0.380	0.420
b	0.51	0.99	0.020	0.039	E1	6.22	-	0.245	-
b1	0.51	0.89	0.020	0.035	e	2.54 BSC		0.100 BSC	
b2	1.14	1.78	0.045	0.070	H	14.61	15.88	0.575	0.625
b3	1.14	1.73	0.045	0.068	L	1.78	2.79	0.070	0.110
c	0.38	0.74	0.015	0.029	L1	-	1.65	-	0.066
c1	0.38	0.58	0.015	0.023	L2	-	1.78	-	0.070
c2	1.14	1.65	0.045	0.065	L3	0.25 BSC		0.010 BSC	
D	8.38	9.65	0.330	0.380	L4	4.78	5.28	0.188	0.208
ECN: S-82110-Rev. A, 15-Sep-08 DWG: 5970									

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D^2PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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