



# 74AHC1G79-Q100; 74AHCT1G79-Q100

Single D-type flip-flop; positive-edge trigger

Rev. 5 — 20 September 2023

Preliminary data sheet

## 1. General description

The 74AHC1G79-Q100; 74AHCT1G79-Q100 is a single positive-edge triggered D-type flip-flop. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Symmetrical output impedance
- Balanced propagation delays
- Input levels:
  - For 74AHC1G79-Q100: CMOS level
  - For 74AHCT1G79-Q100: TTL level
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74AHC1G79GW-Q100</a> <a href="#">74AHCT1G79GW-Q100</a>	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	<a href="#">SOT353-1</a>
<a href="#">74AHC1G79GV-Q100</a> <a href="#">74AHCT1G79GV-Q100</a>	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	<a href="#">SOT753</a>

## 4. Marking

Table 2. Marking codes

Type number	Marking <sup>[1]</sup>
74AHC1G79GW-Q100	AP
74AHCT1G79GW-Q100	CP
74AHC1G79GV-Q100	A79
74AHCT1G79GV-Q100	C79

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram

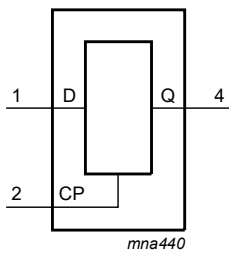


Fig. 1. Logic symbol

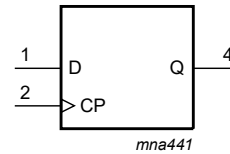


Fig. 2. IEC logic symbol

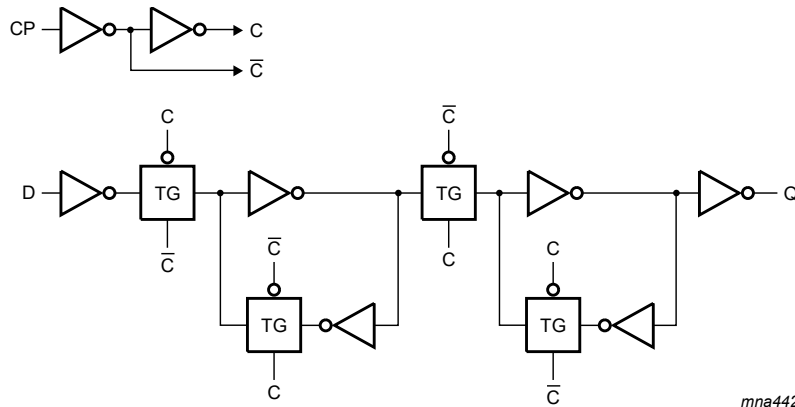
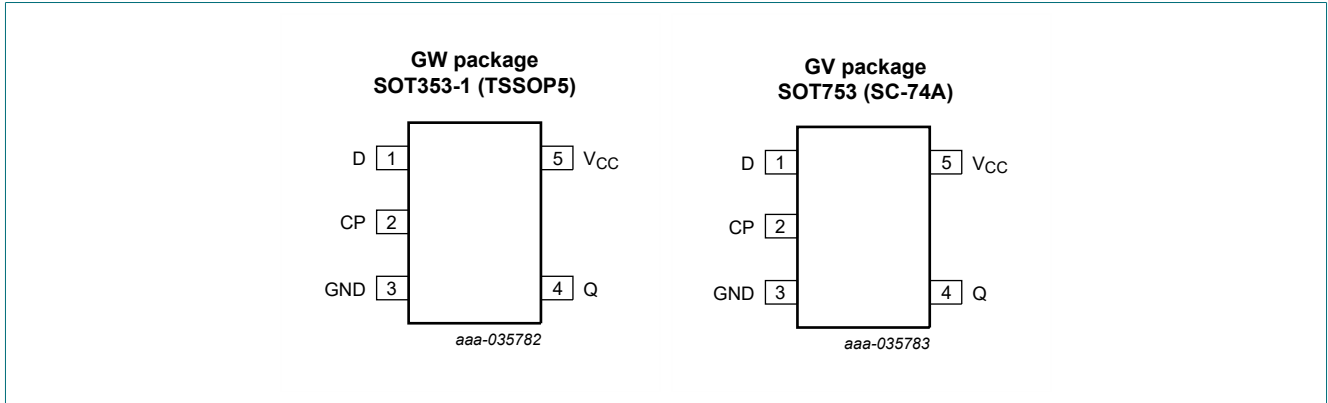


Fig. 3. Logic diagram

## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
D	1	data input
CP	2	clock pulse input
GND	3	ground (0 V)
Q	4	data output
V <sub>CC</sub>	5	supply voltage

## 7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH CP transition; X = don't care;  
 Q + 1 = state after the next LOW-to-HIGH CP transition.

Inputs		Output
CP	D	Q + 1
↑	L	L
↑	H	H
L	X	Q

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	-20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
$I_O$	output current	$-0.5$ V < $V_O$ < $V_{CC} + 0.5$ V	-	±25	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package:  $P_{tot}$  derates linearly with 3.3 mW/K above 74 °C.

For SOT753 (SC-74A) package:  $P_{tot}$  derates linearly with 3.8 mW/K above 85 °C.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC1G79-Q100			74AHCT1G79-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	-	-	20	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC1G79-Q100</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0$ V	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 5.5$ V	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0$ V	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5$ V	-	-	1.65	-	1.65	-	1.65	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	µA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF
<b>74AHCT1G79-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = 3.4 V; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

$GND = 0\text{ V}$ ;  $t_r = t_f = \leq 3.0\text{ ns}$ . For test circuit see Fig. 5. For waveform see Fig. 4.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC1G79-Q100</b>										
$t_{pd}$	propagation delay	CP to Q [1]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2]								
		$C_L = 15\text{ pF}$	-	4.9	8.4	1.0	9.8	1.0	11.5	ns
		$C_L = 50\text{ pF}$	-	6.9	12.0	1.0	14.0	1.0	15.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]								
		$C_L = 15\text{ pF}$	-	3.5	5.6	1.0	7.0	1.0	8.0	ns
		$C_L = 50\text{ pF}$	-	5.1	8.0	1.0	10.0	1.0	11.0	ns
$t_{su}$	set-up time	D to CP	3.0	1.0	-	3.0	-	4.0	-	ns
$t_h$	hold time	D to CP	+2.0	-1.0	-	2.0	-	3.0	-	ns
$t_W$	pulse width	clock HIGH or LOW	3.0	-	-	3.0	-	4.0	-	ns
$f_{max}$	maximum frequency		90	-	-	90	-	70	-	MHz
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ ; $V_I = GND\text{ to }V_{CC}$ [4]	-	15	-	-	-	-	-	pF
<b>74AHCT1G79-Q100</b>										
$t_{pd}$	propagation delay	CP to Q [1]								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]								
		$C_L = 15\text{ pF}$	-	3.5	5.0	1.0	6.0	1.0	8.0	ns
		$C_L = 50\text{ pF}$	-	5.0	8.0	1.0	10.0	1.0	11.0	ns
$t_{su}$	set-up time	D to CP	3.0	1.0	-	3.0	-	4.0	-	ns
$t_h$	hold time	D to CP	+2.0	-1.0	-	2.0	-	3.0	-	ns
$t_W$	pulse width	clock HIGH or LOW	3.0	-	-	3.0	-	4.0	-	ns
$f_{max}$	maximum frequency		90	-	-	90	-	70	-	MHz
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ ; $V_I = GND\text{ to }V_{CC}$ [4]	-	16	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[2] Typical values are measured at  $V_{CC} = 3.3\text{ V}$ .

[3] Typical values are measured at  $V_{CC} = 5.0\text{ V}$ .

[4]  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V.

11.1. Waveform and test circuit

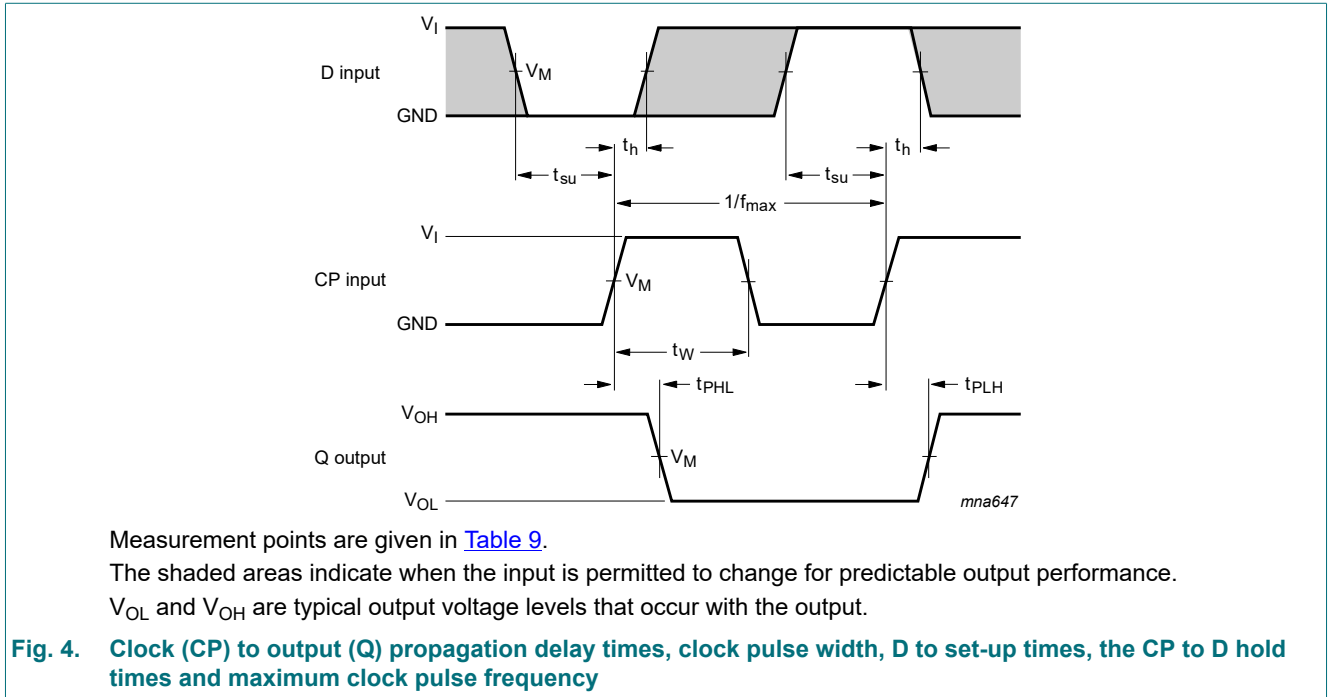
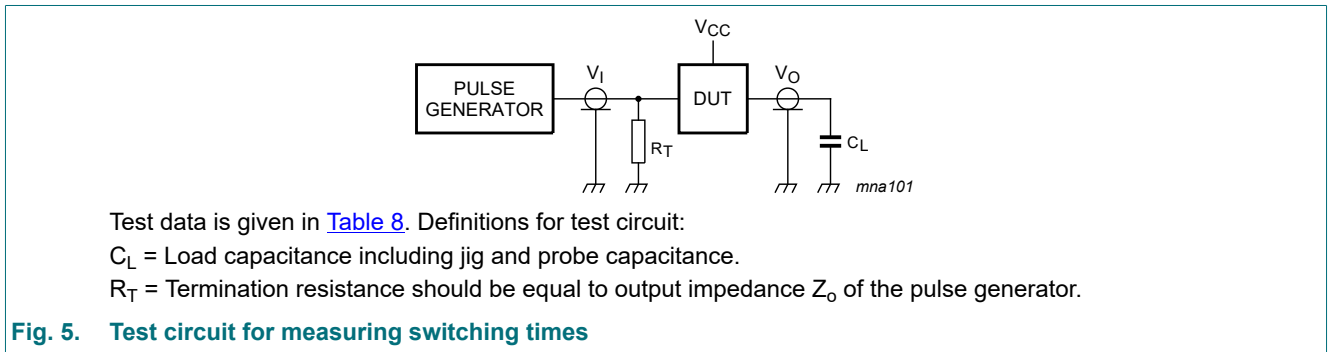


Table 9. Measurement points

Type	Inputs		Output
	$V_I$	$V_M$	$V_M$
74AHC1G79-Q100	GND to $V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT1G79-Q100	GND to 3.0 V	1.5 V	$0.5 \times V_{CC}$



## 12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



Fig. 6. Package outline SOT353-1 (TSSOP5)



Plastic surface-mounted package; 5 leads

SOT753

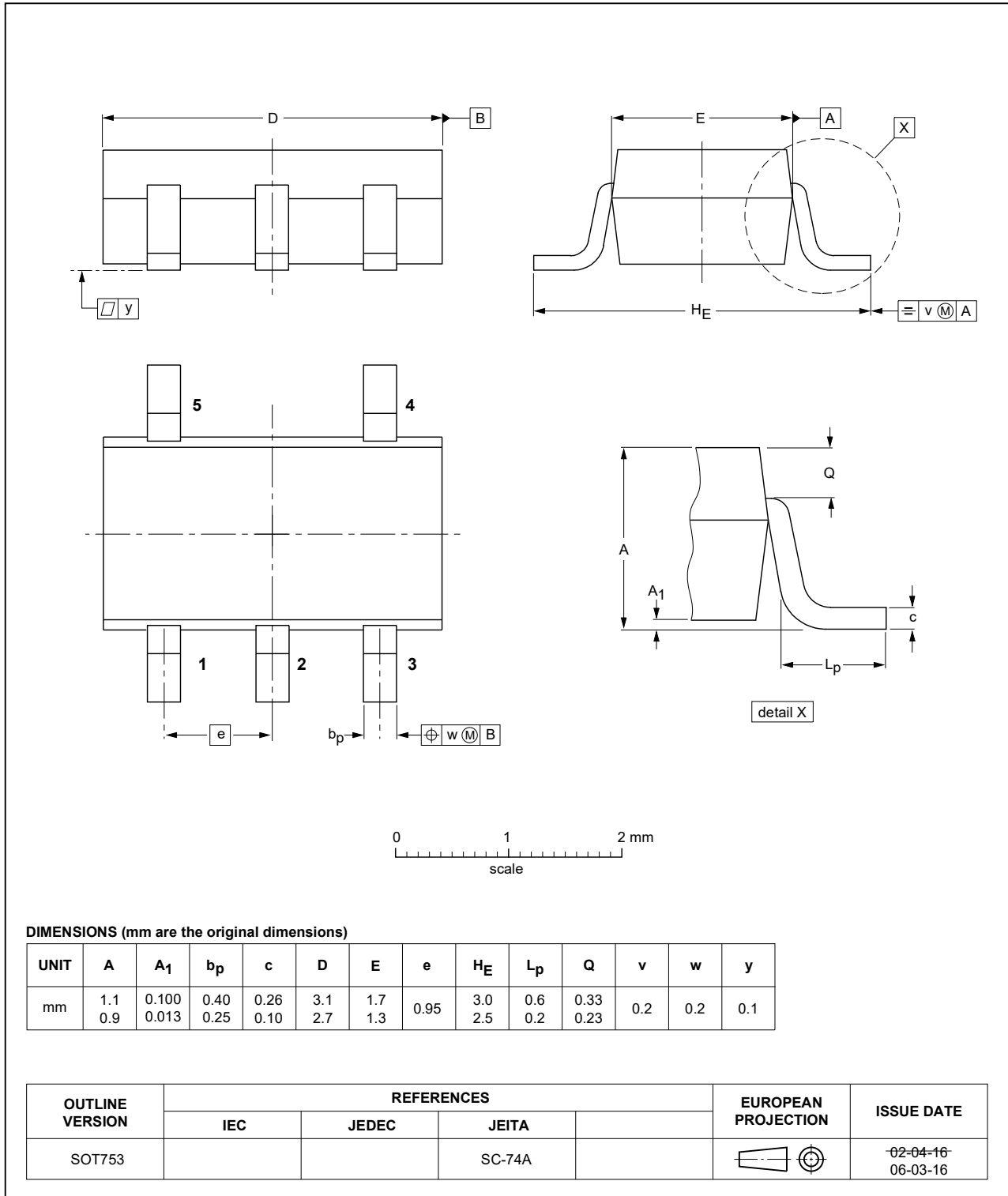


Fig. 7. Package outline SOT753 (SC-74A)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G79_Q100 v.5	20230920	Product data sheet	-	74AHC_AHCT1G79_Q100 v.4
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74AHC_AHCT1G79_Q100 v.4	20220111	Product data sheet	-	74AHC_AHCT1G79_Q100 v.3
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">SOT353-1</a>: Package outline drawing updated.</li> </ul>			
74AHC_AHCT1G79_Q100 v.3	20210830	Product data sheet	-	74AHC_AHCT1G79_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>• <a href="#">Section 4</a>: marking code corrected.</li> <li>• <a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74AHC_AHCT1G79_Q100 v.2	20140923	Product data sheet	-	74AHC_AHCT1G79_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 4</a>: table note added.</li> </ul>			
74AHC_AHCT1G79_Q100 v.1	20130516	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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