DRV8833C 双路 H 桥电机驱动器

1 特性

- 带电流控制的双 H 桥电机驱动器
  - 1 个或 2 个直流电机或者 1 个步进电机
  - 低导通电阻：高侧 + 低侧 (HS + LS) = 1735mΩ（25°C 时的典型值）
- 输出电流能力（V_M = 5V，25°C 时）
  - 散热薄型小外形尺寸 PWP (HTSSOP) 封装
    - 每个 H 桥的均方根 (RMS) 电流为 0.7A，峰值 1A
    - 并行模式下 RMS 为 1.4A
  - 四方扁平无引线 RTE (QFN) 封装
    - 每个 H 桥的均方根 (RMS) 电流为 0.6A，峰值 1A
    - 并行模式下 RMS 为 1.2A
- 宽电源电压范围
  - 2.7V 至 10.8V
- 集成电流调节
- 简易脉宽调制 (PWM) 接口
- 1.6μA 低电流睡眠模式（电压 5V 时）
- 小型封装尺寸
  - 16HTSSOP (PowerPAD™) 5.00 × 6.40mm
  - 16 QFN (PowerPAD) 3.00 × 3.00mm
- 保护特性
  - V_M 欠压闭锁 (UVLO)
  - 过流保护 (OCP)
  - 热关断 (TSD)
  - 故障指示引脚 (nFAULT)

2 应用

- 销售点打印机
- 视频安保摄像机
- 办公自动化设备
- 游戏机
- 机器人
- 电池供电式玩具

3 说明

DRV8833C 为玩具、打印机及其他机电一体化应用提供了一款双桥电机驱动器解决方案。

该器件具有两个 H 桥驱动器，能够驱动两个直流电刷电机、一个双极性步进电机、螺线管或其它电感性负载。

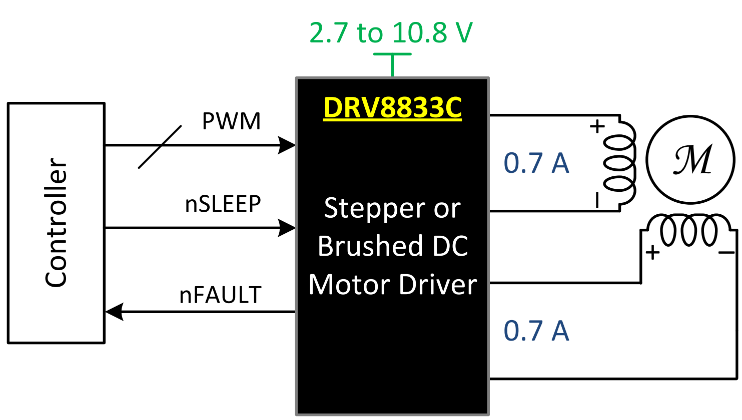
每个 H 桥输出都包括一对 N 通道和 P 通道金属氧化物半导体场效应晶体管 (MOSFET) 以及用于调节绕组电流的电路。 借助正确的印刷电路板 (PCB) 设计，DRV8833C 的每个 H 桥能够持续驱动高达 700mA RMS（或 DC）（在 25°C 采用 5V V_M 电源时）。该器件可支持每个 H 桥高达 1A 的峰值电流。在较低的 V_M 电压条件下，电流能力略有下降。

输出引脚发生故障时，还可提供用于过流保护、短路保护、UVLO 和过热保护的内部关断功能。 另外，还提供了一种低功耗睡眠模式。

器件信息(1)

部件号	封装	封装尺寸（标称值）
DRV8833C	HTSSOP (16)	5.00mm x 6.40mm
	四方扁平无引线 (QFN) (16)	3.00mm x 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

目录

4 修订历史记录

日期	修订版本	注释
2014 年 8 月	*	最初发布。

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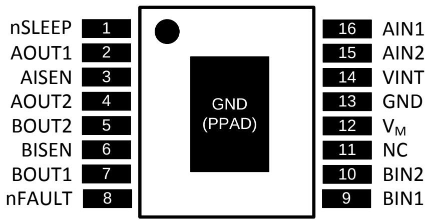
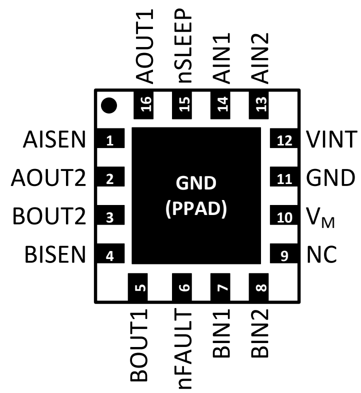
5 Pin Configuration and Functions

HTSSOP (PWP)
16 Pins
Top View



QFN (RTE)
16 Pins
Top View



Pin Functions

PIN			TYPE	DESCRIPTION	
NAME	PWP	RTE			
POWER AND GROUND					
GND	13	11	PWR	Device ground	Both the GND pin and device PowerPAD must be connected to ground
VINT	14	12	—	Internal regulator (3.3 V)	Internal supply voltage; bypass to GND with 2.2-μF, 6.3-V capacitor
V_M	12	10	PWR	Power supply	Connect to motor supply voltage; bypass to GND with a 10-μF (minimum) capacitor rated for V_M
CONTROL					
AIN1	16	14	I	H-bridge A PWM input	Controls the state of AOUT1 and AOUT2; internal pulldown
AIN2	15	13			
BIN1	9	7	I	H-bridge B PWM input	Controls the state of BOUT1 and BOUT2; internal pulldown
BIN2	10	8			
nSLEEP	1	15	I	Sleep mode input	Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown
STATUS					
nFAULT	8	6	OD	Fault indication pin	Pulled logic low with fault condition; open-drain output requires an external pullup
OUTPUT					
AISEN	3	1	O	Bridge A sense	Sense resistor to GND sets PWM current regulation level (see *PWM Motor Drivers*)
AOUT1	2	16	O	Bridge A output	Positive current is AOUT1 → AOUT2
AOUT2	4	2			
BISEN	6	4	O	Bridge B sense	Sense resistor to GND sets PWM current regulation level (see *PWM Motor Drivers*)
BOUT1	7	5	O	Bridge B output	Positive current is BOUT1 → BOUT2
BOUT2	5	3			

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External Components

Component	Pin 1	Pin 2	Recommended
C_{VM}	V_M	GND	10-µF(1) ceramic capacitor rated for V_M
C_{VINT}	VINT	GND	6.3-V, 2.2-µF ceramic capacitor
R_{nFAULT}	VINT(2)	nFAULT	>1 kΩ
R_{AISEN}	AISEN	GND	Sense resistor, see *Typical Application* for sizing
R_{BISEN}	BISEN	GND	Sense resistor, see *Typical Application* for sizing

(1) Proper bulk capacitance sizing depends on the motor power.
(2) nFAULT may be pulled up to an external supply rated < 5.5 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	Power supply (V_M)	–0.3	11.8	V
	Internal regulator (VINT)	–0.3	3.8	V
	Control pins (AIN1, AIN2, BIN1, BIN2, nSLEEP, nFAULT)	–0.3	7	V
	Continuous phase node pins (AOUT1, AOUT2, BOUT1, BOUT2)	–0.3	V_M + 0.5	V
	Pulsed 10 µs phase node pins (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_M + 1	V
	Continuous shunt amplifier input pins (AISEN, BISEN)	–0.3	0.5	V
	Pulsed 10 µs shunt amplifier input pins (AISEN, BISEN)	–1	1	V
	Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2, AISEN, BISEN)	Internally limited		A
T_J	Operating junction temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_M	Power supply voltage range(1)		2.7	10.8	V
V_I	Logic level input voltage		0	5.5	V
I_{RMS}	Motor RMS current(2)	PWP package	0	0.7	A
		RTE package	0	0.6	A
f_{PWM}	Applied PWM signal to AIN1, AIN2, BIN1, or BIN2		0	200	kHz
T_A	Operating ambient temperature		–40	85	°C

(1) Note that when V_M is below 5 V, $R_{DS(ON)}$ increases and maximum output current is reduced.
(2) Power dissipation and thermal limits must be observed.

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6.4 Thermal Information

THERMAL METRIC(1)		DRV8833C HTSSOP 16 PINS	DRV8833C QFN 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.5	44.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.8	16.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.5	16.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.8	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_M, VINT)						
V_M	V_M operating voltage		2.7		10.8	V
I_{VM}	V_M operating supply current	V_M = 5 V, xINx low, nSLEEP high		1.7	3	mA
I_{VMQ}	V_M sleep mode supply current	V_M = 5 V, nSLEEP low		1.6	2.7	μA
t_{SLEEP}	Sleep time	nSLEEP low to sleep mode		10		μs
t_{WAKE}	Wake-up time	nSLEEP high to output transition		155		μs
t_{ON}	Turn-on time	V_M > V_{UVLO} to output transition		25		μs
VINT	Internal regulator voltage	V_M = 5 V	3	3.3	3.6	V
CONTROL INPUTS (AIN1, AIN2, BIN1, BIN2, nSLEEP)						
V_{IL}	Input logic low voltage	xINx	0		0.7	V
		nSLEEP	0		0.5	
V_{IH}	Input logic high voltage	xINx	2		5.5	V
		nSLEEP	2.5		5.5	
V_{HYS}	Input logic hysteresis		350	400	650	mV
I_{IL}	Input logic low current	V_{IN} = 0 V	–1		1	μA
I_{IH}	Input logic high current	V_{IN} = 5 V			50	μA
R_{PD}	Pulldown resistance	xINx	100	150	250	kΩ
		nSLEEP	380	500	750	
t_{DEG}	Input deglitch time			575		ns
t_{PROP}	Propagation delay INx to OUTx	V_M = 5 V		1.2		μs
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic high leakage	R_{PULLUP} = 1 kΩ to 5 V	–1		1	μA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on-resistance	V_M = 5 V, I = 0.2 A, T_A = 25°C		1180		mΩ
		V_M = 5 V, I = 0.2 A, T_A = 85°C(1)		1400	1475	
		V_M = 2.7 V, I = 0.2 A, T_A = 25°C		1550		
		V_M = 2.7 V, I = 0.2 A, T_A = 85°C(1)		1875	1975	
$R_{DS(ON)}$	Low-side FET on-resistance	V_M = 5 V, I = 0.2 A, T_A = 25°C		555		mΩ
		V_M = 5 V, I = 0.2 A, T_A = 85°C(1)		675	705	
		V_M = 2.7 V, I = 0.2 A, T_A = 25°C		635		
		V_M = 2.7 V, I = 0.2 A, T_A = 85°C(1)		775	815	

(1) Not tested in production; based on design and characterization data

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OFF}	Off-state leakage current	V_M = 5 V	–1		1	μA
t_{RISE}	Output rise time	V_M = 5 V; R_L = 16 Ω to GND		70		ns
t_{FALL}	Output fall time	V_M = 5 V; R_L = 16 Ω to V_M		80		ns
t_{DEAD}	Output dead time	Internal dead time		450		ns
PWM CURRENT CONTROL (AISEN, BISEN)						
V_{TRIP}	xISEN trip voltage		160	200	240	mV
t_{OFF}	Current control constant off time	Internal PWM constant off time		20		μs
PROTECTION CIRCUITS						
V_{UVLO}	V_M undervoltage lockout	V_M falling; UVLO report			2.6	V
		V_M rising; UVLO recovery			2.7	
$V_{UVLO,HYS}$	V_M undervoltage hysteresis	Rising to falling threshold		90		mV
I_{OCP}	Overcurrent protection trip level		1			A
t_{DEG}	Overcurrent deglitch time			2.3		μs
t_{OCP}	Overcurrent protection period			1.4		ms
T_{TSD} (1)	Thermal shutdown temperature	Die temperature, T_J	150			°C
T_{HYS}	Thermal shutdown hysteresis	Die temperature, T_J		20		°C

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6.6 Typical Characteristics

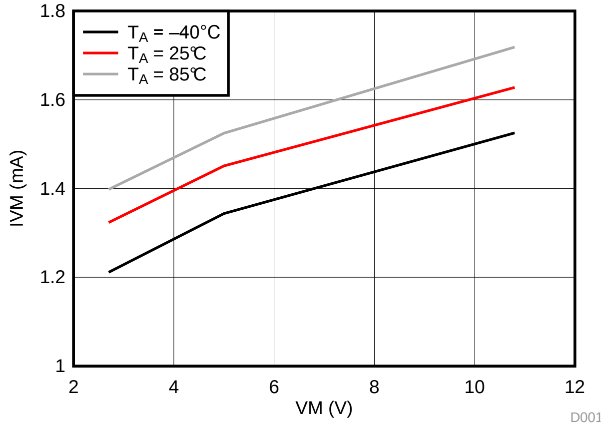


Figure 1. Supply Current

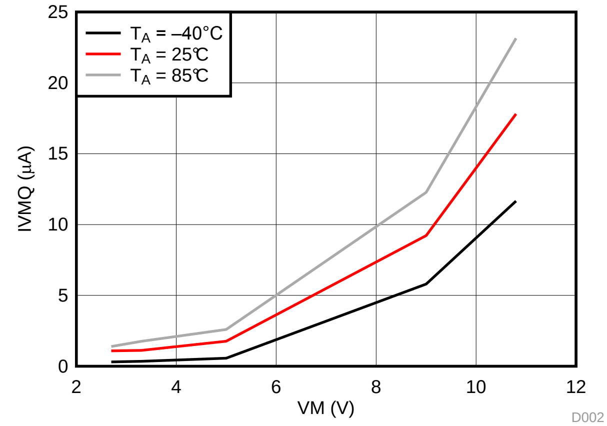


Figure 2. Sleep Current

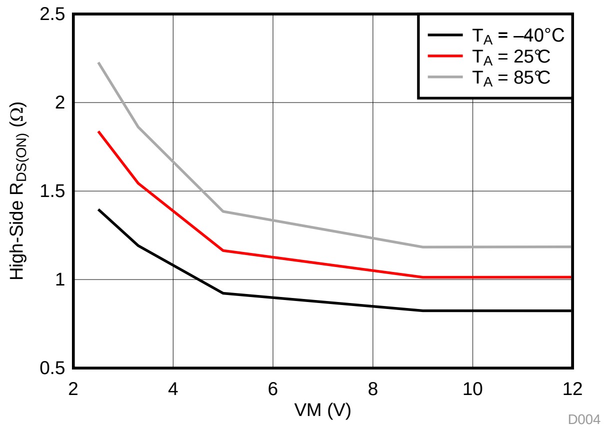


Figure 3. High-Side $R_{DS(ON)}$

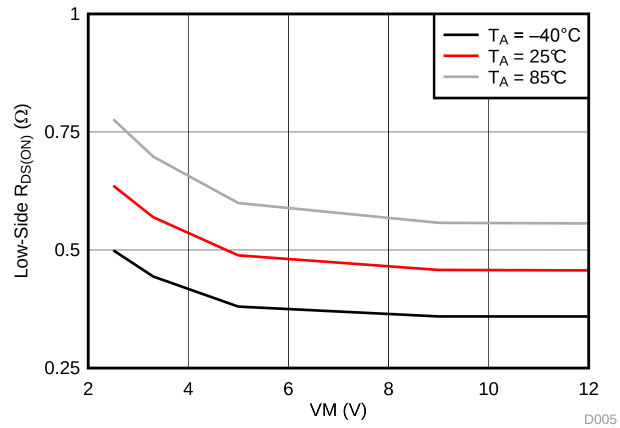


Figure 4. Low-Side $R_{DS(ON)}$

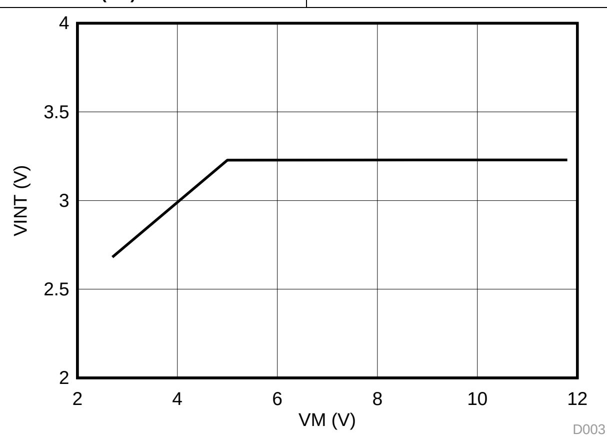


Figure 5. VINT Over V_M

7 Detailed Description

7.1 Overview

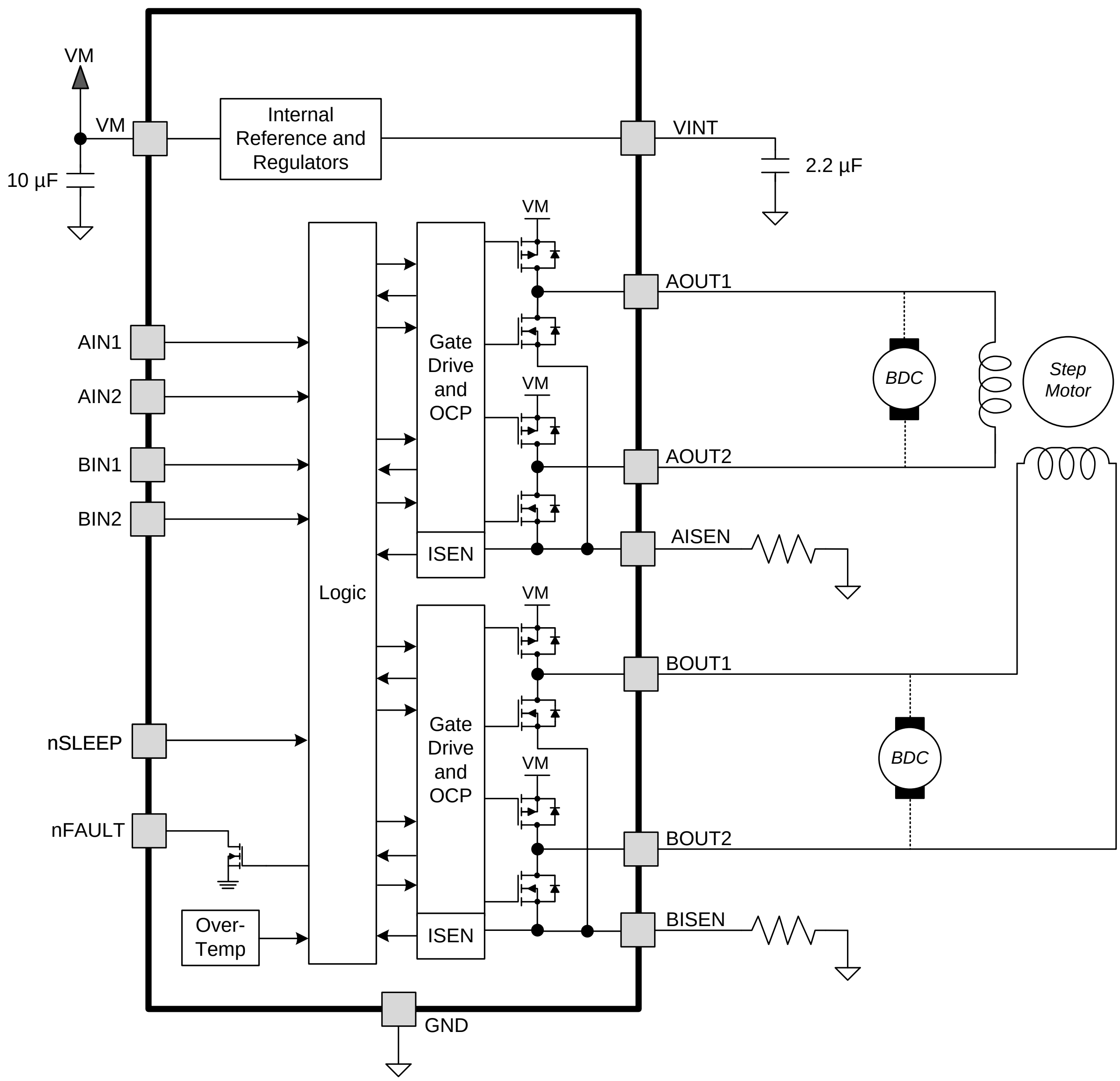
The DRV8833C device is an integrated motor driver solution for brushed DC or bipolar stepper motors. The device integrates two PMOS + NMOS H-bridges and current regulation circuitry. The DRV8833C can be powered with a supply voltage from 2.7 to 10.8 V and can provide an output current up to 700 mA RMS.

A simple PWM interface allows easy interfacing to the controller circuit.

The current regulation is a 20-µs fixed off-time slow decay.

The device includes a low-power sleep mode, which lets the system save power when not driving the motor.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8833C contains drivers for two full H-bridges. Figure 6 shows a block diagram of the circuitry.

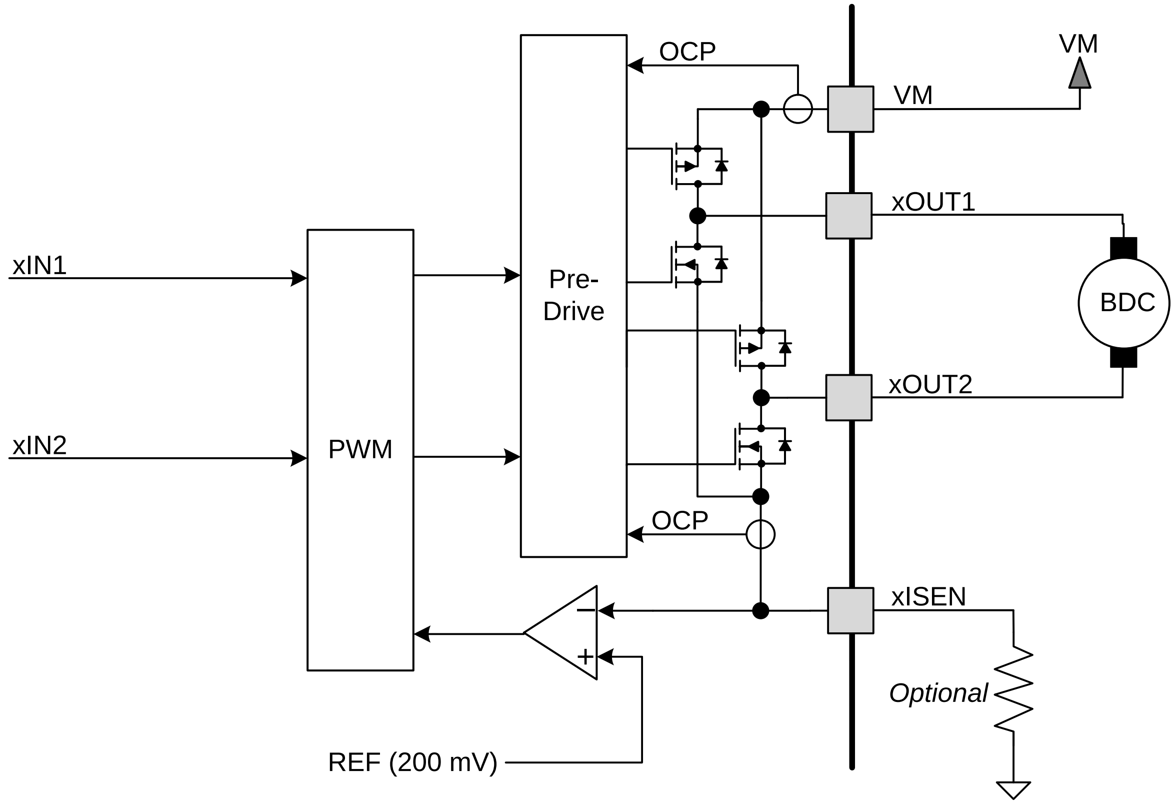

Figure 6. H-Bridge and Current-Chopping Circuitry

7.3.2 Bridge Control and Decay Modes

The AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2 outputs; similarly, the BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2 outputs (see Table 1).

Table 1. H-Bridge Logic

xIN1	xIN2	xOUT1	xOUT2	FUNCTION
0	0	Z	Z	Coast / fast decay
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake / slow decay

The inputs can also be used for PWM control of the motor speed. When controlling a winding with PWM and the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow (called recirculation current). To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay. In fast-decay mode, the H-bridge is disabled and recirculation current flows through the body diodes. In slow-decay mode, the motor winding is shorted by enabling both low-side FETs.

To externally pulse-width modulate the bridge in fast-decay mode, the PWM signal is applied to one xIN pin while the other is held low; to use slow-decay mode, one xIN pin is held high. See Table 2 for more information.

Table 2. PWM Control of Motor Speed

xIN1	xIN2	FUNCTION
PWM	0	Forward PWM, fast decay
1	PWM	Forward PWM, slow decay
0	PWM	Reverse PWM, fast decay
PWM	1	Reverse PWM, slow decay

The internal current control is still enabled when applying external PWM to xIN. To disable the current control when applying external PWM, the xISEN pins should be connected directly to ground. Figure 7 show the current paths in different drive and decay modes.

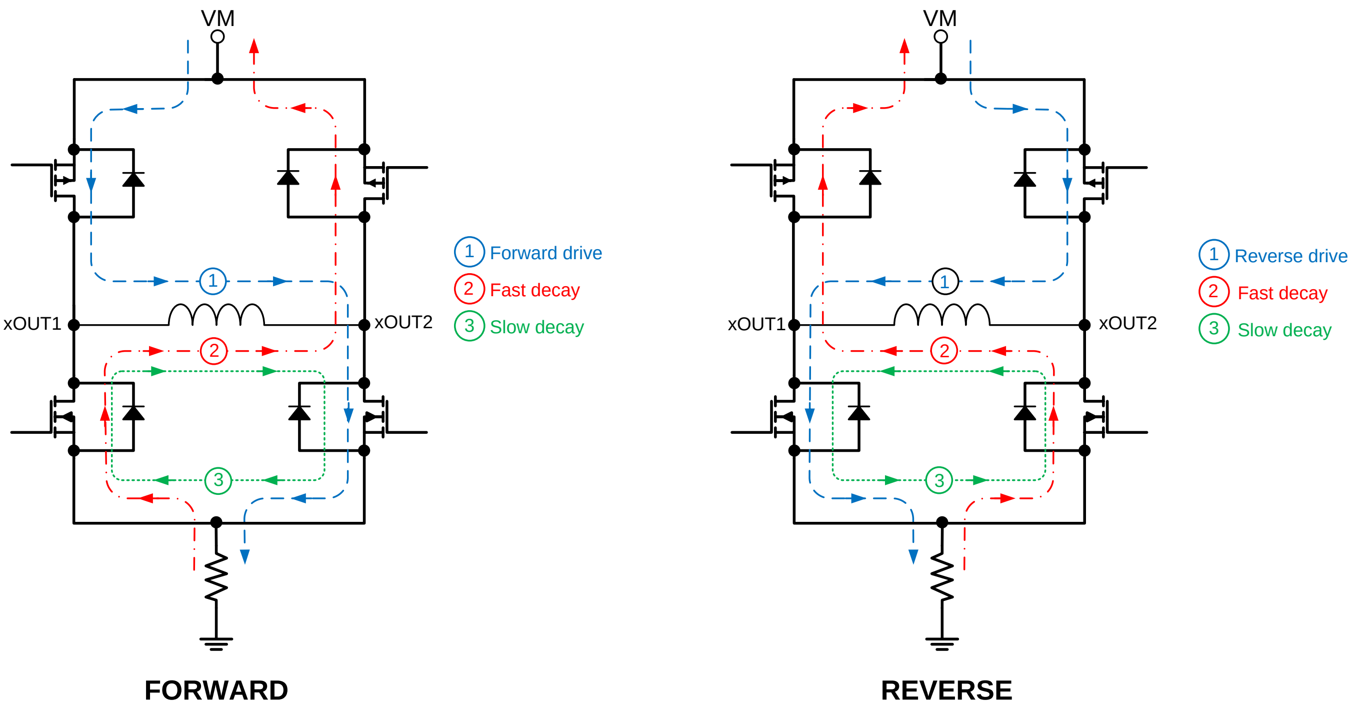

Figure 7. Drive and Decay Modes

7.3.3 Current Control

The current through the motor windings may be limited, or controlled, by a 20-µs constant off-time PWM current regulation, or current chopping. For DC motors, current control is used to limit the start-up and stall current of the motor. For stepper motors, current control is often used at all times.

When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle. Note that immediately after the output is enabled, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs.

The PWM chopping current is set by a comparator that compares the voltage across a current sense resistor connected to the xISEN pins with a reference voltage. The reference voltage, V_{TRIP}, is is fixed at 200 mV nominally.

The chopping current is calculated as in Equation 1.

$$I_{CHOP} = \frac{200\ \text{mV}}{R_{XISEN}} \tag{1}$$

Example: If a 1-Ω sense resistor is used, the chopping current will be 200 mV / 1 Ω = 200 mA.

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NOTE

If current control is not needed, the xISEN pins should be connected directly to ground.

7.3.4 Decay Mode

After the chopping current threshold is reached, the H-bridge switches to slow-decay mode. This state is held for t_{off} (20 µs) until the next cycle to turn on the high-side MOSFETs.

7.3.5 Slow Decay

In slow-decay mode, the high-side MOSFETs are turned off and both of the low-side MOSFETs are turned on. The motor current decreases while flowing in the two low-side MOSFETs until reaching its fixed off time (typically 20 µs). After that, the high-side MOSFETs are enabled to increase the winding current again.

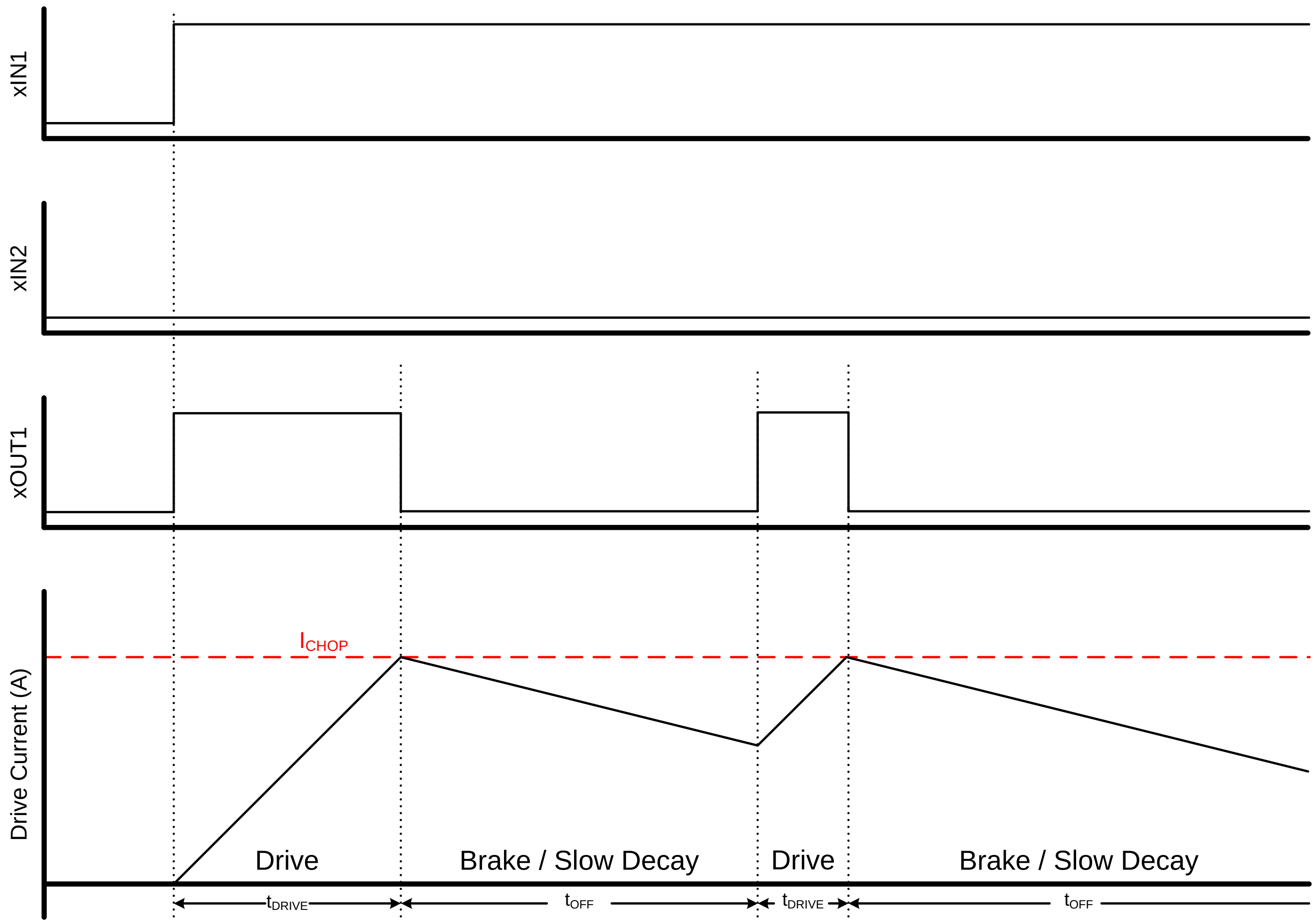

Figure 8. Current Chopping Operation

7.3.6 Sleep Mode

Driving nSLEEP low puts the device into a low-power sleep state. In this state, the H-bridges are disabled, all internal logic is reset, and all internal clocks are stopped. All inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time, t_{WAKE}, needs to pass before the motor driver becomes fully operational. To make the board design simple, the nSLEEP can be pulled up to the supply (V_M). TI recommends to use a pullup resistor when this is done. This resistor limits the current to the input in case V_M is higher than 6.5 V. Internally, the nSLEEP pin has a 500-kΩ resistor to GND. It also has a clamping Zener diode that clamps the voltage at the pin at 6.5 V. Currents greater than 250 µA can cause damage to the input structure. Therefore, TI recommends a pullup resistor between 20 to 75 kΩ.

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7.3.7 Parallel Mode

The two H-bridges in the DRV8833C can be connected in parallel for double the current of a single H-bridge. The internal dead time in the DRV8833C prevents any risk of cross-conduction (shoot-through) between the two bridges due to timing differences between the two bridges. Figure 9 shows the connections.

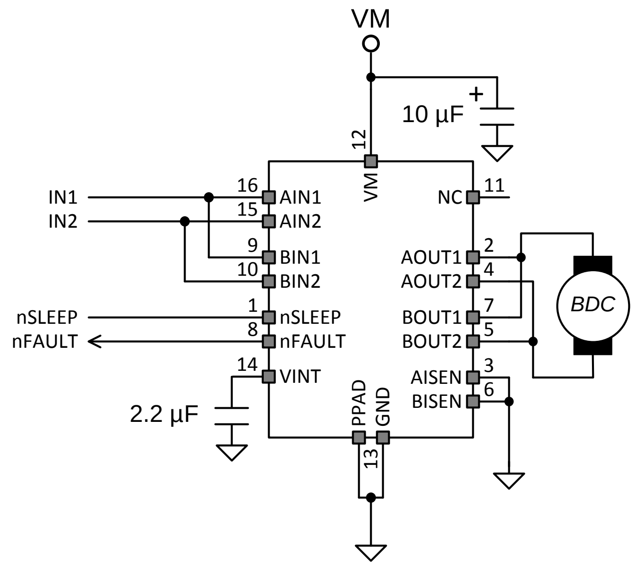

Figure 9. Parallel Mode Schematic

7.3.8 Protection Circuits

The DRV8833C is fully protected against overcurrent, overtemperature, and undervoltage events.

7.3.8.1 Overcurrent Protection (OCP)

An analog current limit (I_{OCP}) circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time (t_{DEG}), all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The driver is re-enabled after the OCP retry period (t_{OCP}) has passed. nFAULT becomes high again after the retry time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted. Note that only the H-bridge in which the OCP is detected will be disabled while the other bridge functions normally.

Overcurrent conditions are detected independently on both high-side and low-side devices; a short to ground, supply, or across the motor winding all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, so it functions even without presence of the xISEN resistors.

7.3.8.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature has fallen below the specified hysteresis (T_{HYS}), operation automatically resumes. The nFAULT pin is released after operation has resumed.

7.3.8.3 UVLO

If at any time the voltage on the V_M pin falls below the UVLO threshold voltage, V_{UVLO}, all circuitry in the device is disabled, and all internal logic is reset. Operation resumes when V_M rises above the UVLO threshold. The nFAULT pin is not driven low during an undervoltage condition.

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Table 3. Device Protection

Fault	Condition	Error Report	H-Bridge	Internal Circuits	Recovery
V_M undervoltage (UVLO)	V_M < 2.6 V	None	Disabled	Disabled	V_M > 2.7 V
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	FAULTn	Disabled	Operating	OCP
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	FAULTn	Disabled	Operating	$T_J < T_{TSD} – T_{HYS}$

7.4 Device Functional Modes

The DRV8833C is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled (Hi-Z). Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DRV8833C is brought out of sleep mode automatically if nSLEEP is brought logic high. Note that t_{WAKE} must elapse before the outputs change state after wake-up.

Table 4. Modes of Operation

Fault	Condition	H-Bridge	Internal Circuits
Operating	nSLEEP pin high	Operating	Operating
Sleep mode	nSLEEP pin low	Disabled	Disabled
Fault encountered	Any fault condition met	Disabled	See Table 3

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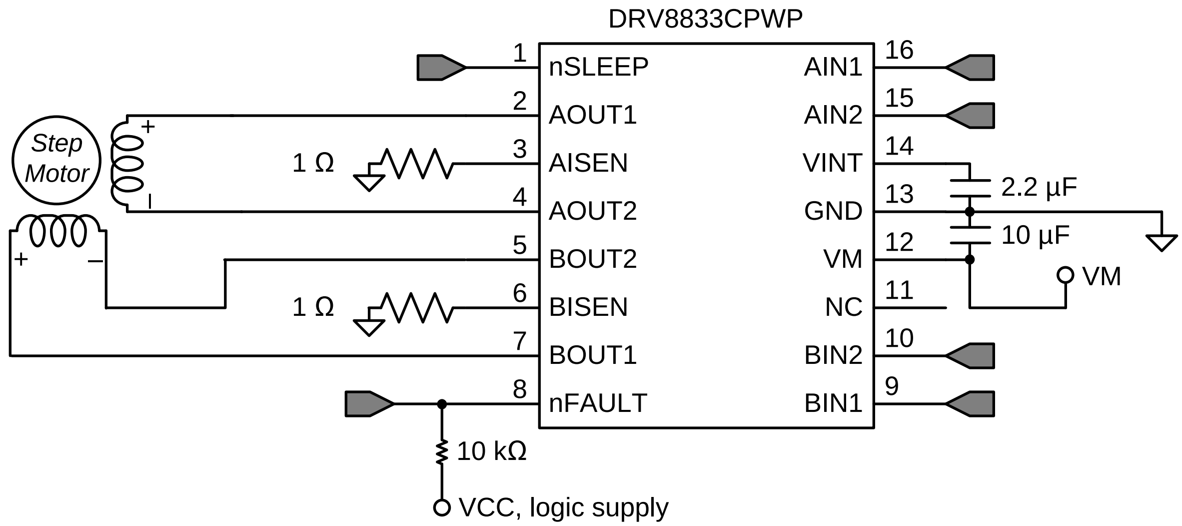
8 Application and Implementation

8.1 Application Information

The DRV8833C is used in stepper or brushed DC motor control. The following design procedure can be used to configure the DRV8833C in a bipolar stepper motor application.

8.2 Typical Application



8.2.1 Design Requirements

Table 5 gives design input parameters for system design.

Table 5. Design Parameters

Design Parameter	Reference	Example Value
Supply voltage	V_M	9 V
Motor winding resistance	R_L	12 Ω/phase
Motor winding inductance	L_L	10 mH/phase
Motor full step angle	θ_{step}	1.8 °/step
Target stepping level	n_m	2 (half-stepping)
Target motor speed	v	120 rpm
Target chopping current	I_{CHOP}	200 mA
Sense resistor	R_{ISEN}	1 Ω

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8833C requires the desired motor speed and stepping level. The DRV8833C can support full- and half-stepping modes using the PWM interface.

If the target motor speed is too high, the motor does not spin. Ensure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}\,(\text{steps/s}) = \frac{v(\text{rpm}) \times n_m\,(\text{steps}) \times 360°/\text{rot}}{\theta_{step}\,(°/\text{step}) \times 60\ \text{s/min}} \quad (2)$$

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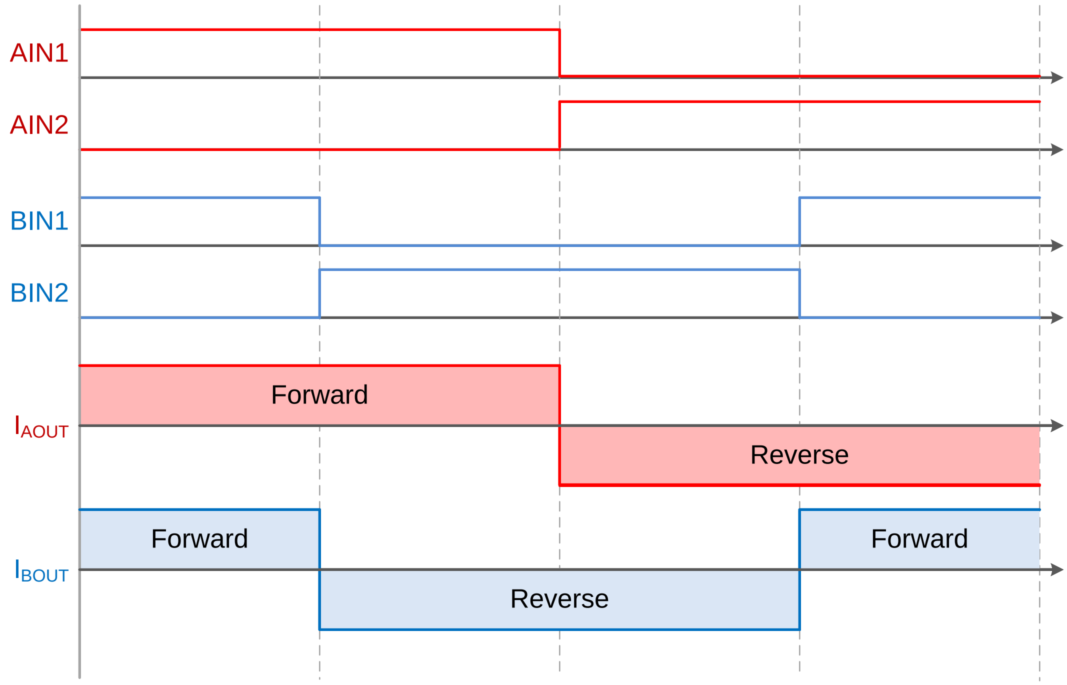

Figure 10. Full-Step Mode

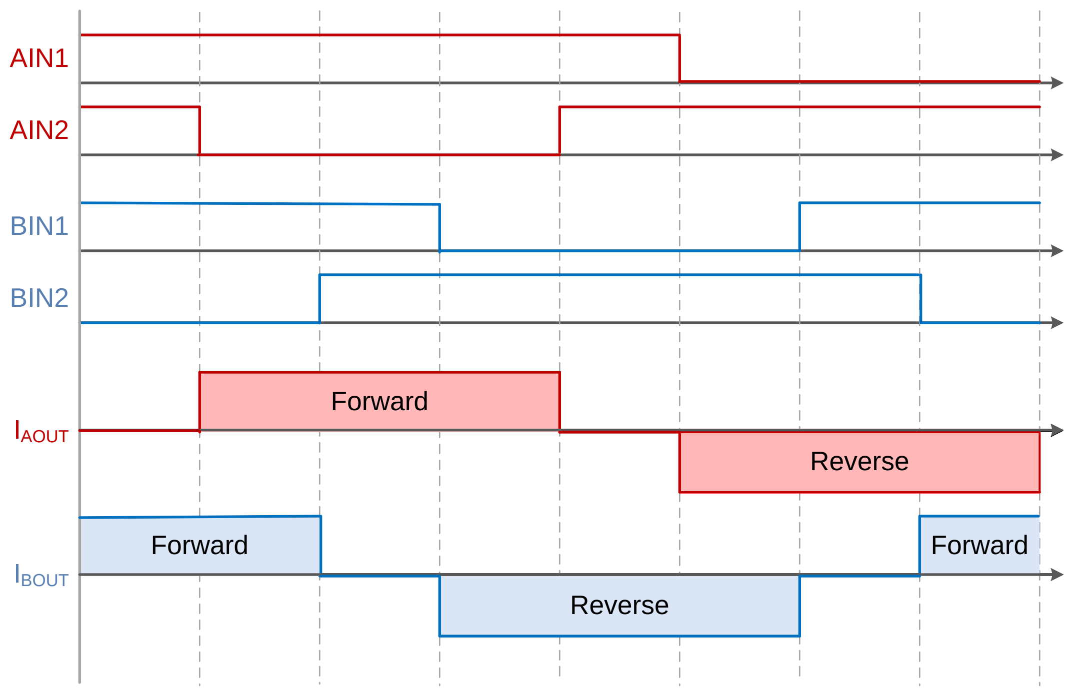

Figure 11. Half-Step Mode

8.2.2.2 Current Regulation

The chopping current (I_{CHOP}) is the maximum current driven through either winding. This quantity depends on the sense resistor value (R_{XISEN}).

$$I_{CHOP} = \frac{200\text{ mV}}{R_{XISEN}} \tag{3}$$

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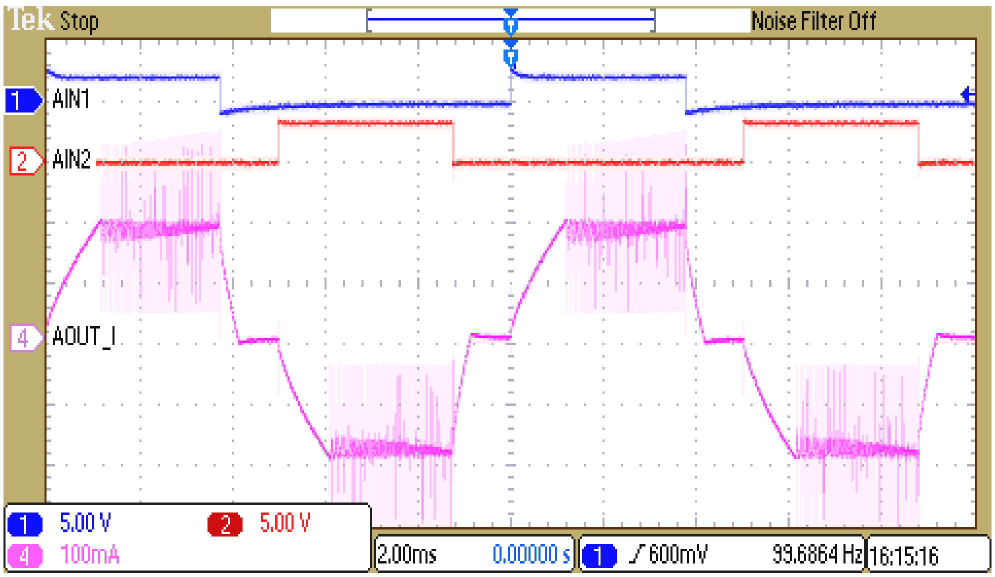
I_{CHOP} is set by a comparator which compares the voltage across R_{XISEN} to a reference voltage. Note that I_{CHOP} must follow Equation 4 to avoid saturating the motor.

$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + R_{DS(ON)}\ HS\ (\Omega) + R_{DS(ON)}\ LS\ (\Omega)} \quad (4)$$

where

- V_M is the motor supply voltage.
- R_L is the motor winding resistance.

8.2.3 Application Curve



A. Channel 1 is the AIN1 input PWM signal, and channel 2 is the AIN2 input PWM signal. BIN1 and BIN2 follow the same pattern, but are shifted by 90° from AIN1 and AIN2 as shown in Figure 11. Channel 4 is the output current in the direction AOUT1 → AOUT2. In forward and reverse drive, the current rises until it hits the current chopping limit of 200 mA, and is regulated at that level with fixed-off time current chopping.

Figure 12. ½ Stepping Operation

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9 Power Supply Recommendations

The DRV8833C is designed to operate from an input voltage supply (V_M) range between 2.7 to 10.8 V. A 10-µF ceramic capacitor rated for V_M must be placed as close to the DRV8833C as possible.

9.1 Sizing Bulk Capacitance for Motor Drive Systems

Bulk capacitance sizing is an important factor in motor drive system design. It depends on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. Size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate-sized bulk capacitor.

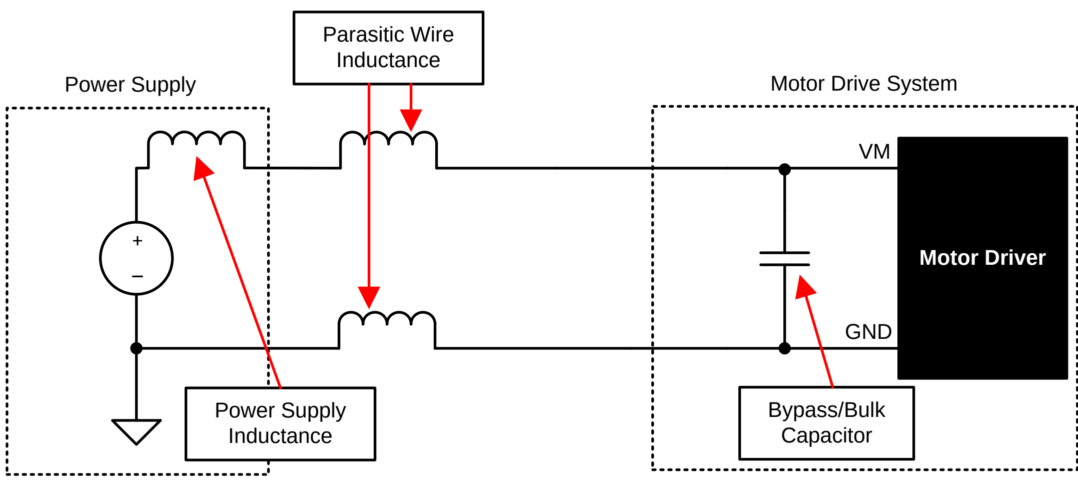

Figure 13. Setup of Motor Drive System With External Power Supply

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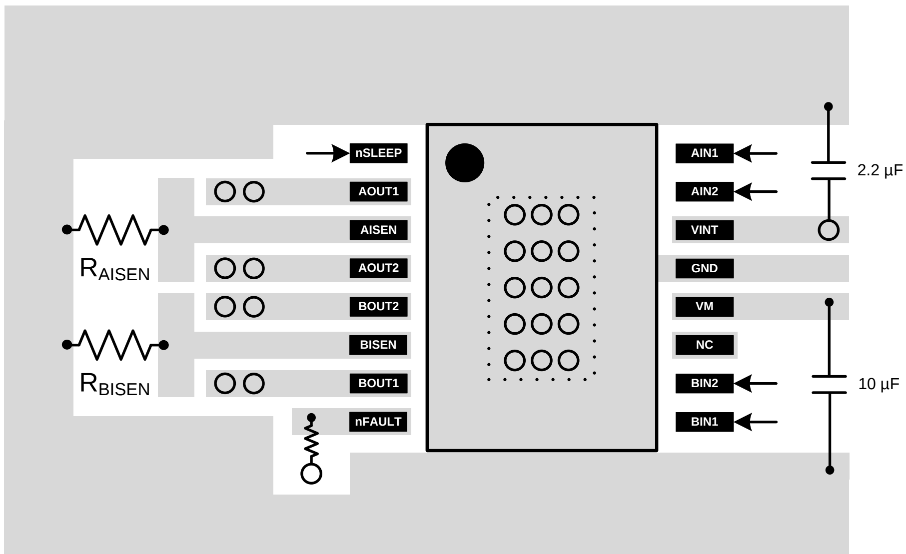
10 Layout

10.1 Layout Guidelines

Bypass the V_M terminal to GND using a low-ESR ceramic bypass capacitor with a recommended value of 10 µF rated for V_M. This capacitor should be placed as close to the V_M pin as possible with a thick trace or ground plane connection to the device GND pin and PowerPAD.

Bypass VINT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

10.2 Layout Example



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11 器件和文档支持

11.1 商标

PowerPAD is a trademark of Texas Instruments.

11.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8833CPWP	Obsolete	Production	HTSSOP (PWP) | 16	-	-	Call TI	Call TI	-40 to 85	8833C
DRV8833CPWPR	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	8833C
DRV8833CRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	8833C
DRV8833CRTET	Obsolete	Production	WQFN (RTE) | 16	-	-	Call TI	Call TI	-40 to 85	8833C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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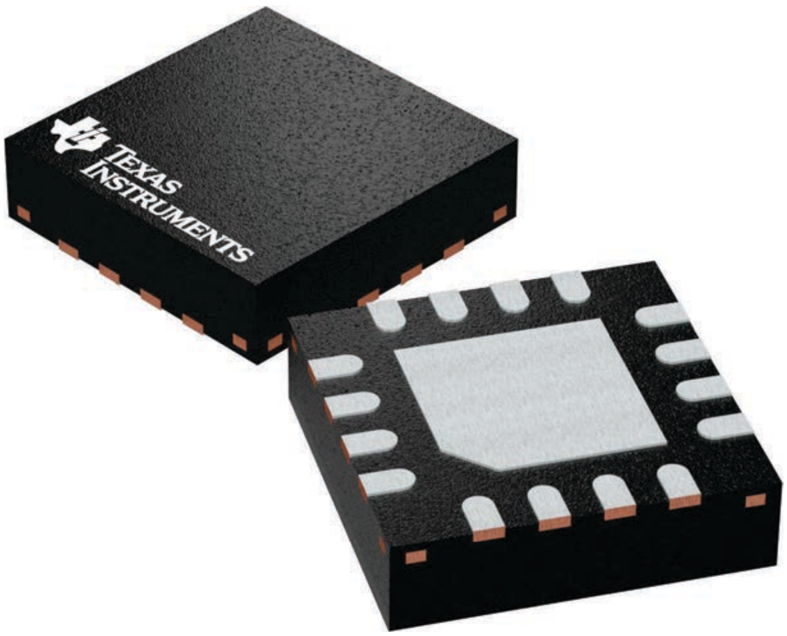
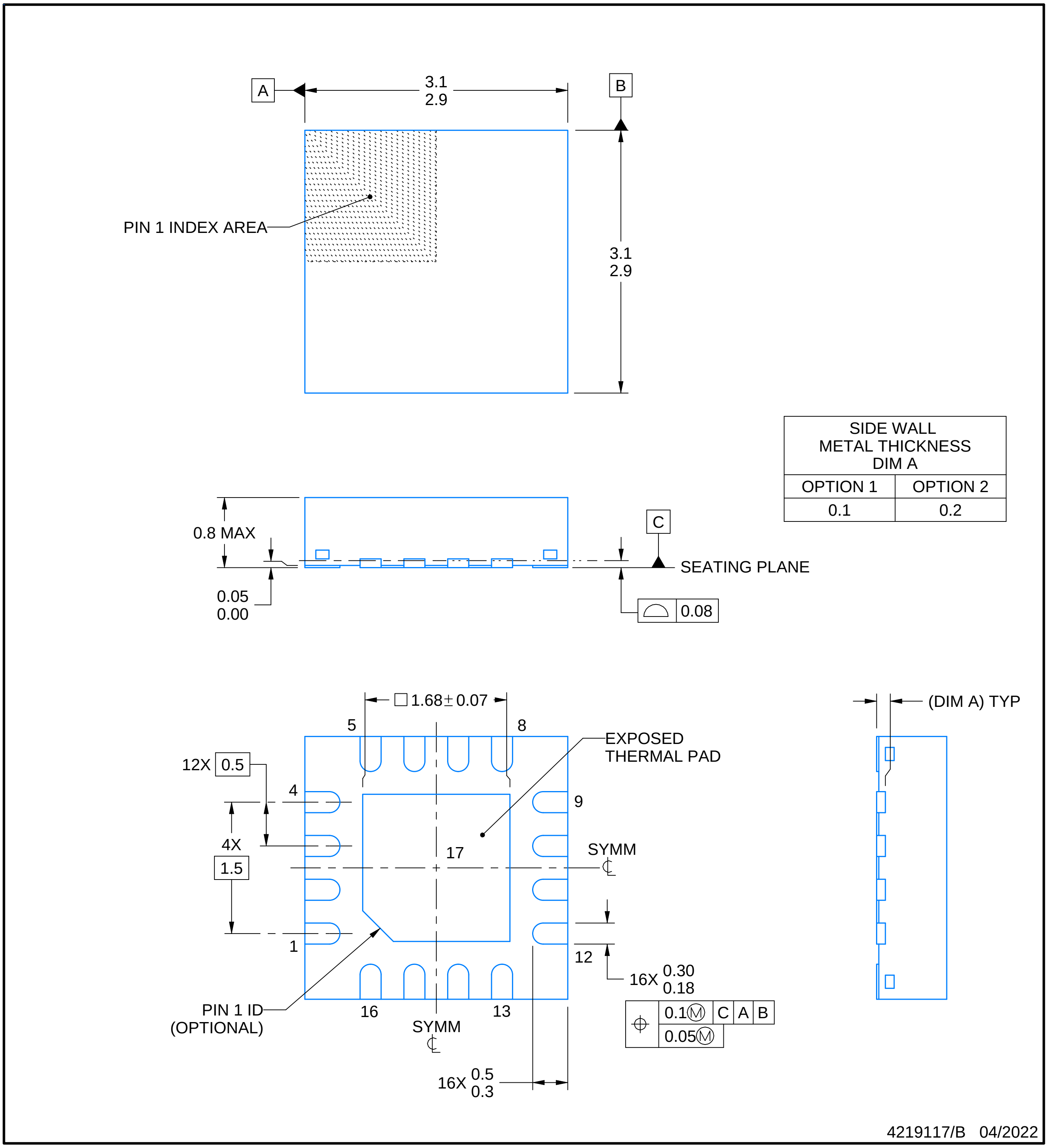
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

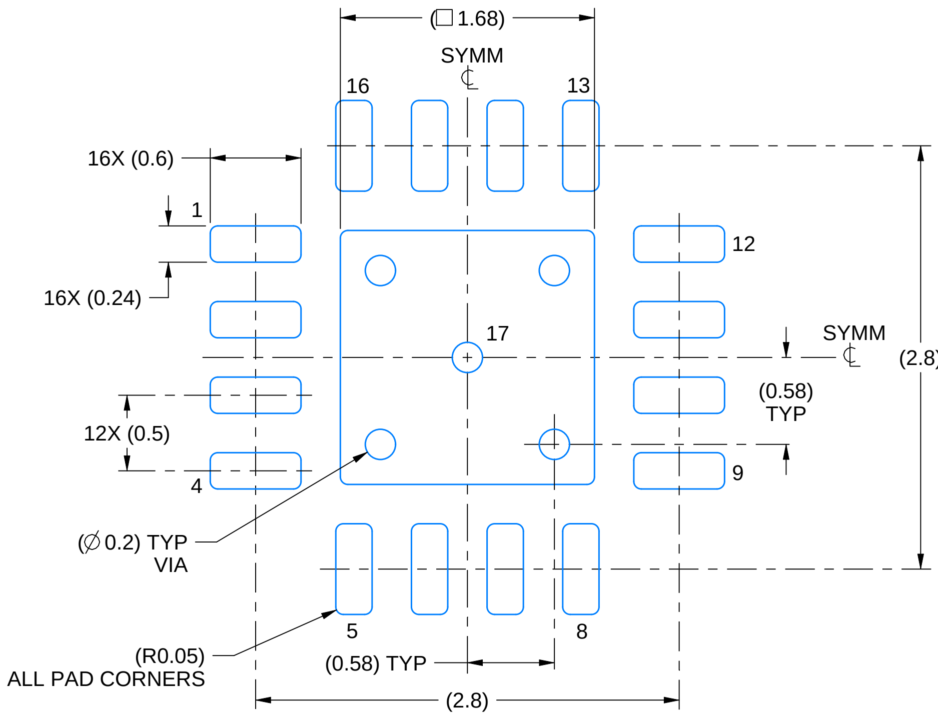




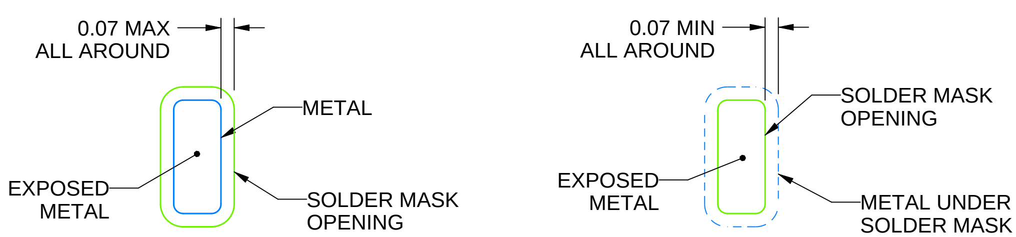
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

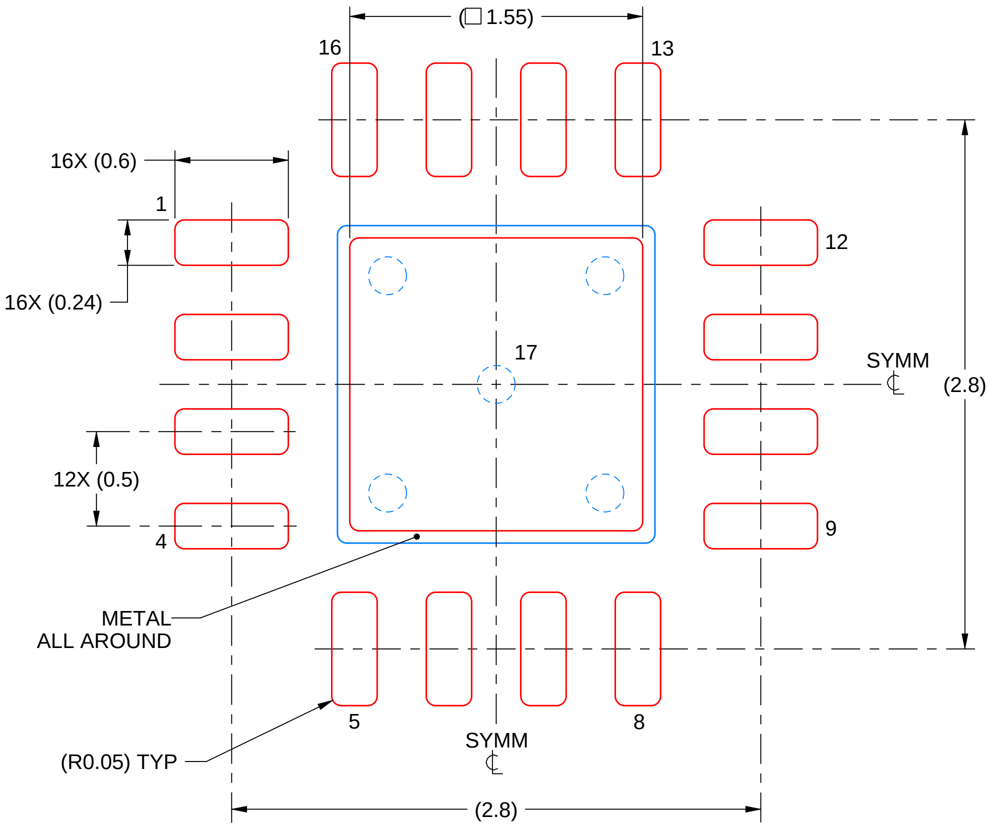
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

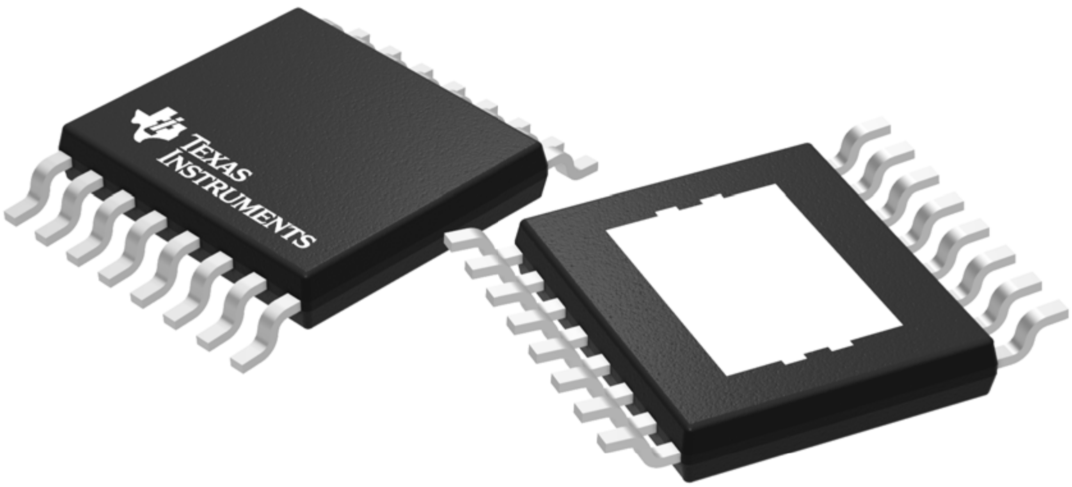
4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

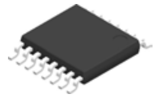
PWP 16 **PowerPAD™ TSSOP - 1.2 mm max height**

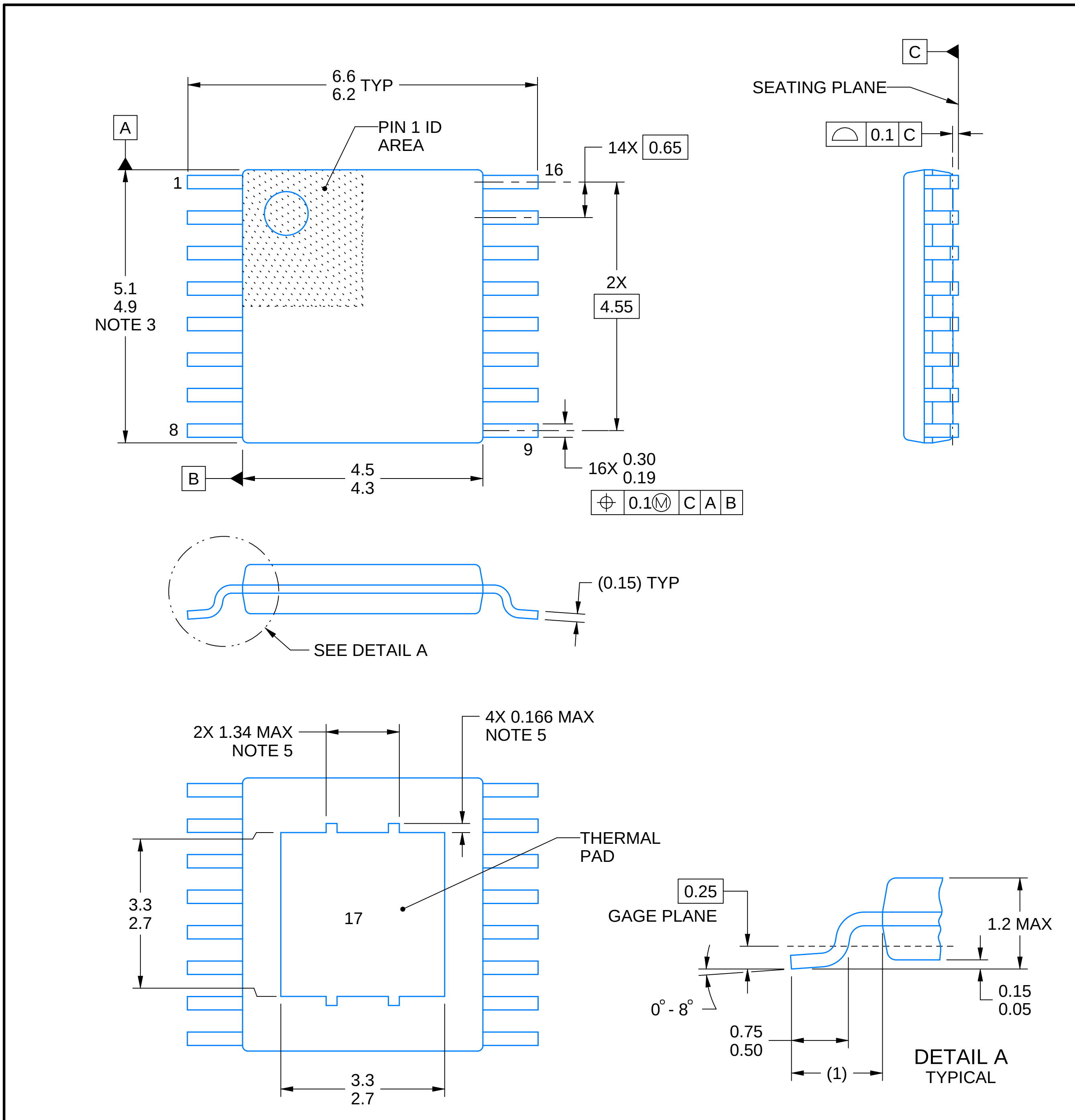
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073225-3/J





4214868/A 02/2017

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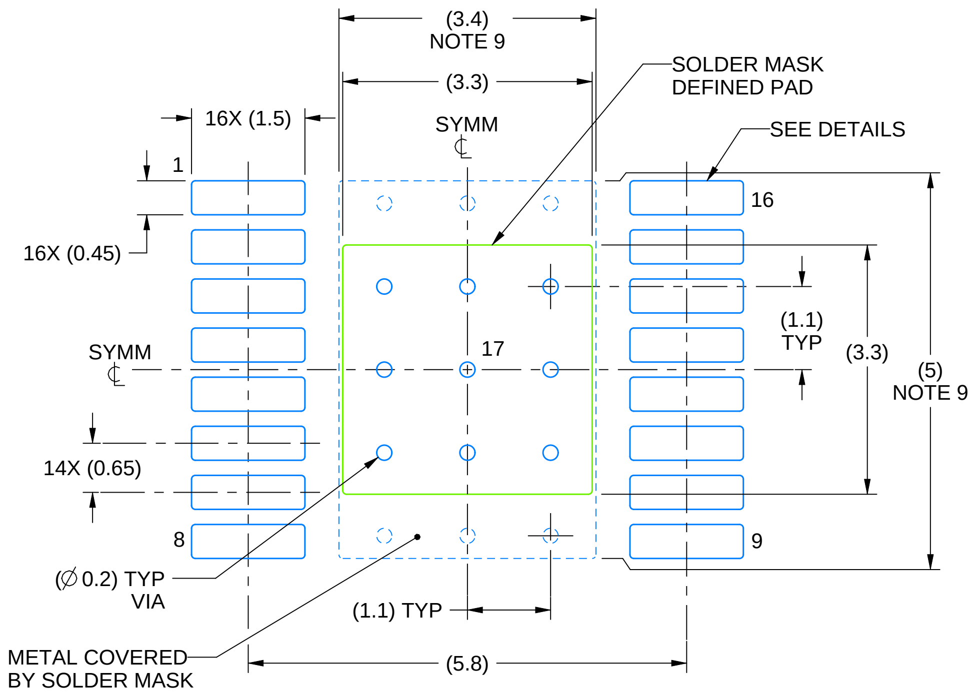
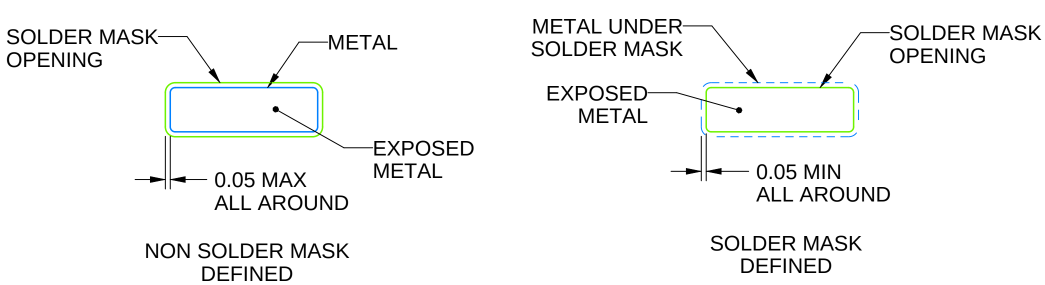
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

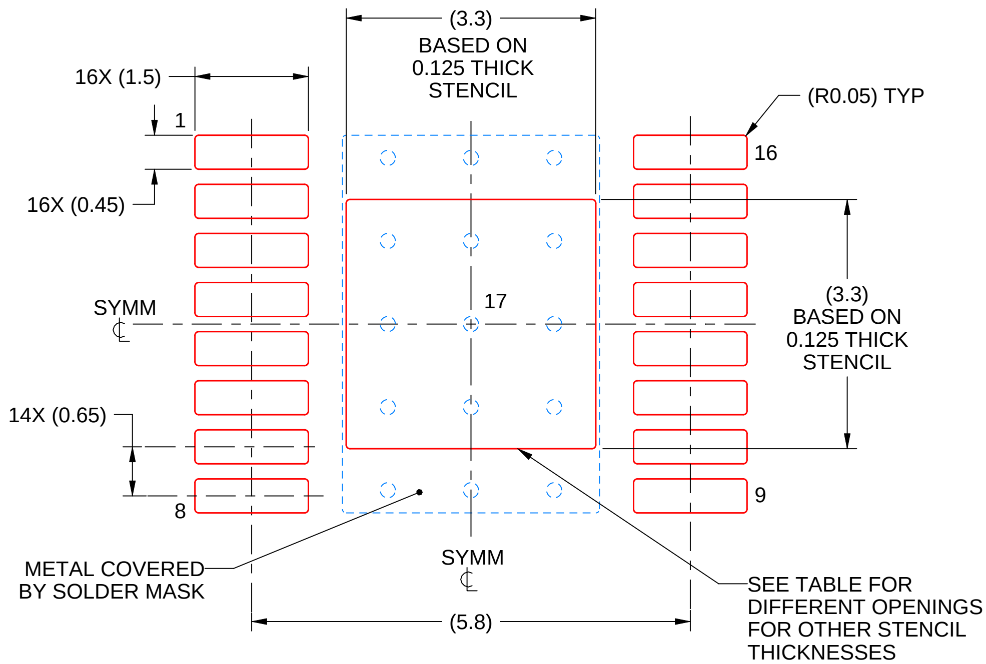


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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