TPD6E001 Low-Capacitance 6-Channel ESD-Protection for High-Speed Data Interfaces

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±8-kV IEC 61000-4-2 Contact Discharge
  - ±15-kV IEC 61000-4-2 Air-Gap Discharge
- I/O Capacitance: 1.5-pF (Typical)
- Low Leakage Current: 1-nA (Maximum)
- Low Supply Current: 1-nA (Typical)
- 0.9-V to 5.5-V Supply-Voltage Range
- Space-Saving RSE and RSF Package Options
- Alternate 2-, 3-, 4-Channel Options Available: TPD2E2U06, TPD3E001, and TPD4E1U06

2 Applications

- End Equipments
  - Portable Data Terminal
  - Industrial Monitor
  - IP Camera
  - Blood Glucose Meters
- Interfaces
  - SDIO
  - Precision Analog Interface
  - SVGA Connections
  - USB 2.0

3 Description

The TPD6E001 is a six-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array. The TPD6E001 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device has a 1.5-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces. The ultra low leakage current (<1 nA max) is suitable for precision analog measurements in applications like glucose meters and heart rate monitors.

The TPD6E001 is available in space saving RSE (UQFN) and RSF (WQFN) packages and is specified for –40°C to 85°C operation. Also see TPD2E2U06, TPD3E001, and TPD4E1U06 which are 2, 3, and 4 channel ESD protection options, respectively, for ESD protection diode arrays with a different number of channels. The TPD2E2U06 provides a higher level of IEC ESD protection, when compared to the TPDxE001 family, and removes the need for an input capacitor. The TPD4E1U06 removes the need for an input capacitor, provides higher IEC ESD protection, and provides lower capacitance, when compared to the TPDxE001 family.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD6E001	UQFN (10)	1.50 mm × 2.00 mm
	WQFN (12)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Schematic

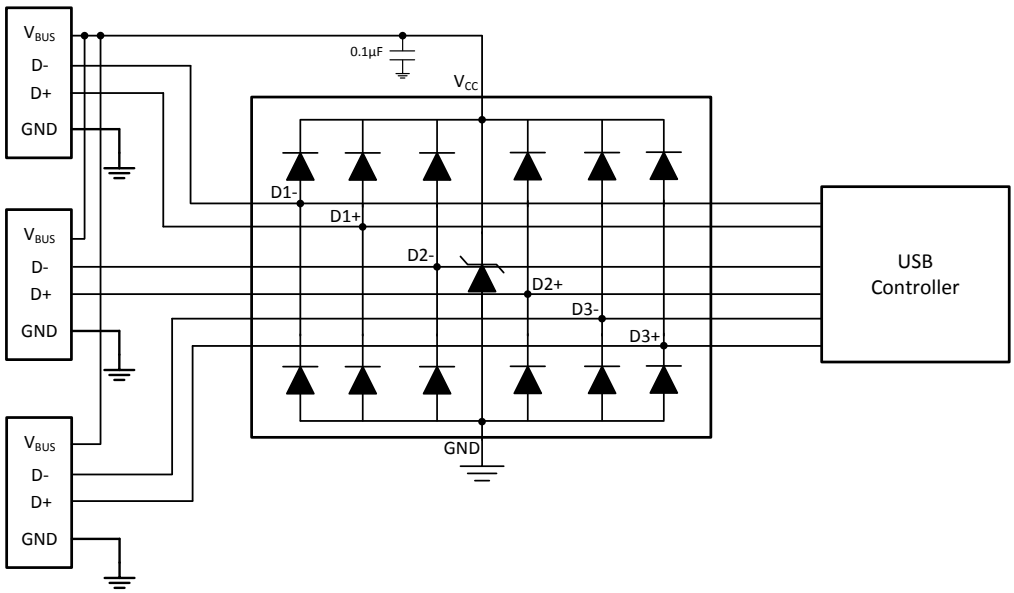


Table of Contents

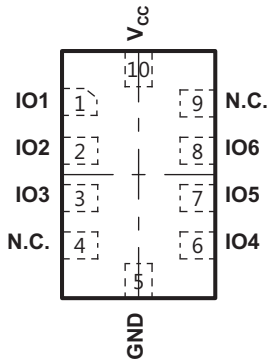
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2007) to Revision D	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

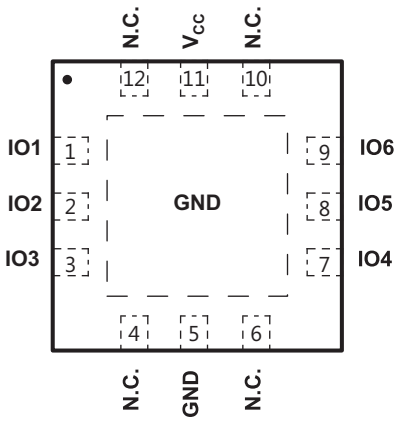
5 Pin Configuration and Functions

RSE Package
10-Pin UQFN
Top View



N.C.- Not internally connected

RSF Package
12-Pin WQFN
Top View



N.C.- Not internally connected

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	RSE	RSF		
GND	5	5	GND	Ground
IOx	1, 2, 3, 6, 7, 8	1, 2, 3, 7, 8, 9	I/O	ESD-protected channel
N.C.	4, 9	4, 6, 10, 12	—	Not internally connected
V_{CC}	10	11	Power	Power-supply input. Bypass V_{CC} to GND with a 0.1-µF ceramic capacitor.
EP	–	EP	GND	Exposed pad. Connect to GND.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}			–0.3	7	V
$V_{I/O}$			–0.3	V_{CC} + 0.3	V
T_J	Junction temperature			150	°C
	Bump temperature (soldering)	Infrared (15 s)		220	°C
		Vapor phase (60 s)		215	°C
	Lead temperature (soldering, 10 s)			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±15000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V
	IEC 61000-4-2 Contact Discharge	±8000	V
	IEC 61000-4-2 Air-Gap Discharge	±15000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A Operating free-air temperature range		-40		85	°C
Operating Voltage	V_{CC} Pin	0.9		5.5	V
	IOx Pins	0		V_{CC}	

6.4 Thermal Information

THERMAL METRIC(1)		TPD6E001		UNIT
		RSE (UQFN)	RSF (WQFN)	
		10 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	235.0	75.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	140.9	74.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	154.6	51.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.8	5.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	154.6	51.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	31.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{CC} = 5 V ± 10%, T_A = -40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{CC}	Supply voltage			0.9		5.5	V
I_{CC}	Supply current				1	100	nA
V_F	Diode forward voltage	I_F = 10 mA		0.65		0.95	V
V_{BR}	Breakdown voltage	I_{BR} = 10 mA		11			V
V_C	Channel clamp voltage(2)	T_A = 25°C, ±15-kV HBM, I_F = 10 A	Positive transients			V_{CC} + 25	V
			Negative transients			–25	V
		T_A = 25°C, ±8-kV Contact Discharge (IEC 61000-4-2), I_F = 24 A	Positive transients			V_{CC} + 60	V
			Negative transients			–60	V
		T_A = 25°C, ±15-kV Air-Gap Discharge (IEC 61000-4-2), I_F = 45 A	Positive transients			V_{CC} + 100	V
			Negative transients			–100	V
$I_{i/o}$	Channel leakage current	$V_{i/o}$ = GND to V_{CC}				±1	nA
$C_{i/o}$	Channel input capacitance	V_{CC} = 5 V, Bias of V_{CC}/2			1.5		pF

(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Channel clamp voltage is not production tested.

6.6 Typical Characteristics

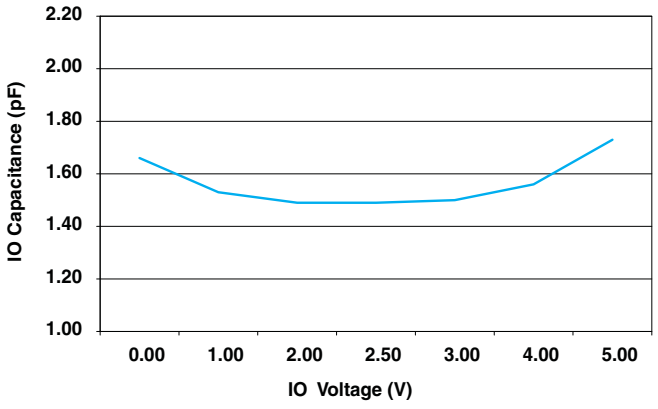


Figure 1. IO Capacitance vs IO Voltage (V_{CC} = 5 V)

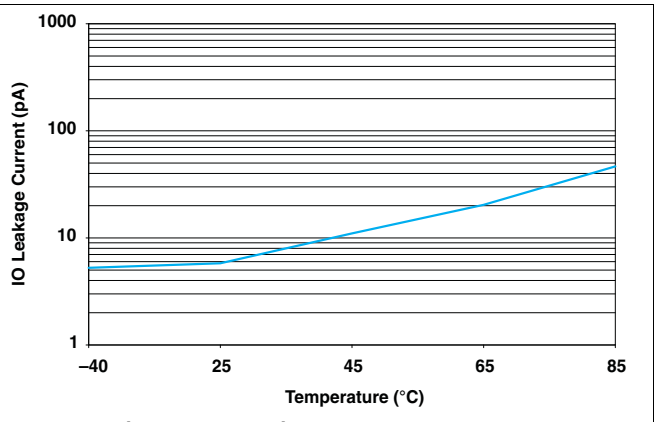


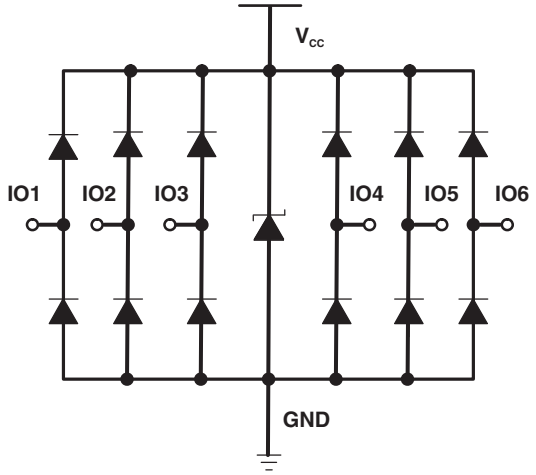
Figure 2. IO Leakage Current vs Temperature (V_{CC} = 5.5 V)

7 Detailed Description

7.1 Overview

The TPD6E001 is a six-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array. The TPD6E001 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device has a 1.5-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces. The ultra low leakage current (< 1 nA maximum) is suitable for precision analog measurements in applications like glucose meters and heart rate monitors.

7.2 Functional Block Diagram



7.3 Feature Description

TPD6E001 is a uni-directional ESD protection device with low capacitance. The device is constructed with a central ESD clamp that features two hiding diodes per line to reduce the capacitive loading. This central ESD clamp is also connected to V_{CC} to provide protection for the V_{CC} line. Each IO line is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 level 4 international standard. The TPD6E001's low loading capacitance makes it ideal for protection high-speed signal terminals.

7.4 Device Functional Modes

TPD6E001 is a passive-integrated circuit that activates whenever voltages above V_{BR} or below the lower diodes $V_{forward}$ (–0.6V) are present upon the circuit being protected. During ESD events, voltages as high as ±15 kV can be directed to ground and V_{CC} via the internal diode network. Once the voltages on the protected lines fall below the trigger voltage of the TPD6E001 (usually within 10's of nano-seconds) the device reverts back to a high-impedance state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPD6E001 is a diode array type Transient Voltage Suppressor (TVS) which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

8.2 Typical Application

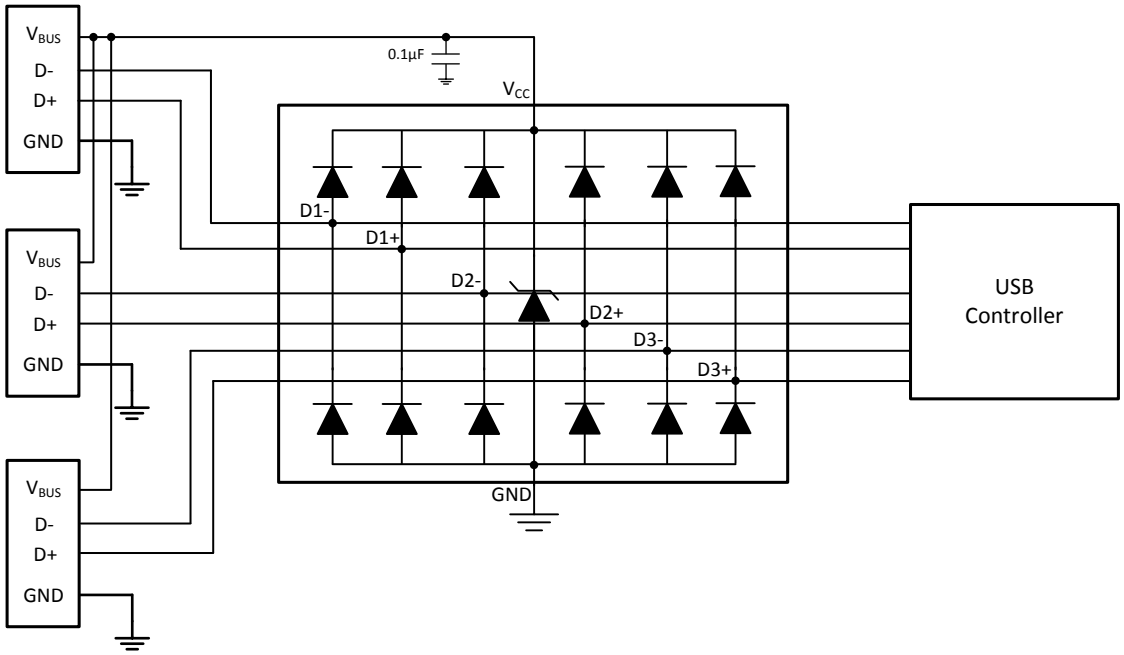


Figure 3. Typical Application Schematic

8.2.1 Design Requirements

For this design example, a single TPD6E001 is used to protect all the pins of three USB2.0 connectors.

Given the USB application, the following parameters are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, IO2, IO3, IO4, IO5, IO6	0 V to 3.6 V
Signal voltage range on V_{CC}	0 V to 5.25 V
Operating Frequency	240 MHz

8.2.2 Detailed Design Procedure

When placed near the USB connectors, the TPD6E001 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD6E001 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, the following layout/ design guidelines should be followed:

1. Place the TPD6E001 solution close to the connectors. This allows the TPD6E001 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1-µF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD6E001 consumes 1 nA (max) leakage current. But during the ESD event, V_{CC} and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating. In this example of protecting three USB ports, none of the IO pins will be left unused.
5. The V_{CC} pin can be connected in two different ways:
   (a) If the V_{CC} pin is connected to the system power supply, the TPD6E001 works as a transient suppressor for any signal swing above V_{CC} + V_F. A 0.1-µF capacitor on the device V_{CC} pin is recommended for ESD bypass.
   (b) If the V_{CC} pin is not connected to the system power supply, the TPD6E001 can tolerate higher signal swing in the range up to 10 V. Please note that a 0.1-µF capacitor is still recommended at the V_{CC} pin for ESD bypass.

8.2.3 Application Curve

Figure 4 is a capture of the voltage clamping waveform of TPD6E001 on IO1 during a +8kV Contact IEC61000-4-2 ESD strike.

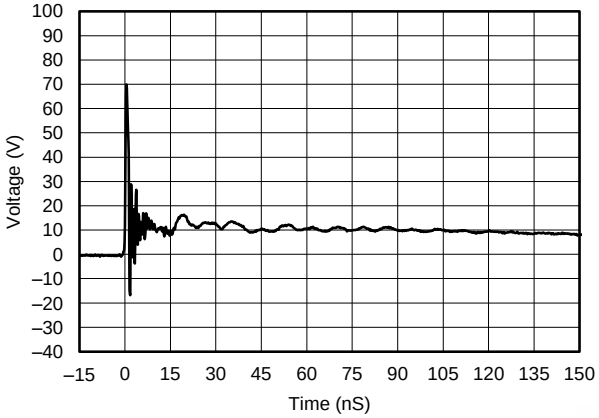


Figure 4. TPD6E001 +8kV Contact IEC61000-4-2 Voltage Clamping Waveform

9 Power Supply Recommendations

TPD6E001 is a passive TVS diode, so there is no requirement to power this device. However, for best IEC 61000-4-2 ESD performance and lowest capacitance performance, it is recommended that the V_{CC} pin is biased with a 5V supply and that a 0.1µF capacitor is placed near the V_{CC} pin. Take care to make sure that the maximum voltage specification for the V_{CC} pin is not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

Figure 5 is an example of how to layout three differential data pairs with the TPD6E001. One example could be protecting three USB2.0 ports from IEC ESD, as discussed in the Application and Implementation section.

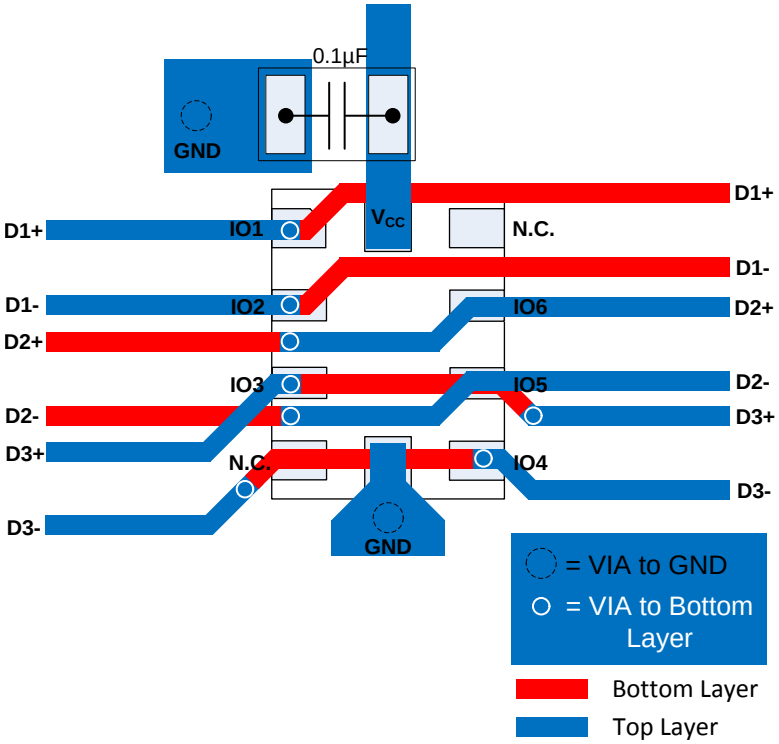


Figure 5. Routing with the RSE Package

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD6E001RSER	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2DO
TPD6E001RSFR	Active	Production	WQFN (RSF) | 12	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

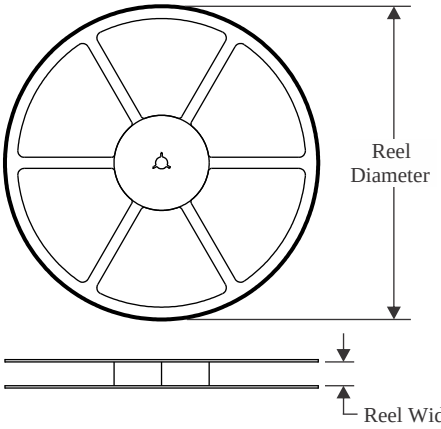
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

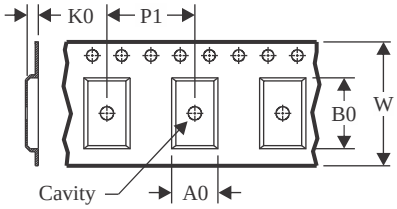
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

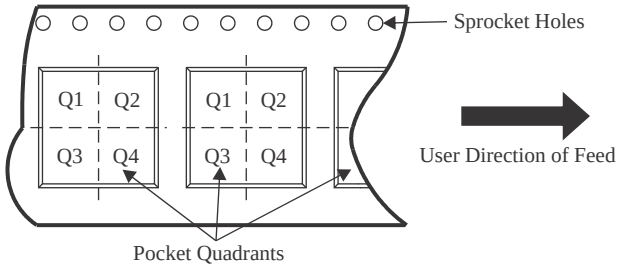


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

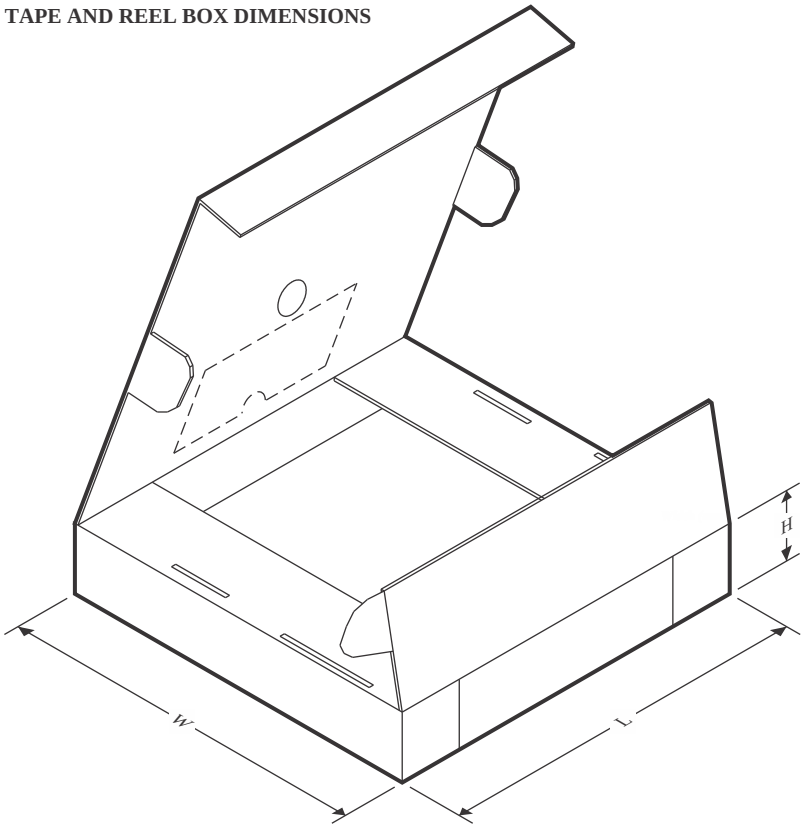
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD6E001RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1
TPD6E001RSFR	WQFN	RSF	12	2000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

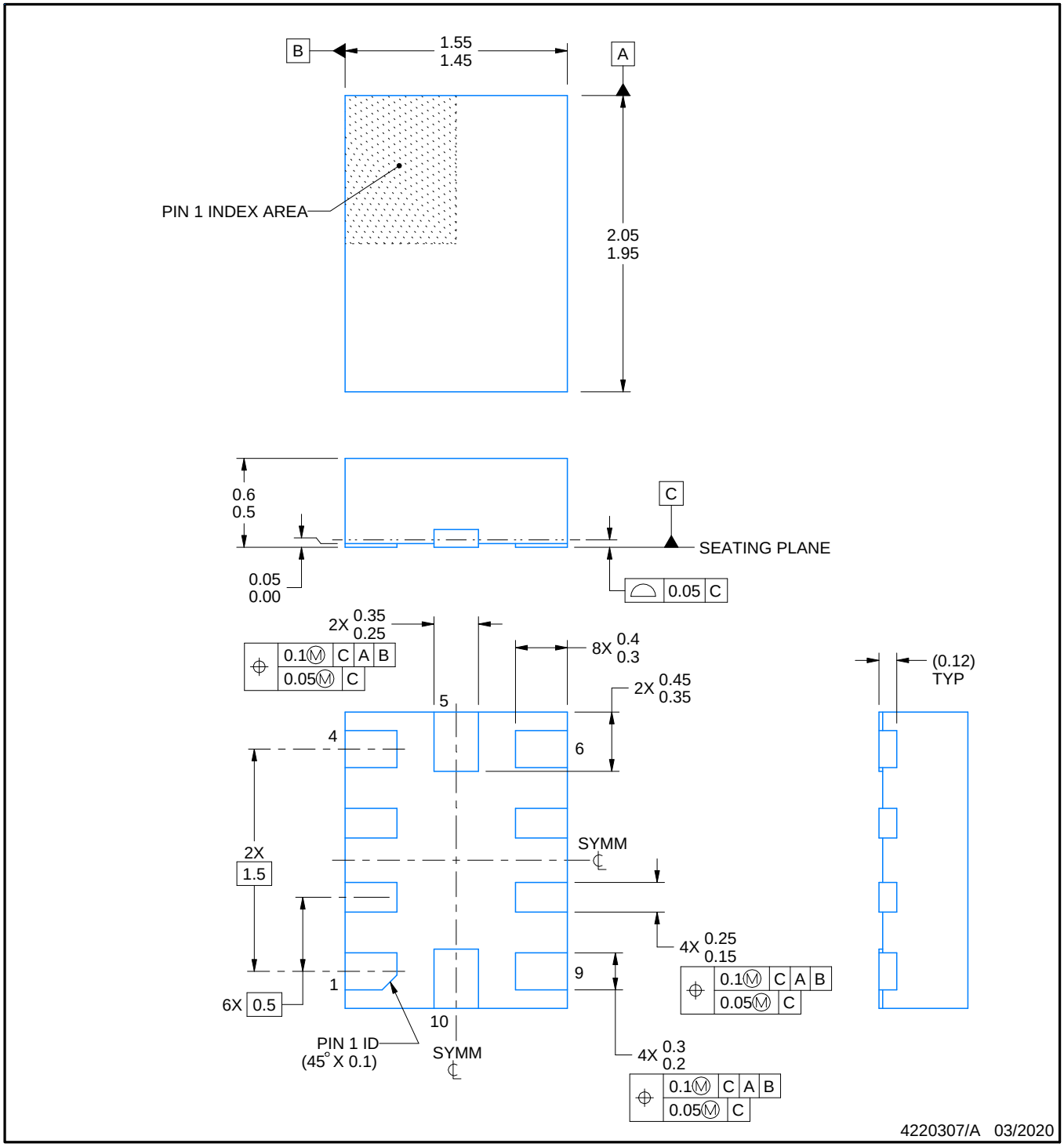
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD6E001RSER	UQFN	RSE	10	3000	189.0	185.0	36.0
TPD6E001RSFR	WQFN	RSF	12	2000	346.0	346.0	35.0

RSE0010A

PACKAGE OUTLINE

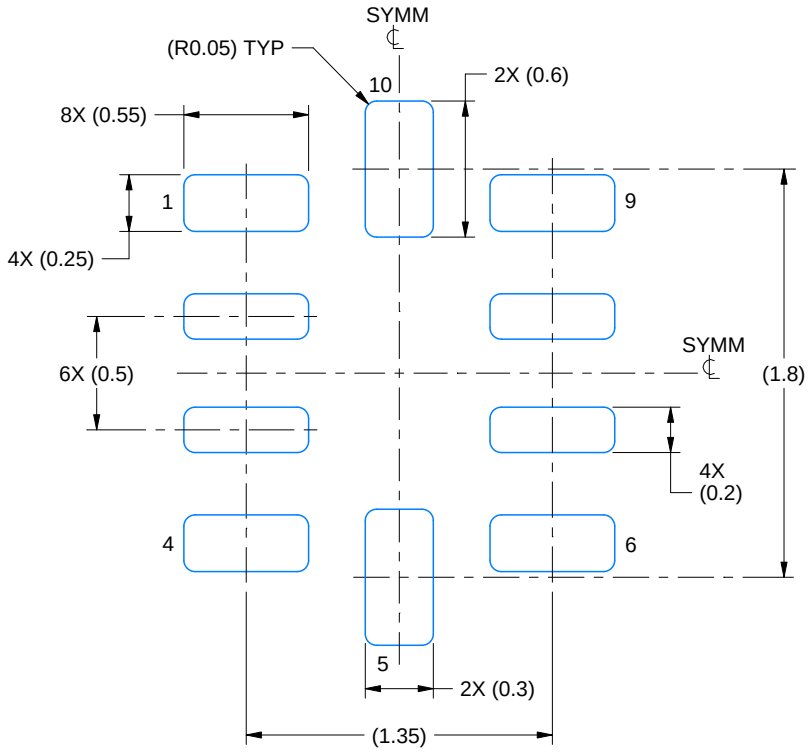
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

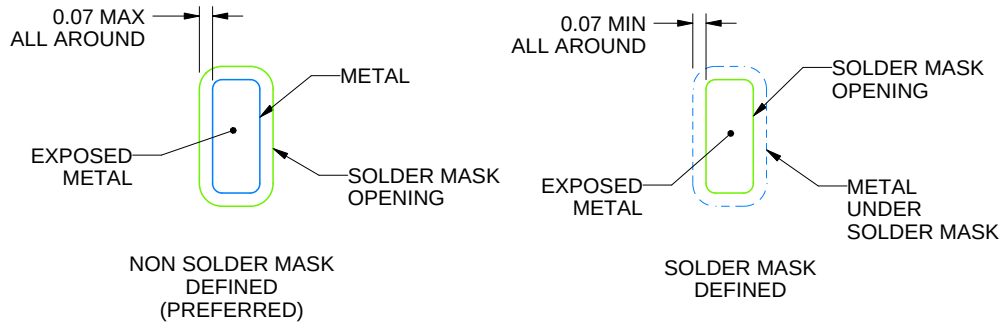


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

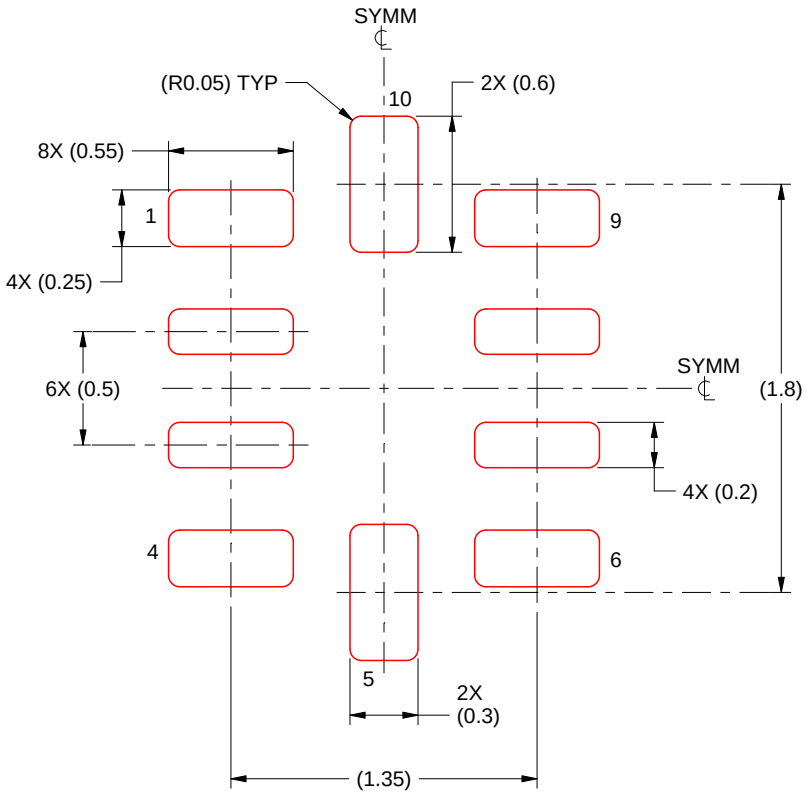


SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



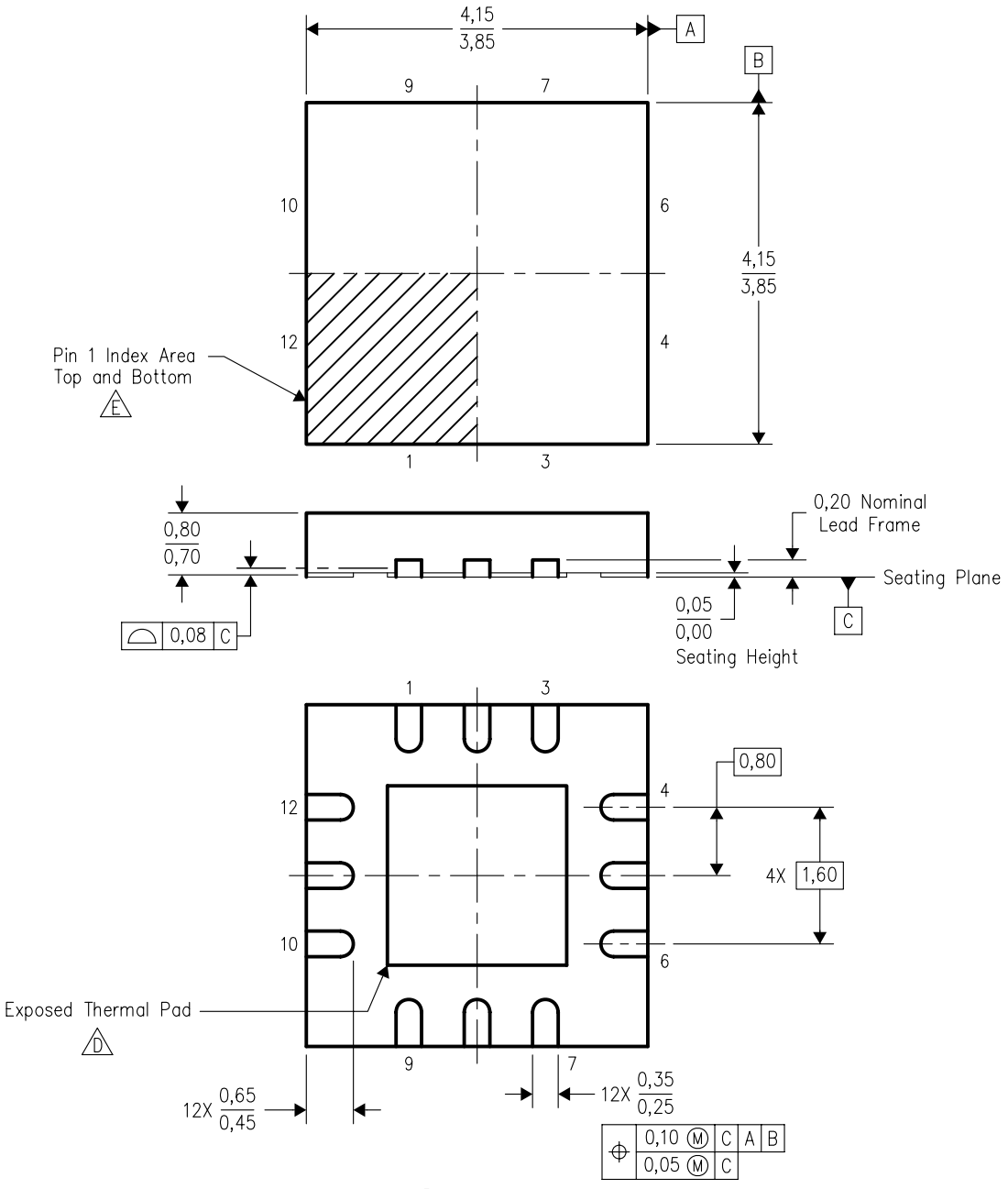
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RSF (S–PQFP–N12) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Complies to JEDEC MO–220 variation WGGB.

THERMAL PAD MECHANICAL DATA

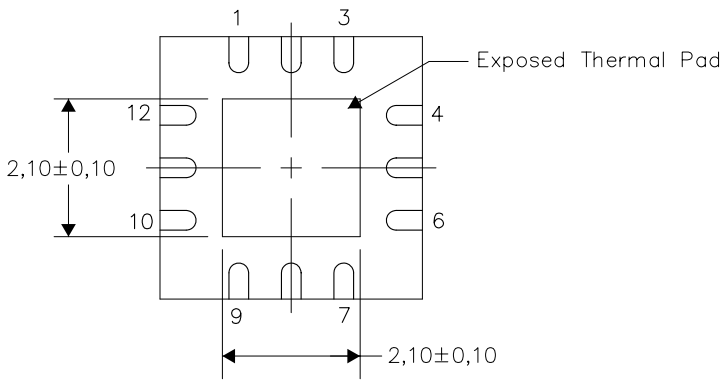
RSF (S–PWQFN–N12)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

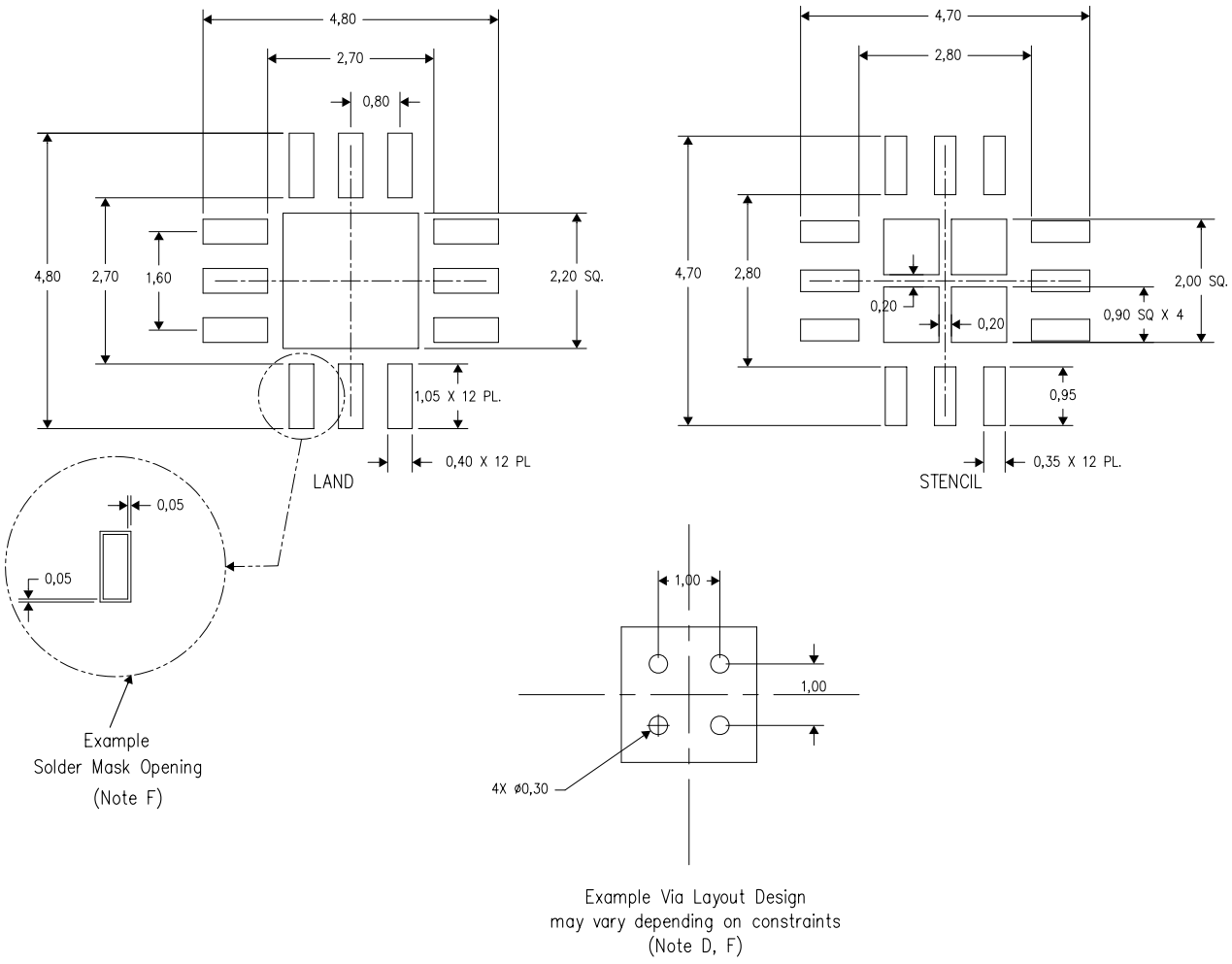


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RSF (R–PWQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



4208245–2/B 06/10

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265