TPS6217x-Q1 具有 DCS-Control™ 功能的 3V 到 17V 0.5A 降压转换器

1 特性

- DCS-Control™拓扑
- 适用于汽车电子 应用
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度等级：-40°C 至 125°C 的运行结温范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- 输入电压范围：3V 至 17V
- 输出电流高达 500mA
- 可调输出电压范围为 0.9V 至 6V
- 固定输出电压版本
- 无缝省电模式转换
- 静态电流典型值为 17μA
- 电源正常输出
- 100% 占空比模式
- 短路保护
- 过热保护
- 与 TPS62160-Q1 引脚对引脚兼容
- 采用 2 × 2mm WSON-8 封装
- 借助 WEBENCH® 电源设计器并使用 TPS62170-Q1 创建定制设计方案

2 应用

- 汽车类 12V 导轨式电源
- 同轴电缆供电 POL 电源
- 摄像机模块、视频模块
- 低压降稳压器 (LDO)

3 说明

TPS6217x-Q1 系列是一款简单易用的同步降压直流/直流转换器，针对 高功率密度的应用 进行了优化。该器件的开关频率典型值高达 2.25MHz，允许使用小型电感，利用 DCS-Control™ 拓扑技术提供快速瞬态响应并实现高输出电压精度。

此器件具有 3V 至 17V 宽运行输入电压范围，非常适用于由锂离子或其它电池以及 12V 中间电源轨供电的系统。其输出电压为 0.9V 至 6V，支持高达 0.5A 的持续输出电流（使用 100% 占空比模式）。

通过配置使能引脚和开漏电源正常状态引脚也可以实现电源排序。

在节能模式下，器件可根据输入电压 (VIN) 生成约 17μA 的静态电流。负载较小时可自动且无缝进入节能模式，同时该模式可保持整个负载范围内的高效率。在关断模式下，此器件会关闭且关断期间的流耗少于 2μA。

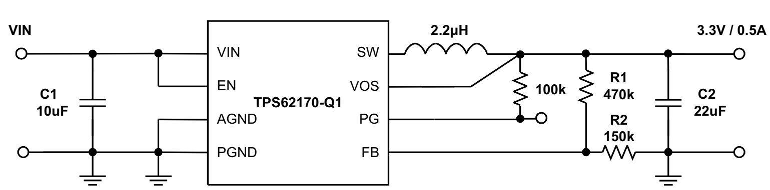
此器件分为可调和固定输出电压型号，采用 2mm × 2mm (DSG) 8 引脚 WSON 封装。

器件信息(1)

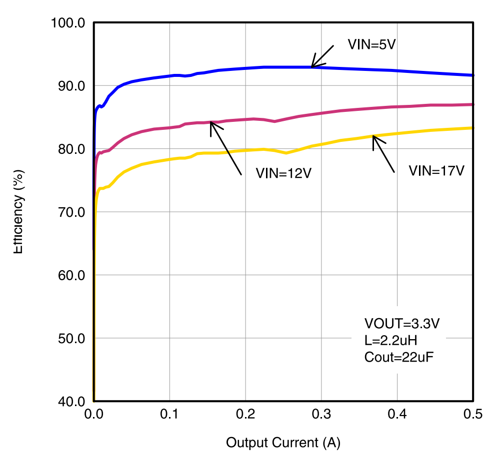
器件型号	封装	封装尺寸（标称值）
TPS62170-Q1	WSON (8)	2.00mm x 2.00mm
TPS62171-Q1	WSON (8)	2.00mm x 2.00mm
TPS62172-Q1	WSON (8)	2.00mm x 2.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



效率与输出电流间的关系



目录

1 特性 1
2 应用 1
3 说明 1
4 修订历史记录 2
5 **Device Comparison Table** 3
6 **Pin Configuration and Functions** 3
7 **Specifications** 4
- 7.1 Absolute Maximum Ratings 4
- 7.2 ESD Ratings 4
- 7.3 Recommended Operating Conditions 4
- 7.4 Thermal Information 4
- 7.5 Electrical Characteristics 5
- 7.6 Typical Characteristics 6

8 **Detailed Description** 7
- 8.1 Overview 7
- 8.2 Functional Block Diagram 7
- 8.3 Feature Description 8
- 8.4 Device Functional Modes 8

9 **Application and Implementation** 11
- 9.1 Application Information 11
- 9.2 Typical TPS62170-Q1 Application 11
- 9.3 System Examples 20

10 **Power Supply Recommendations** 22
11 **Layout** 23
- 11.1 Layout Guidelines 23
- 11.2 Layout Example 23
- 11.3 Thermal Considerations 24

12 器件和文档支持 25
- 12.1 器件支持 25
- 12.2 文档支持 25
- 12.3 相关链接 26
- 12.4 商标 26
- 12.5 静电放电警告 26
- 12.6 接收文档更新通知 26
- 12.7 社区资源 26
- 12.8 Glossary 26

13 机械、封装和可订购信息 26

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (November 2016) to Revision D	Page
• 已添加 WEBENCH® 信息	1
• Changed T_J spec MAX value From 125°C To 150°C in the *Absolute Maximum Ratings* table	4

Changes from Revision B (October 2016) to Revision C	Page
• 已添加 *引脚对引脚兼容*特性	1
• Changed *Thermal Information* table	4
• Added C1, C2, R1, R2, descriptors to *Figure 5*	11
• Added C1, C2 to *Table 1*	11

Changes from Revision A (September 2016) to Revision B	Page
• Added the *Device Comparison Table*	3

Changes from Original (December 2014) to Revision A	Page
• 在应用列表中将"同轴以太网供电 POL 电源"更改为"同轴电缆供电 POL 电源"	1
• 已添加 数据表中增加了 TPS62171-Q1 器件。	1
• Changed Unit from mA to V for Pin voltage at FB, PG, and VOS in the *Absolute Maximum Ratings* table.	4
• Changed Unit from °C to mA in the *Absolute Maximum Ratings* table for Power Good sink current.	4
• Changed Unit from kV to °C in the *Absolute Maximum Ratings* table for the Operating junction temperature, T_J	4
• Added legal NOTE at *Application and Implementation*	11
• Added cross references to Third-Party Products disclaimer in Table 1	11

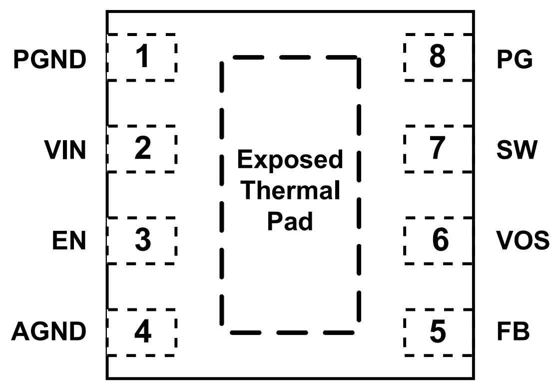
5 Device Comparison Table

PART NUMBER(1)	OUTPUT VOLTAGE
TPS62170-Q1	adjustable
TPS62171-Q1	1.8 V
TPS62172-Q1	3.3 V

(1) For detailed ordering information please check the 机械、封装和可订购信息 section at the end of this datasheet.

6 Pin Configuration and Functions

8-Pin WSON
DSG Package
(Top View)



Pin Functions

PIN(1)		I/O	DESCRIPTION
NAME	NUMBER		
PGND	1		Power ground
VIN	2	I	Supply voltage
EN	3	I	Enable input (High = enabled, Low = disabled)
AGND	4		Analog ground
FB	5	I	Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.
VOS	6	I	Output voltage sense pin and connection for the control loop circuitry.
SW	7	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
PG	8	O	Output power good (High = VOUT ready, Low = VOUT below nominal regulation) ; open drain (requires pull-up resistor; goes high impedance, when device is switched off)
Exposed Thermal Pad			Must be connected to AGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see *Detailed Description* and *Application and Implementation* sections.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Pin voltage[2]	VIN	–0.3	20	V
	EN	–0.3	V_{IN}+0.3	
	SW	-0.3	V_{IN}+0.3	V
	FB, PG, VOS	–0.3	7	V
Power Good sink current	PG		10	mA
Operating junction temperature range, T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	3		17	V
V_{OUT}	Output voltage range	0.9		6	V
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS6217x-Q1	UNIT
		DSG (8 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, .

7.5 Electrical Characteristics

over junction temperature range (T_J = –40°C to +125°C), typical values at V_{IN} = 12 V and T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range[(1)]		3		17	V
I_Q	Operating quiescent current	EN = High, IOUT = 0 mA, Device not switching		17	30	µA
I_{SD}	Shutdown current[(2)]	EN = Low		1.8	25	µA
V_{UVLO}	Undervoltage lockout threshold	Falling input voltage	2.6	2.7	2.82	V
		Hysteresis		180		mV
T_{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			20		
CONTROL (EN, PG)						
V_{EN_H}	High-level input threshold voltage (EN)		0.9			V
V_{EN_L}	Low-level input threshold voltage (EN)				0.3	V
I_{LKG_EN}	Input leakage current (EN)	EN = V_{IN} or GND		0.01	1	µA
V_{TH_PG}	Power Good threshold voltage	Rising (%V_{OUT})	92%	95%	98%	
		Falling (%V_{OUT})	87%	90%	93%	
V_{OL_PG}	Power Good output low	I_{PG} = –2 mA		0.07	0.3	V
I_{LKG_PG}	Input leakage current (PG)	V_{PG} = 1.8 V		1	400	nA
POWER SWITCH						
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{IN} ≥ 6 V		300	600	mΩ
		V_{IN} = 3 V		430		
	Low-side MOSFET ON-resistance	V_{IN} ≥ 6 V		120	200	mΩ
		V_{IN} = 3 V		165		
I_{LIMF}	High-side MOSFET forward current limit[(3)]	V_{IN} = 12 V, T_A = 25°C	0.85	1.05	1.35	A
OUTPUT						
VREF	Internal reference voltage			0.8		V
I_{LKG_FB}	Pin leakage current (FB)	TPS62170-Q1, V_{FB} = 1.2 V		5	400	nA
V_{OUT}	Output voltage range	TPS62170-Q1, V_{IN} ≥ V_{OUT}	0.9		6.0	V
	Feedback voltage accuracy[(4)]	PWM Mode operation, V_{IN} ≥ V_{OUT} + 1 V	–3%		3%	
		Power Save Mode operation, C_{OUT} = 22 µF[(5)]	–3.5%		4%	
	DC output voltage load regulation[(6)]	V_{IN} = 12 V, V_{OUT} = 3.3 V, PWM Mode operation		0.05		% / A
	DC output voltage line regulation[(6)]	3 V ≤ V_{IN} ≤ 17 V, V_{OUT} = 3.3 V, I_{OUT} = 0.5 A, PWM Mode operation		0.02		% / V

(1) The device is still functional down to Under Voltage Lockout (see parameter V_{UVLO}).
(2) Current into VIN pin.
(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see *Current Limit and Short Circuit Protection*).
(4) For fixed voltage versions, the (internal) resistive feedback divider is included.
(5) The accuracy in Power Save Mode can be improved by increasing the C_{OUT} value, reducing the output voltage ripple.
(6) Line and load regulation are depending on external component selection and layout (see Figure 14 and Figure 15).

7.6 Typical Characteristics

At V_{IN} = 12 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)

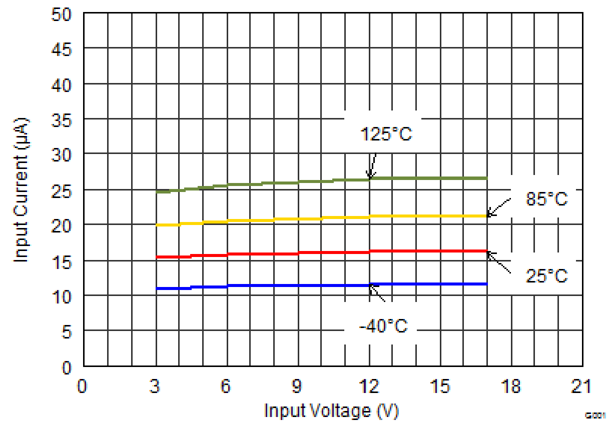


Figure 1. Quiescent Current

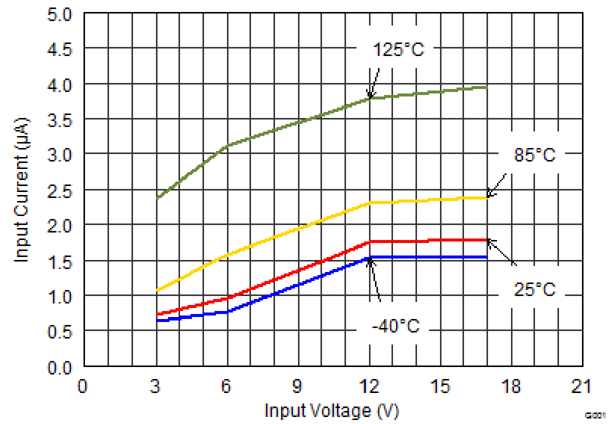


Figure 2. Shutdown Current

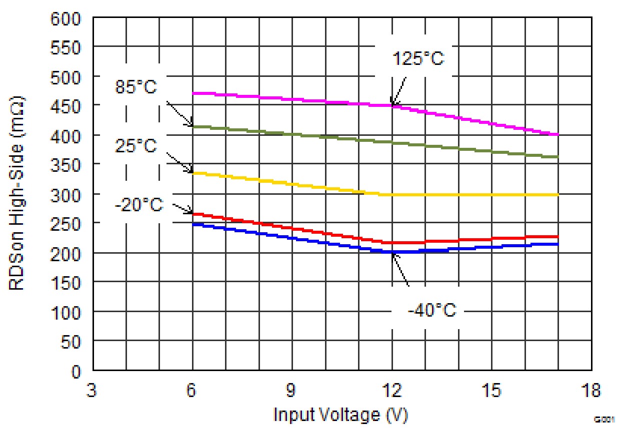


Figure 3. High-Side Static Drain-Source-Resistance (R_{DSon})

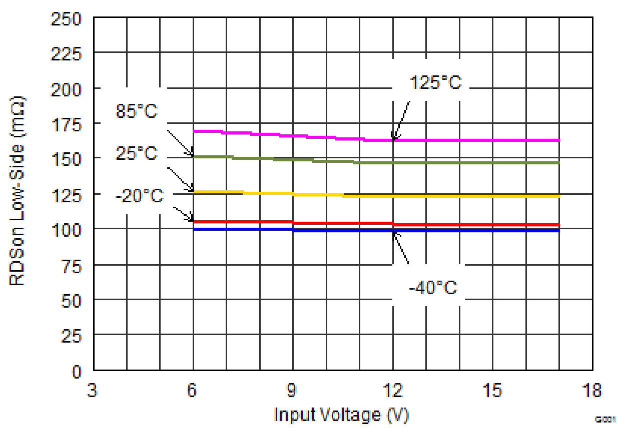


Figure 4. Low-Side Static Drain-Source-Resistance (R_{DSon})

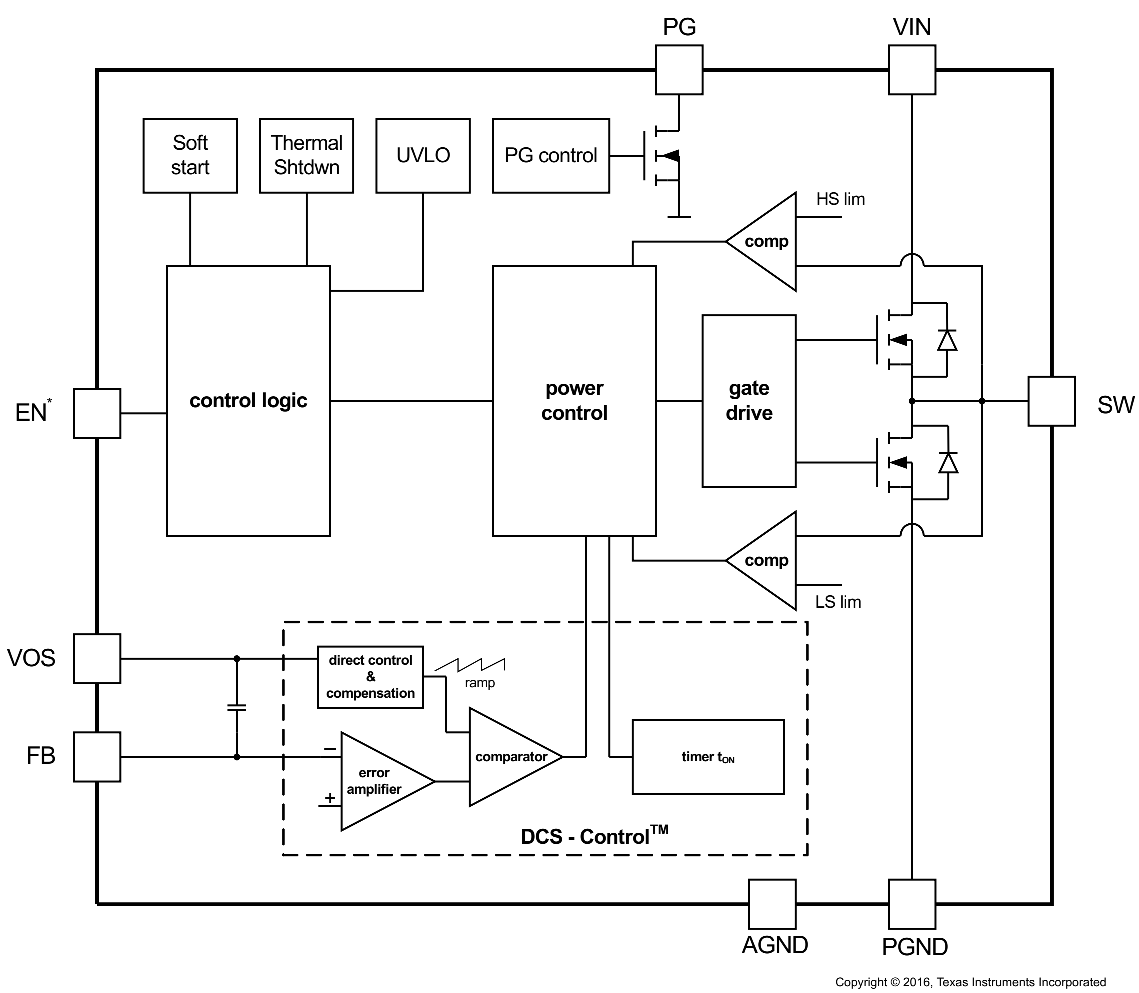
8 Detailed Description

8.1 Overview

The TPS6217x-Q1 synchronous switched mode power converters are based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless transition into power save mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.25 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage.

8.2 Functional Block Diagram



* This pin is connected to a pull down resistor internally (see *Feature Description* section).

8.3 Feature Description

8.3.1 Enable / Shutdown (EN)

When Enable (EN) is set High, the device starts operation.

Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.8 µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. If the EN pin goes Low, an internal pull-down resistor of about 400 kΩ is connected and keeps it Low in case of floating pin. To avoid ON/OFF oscillations, a minimum slew rate of about 50 mV/s is recommended for the EN signal.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

8.3.2 Softstart

The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50 µs and V_{OUT} rises with a slope of about 25 mV/µs. See Figure 26 and Figure 27 for typical startup operation.

The TPS6217x-Q1 can start into a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage.

8.3.3 Power Good (PG)

The TPS6217x-Q1 has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic low level. It is high impedance when the device is turned off due to EN, UVLO, or thermal shutdown.

8.3.4 Under Voltage Lockout (UVLO)

If the input voltage drops, the under voltage lockout prevents misoperation of the device by switching off both the power FETs. The under voltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 180 mV.

8.3.5 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typ), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with Soft Start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shut down temperature.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

The TPS62170-Q1 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of about 2.25 MHz. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

Device Functional Modes (continued)

8.4.2 Power Save Mode Operation

The TPS6217x-Q1's built in Power Save Mode will be entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

The TPS6217x-Q1 includes a fixed on-time circuitry. This on-time, in steady-state operation, can be estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 420ns \quad (1)$$

For very small output voltages, the on-time increases beyond the result of Equation 1, to stay above an absolute minimum on-time, $t_{ON(min)}$, which is around 80 ns to limit switching losses. The peak inductor current in PSM can be approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \quad (2)$$

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS62170-Q1 does not enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

8.4.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D = Vout/Vin and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input to output voltage differences, e.g. for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \quad (3)$$

where

I_{OUT} is the output current,
$R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET and
R_L is the DC resistance of the inductor used.

8.4.4 Current Limit and Short Circuit Protection

The TPS6217x-Q1 devices are protected against heavy load and short circuit events. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET will be turned off. Avoiding shoot through current, the low-side FET is then switched on to allow the inductor current to decrease. The high-side FET will turn on again, only if the current in the low-side FET has decreased below the low side current limit threshold.

Device Functional Modes (continued)

The output current of the device is limited by the current limit (see *Electrical Characteristics*). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD} \tag{4}$$

where

I_{LIMF} is the static current limit, specified in the electrical characteristic table,
L is the inductor value,
V_L is the voltage across the inductor and
t_{PD} is the internal propagation delay.

The dynamic high side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF\_HS} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns \tag{5}$$

Care on the current limit has to be taken if the input voltage is high and very small inductances are used.

8.4.5 Operation Above T_J = 125°C

The operating junction temperature of the device is specified up to 125°C. In power supply circuits, the self heating effect causes, that the junction temperature, T_J, is even higher than the ambient temperature T_A. Depending on T_A and the load current, the maximum operating temperature T_J can be exceeded. However, the electrical characteristics are specified up to a T_J of 125°C only. The device operates as long as thermal shutdown threshold is not triggered.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following information is intended to be a guideline through the individual power supply design process.

9.2 Typical TPS62170-Q1 Application

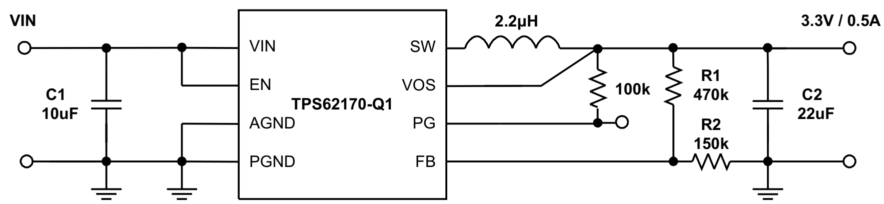


Figure 5. 3.3-V/0.5-A Power Supply

9.2.1 Design Requirements

The step-down converter design can be adapted to different output voltage and load current needs by choosing external components appropriate. The following design procedure is adequate for whole VIN, VOUT and load current range of TPS62170-Q1. Using Table 2, the design procedure needs minimum effort.

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
IC	17-V, 0.5-A step-down converter, WSON	TPS62170QDSG, Texas Instruments
L1	2.2-µH, 1.4-A, 3 x 2.8 x 1.2 mm	VLF3012ST-2R2M1R4, TDK
C1	10-µF, 25-V, ceramic	Standard
C2	22-µF, 6.3-V, ceramic	Standard
R1	Depending on Vout	
R2	Depending on Vout	
R3	100-kΩ, chip, 0603, 1/16-W, 1%	Standard

(1) See *Third-Party Products* disclaimer.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62170-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance

- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Programming the Output Voltage

While the output voltage of the TPS62170-Q1 is adjustable, the TPS62171-Q1 and TPS62172-Q1 are programmed to a fixed output voltage. For fixed output versions, the FB pin is pulled down internally and may be left floating. it is recommended to connect it to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from VOUT to FB to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6. It is recommended to choose resistor values which allow a cross current of at least 2 uA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

$$R_1 = R_2 \left(\frac{V_{OUT}}{0.8V} - 1 \right) \tag{6}$$

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin to about 7.4 V.

9.2.2.3 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS62170-Q1 is optimized to work within a range of external components. The LC output filters inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see *Output Filter and Loop Stability* section). Table 2 can be used to simplify the output filter component selection.

Table 2. Recommended LC Output Filter Combinations(1)

	4.7µF	10µF	22µF	47µF	100µF	200µF	400µF
1µH							
2.2µH		√	√(2)	√	√	√	
3.3µH		√	√	√	√		
4.7µH							

(1) The values in the table are nominal values. Variations of typically ±20% due to tolerance, saturation and DC bias are assumed.
(2) This LC combination is the standard value and recommended for most applications.

More detailed information on further LC combinations can be found in SLVA463.

9.2.2.3.1 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{7}$$

$$\Delta I_{L(\max)} = V_{OUT} \cdot \left(\frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right) \tag{8}$$

where

- I_L(max) is the maximum inductor current,
- ΔI_L is the Peak to Peak Inductor Ripple Current,
- L(min) is the minimum effective inductor value and
- f_{SW} is the actual PWM Switching Frequency.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS62170-Q1 and are recommended for use:

Table 3. List of Inductors

TYPE	INDUCTANCE [µH]	CURRENT [A](1)	DIMENSIONS [L x B x H] mm	MANUFACTURER(2)
VLF3012ST-2R2M1R4	2.2 µH, ±20%	1.9 A	3.0 x 2.8 x 1.2	TDK
VLF302512MT-2R2M	2.2 µH, ±20%	1.9 A	3.0 x 2.5 x 1.2	TDK
VLS252012-2R2	2.2 µH, ±20%	1.3 A	2.5 x 2.0 x 1.2	TDK
XFL3012-222MEC	2.2 µH, ±20%	1.9 A	3.0 x 3.0 x 1.2	Coilcraft
XFL3012-332MEC	3.3 µH, ±20%	1.6 A	3.0 x 3.0 x 1.2	Coilcraft
XPL2010-222MLC	2.2 µH, ±20%	1.3 A	1.9 x 2.0 x 1.0	Coilcraft
XPL2010-332MLC	3.3 µH, ±20%	1.1 A	1.9 x 2.0 x 1.0	Coilcraft
LPS3015-332ML	3.3 µH, ±20%	1.4 A	3.0 x 3.0 x 1.4	Coilcraft
PFL2512-222ME	2.2 µH, ±20%	1.0 A	2.8 x 2.3 x 1.2	Coilcraft
PFL2512-333ME	3.3 µH, ±20%	0.78 A	2.8 x 2.3 x 1.2	Coilcraft
744028003	3.3 µH, ±30%	1.0 A	2.8 x 2.8 x 1.1	Wuerth
PSI25201B-2R2MS	2.2 µH, ±20%	1.3 A	2.0 x 2.5 x 1.2	Cyntec
NR3015T-2R2M	2.2 µH, ±20%	1.5 A	3.0 x 3.0 x 1.5	Taiyo Yuden
BRC2012T2R2MD	2.2 µH, ±20%	1.0 A	2.0 x 1.25 x 1.4	Taiyo Yuden
BRC2012T3R3MD	3.3 µH, ±20%	0.87 A	2.0 x 1.25 x 1.4	Taiyo Yuden

(1) I_{RMS} at 40°C rise or I_{SAT} at 30% drop.
(2) See *Third-Party Products* disclaimer.

The TPS6217x-Q1 can be run with an inductor as low as 2.2 µH. However, for applications running with low input voltages, 3.3 µH is recommended, to allow the full output current. The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L \tag{9}$$

Using Equation 8, this current level can be adjusted by changing the inductor value.

9.2.2.3.2 Capacitor Selection

9.2.2.3.2.1 Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TPS6217x-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode (see SLVA463).

NOTE

In Power Save Mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

9.2.2.3.2.2 Input Capacitor

For most applications, 10 µF is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and GND as close as possible to those pins.

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

9.2.2.4 Output Filter and Loop Stability

The devices of the TPS6217x-Q1 family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 10:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{10}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 2 and are recommended for use. Different values may work, but care has to be taken on the loop stability which might be affected. More information including a detailed L-C stability matrix can be found in SLVA463.

The TPS6217x-Q1 devices, both fixed and adjustable versions, include an internal 25-pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per Equation 11 and Equation 12:

$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25pF} \tag{11}$$

$$f_{pole} = \frac{1}{2\pi \cdot 25pF} \cdot \left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{12}$$

Though the TPS6217x-Q1 devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and/or improved transient response. An external feed-forward capacitor can also be added. A more detailed discussion on the optimization for stability vs transient response can be found in SLVA289 and SLVA466.

If using ceramic capacitors, the DC bias effect has to be considered. The DC bias effect results in a drop in effective capacitance as the voltage across the capacitor increases (see *DC Bias effect* NOTE in the *Input Capacitor* section).

9.2.3 Application Performance Plots

At V_{IN} = 12 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)

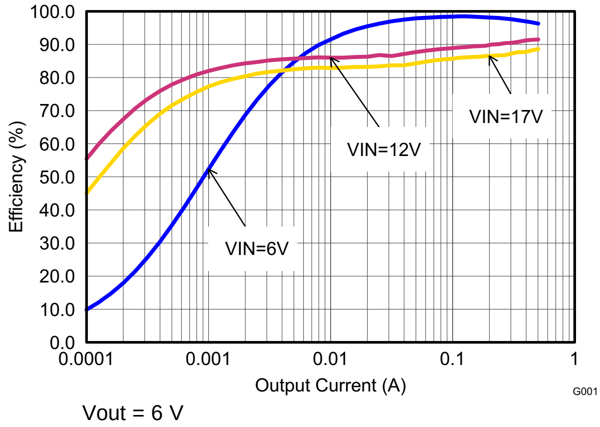


Figure 6. Efficiency vs Output Current

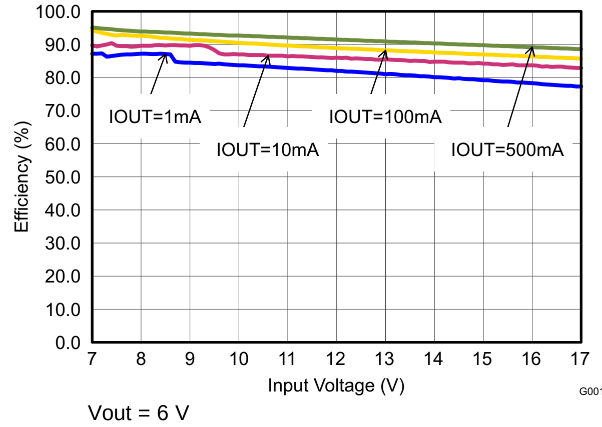


Figure 7. Efficiency vs Input Voltage

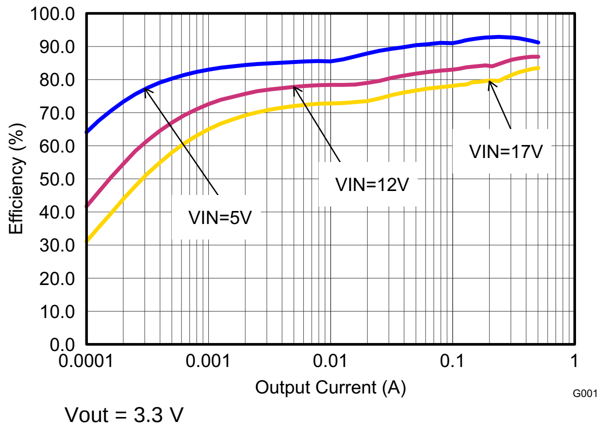


Figure 8. Efficiency vs Output Current

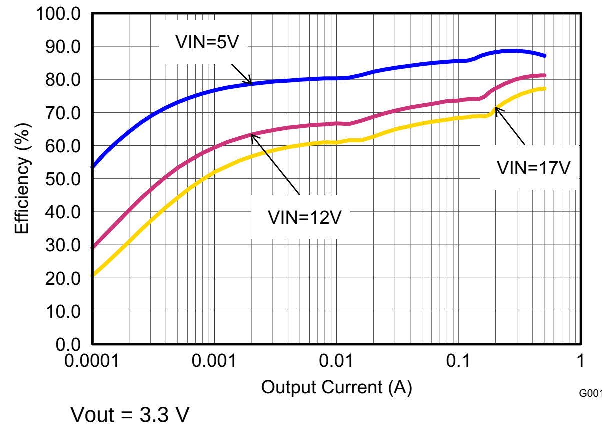


Figure 9. Efficiency vs Input Voltage

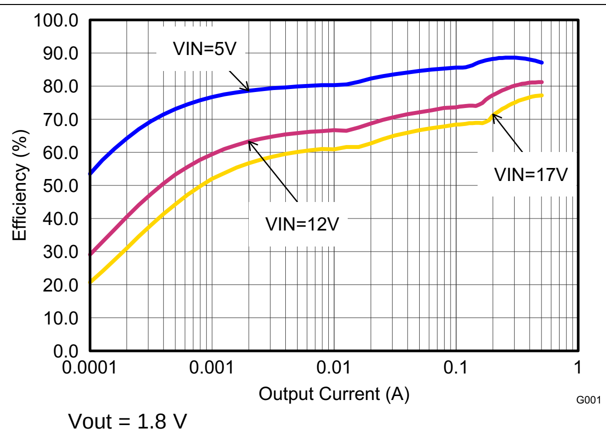


Figure 10. Efficiency vs Output Current

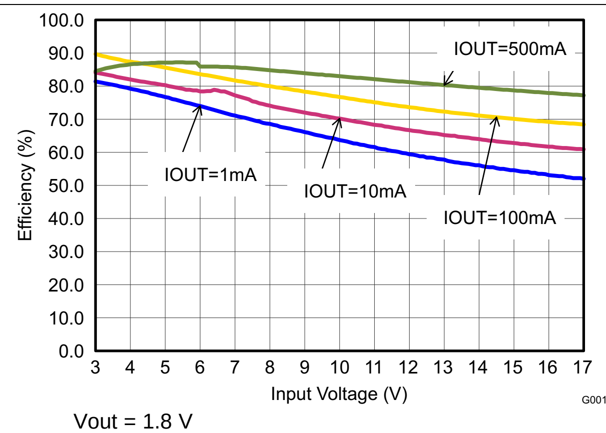


Figure 11. Efficiency vs Input Voltage

At V_{IN} = 12 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)

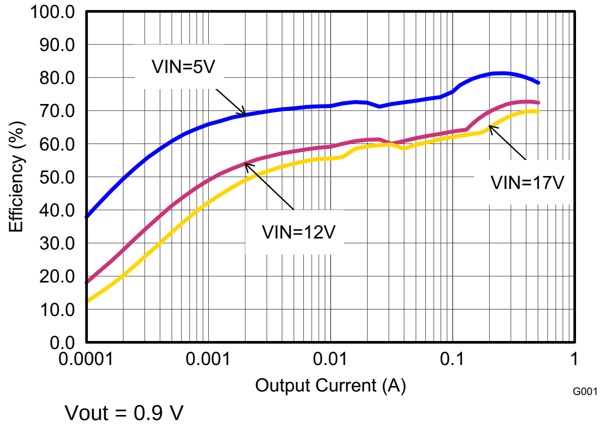


Figure 12. Efficiency vs Output Current

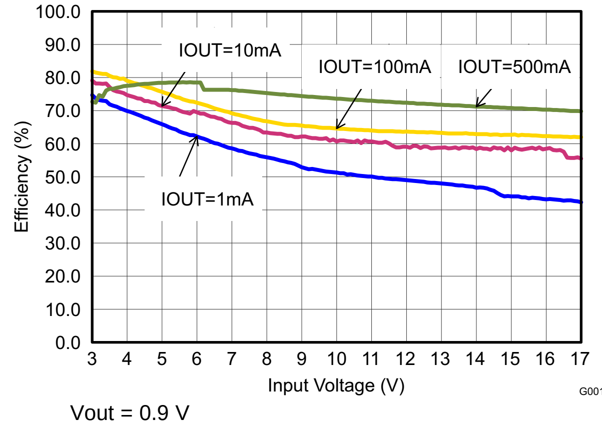


Figure 13. Efficiency vs Input Voltage

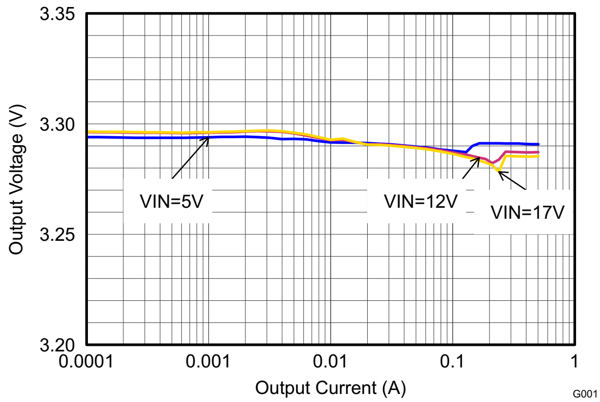


Figure 14. Output Voltage Accuracy (Load Regulation)

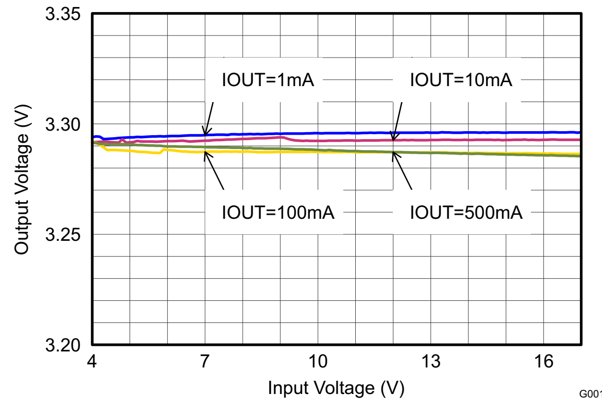


Figure 15. Output Voltage Accuracy (Line Regulation)

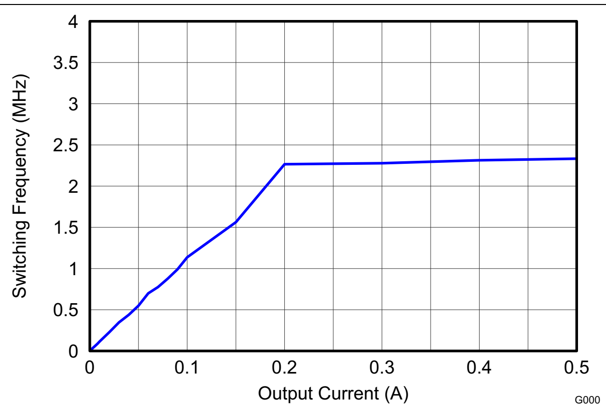


Figure 16. Switching Frequency vs Output Current

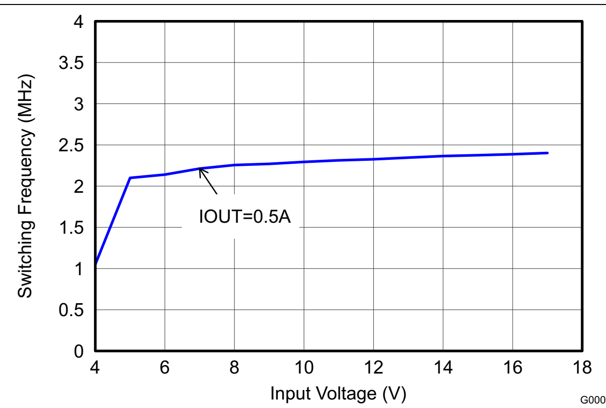


Figure 17. Switching Frequency vs Input Voltage

At V_{IN} = 12 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)

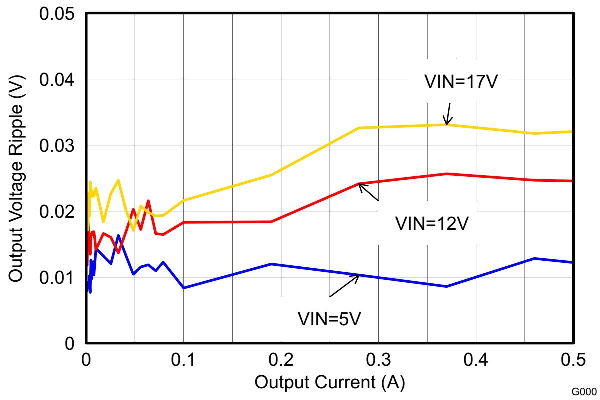


Figure 18. Output Voltage Ripple

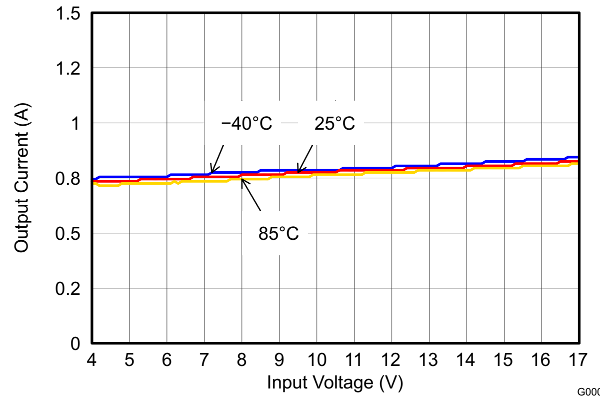


Figure 19. Maximum Output Current

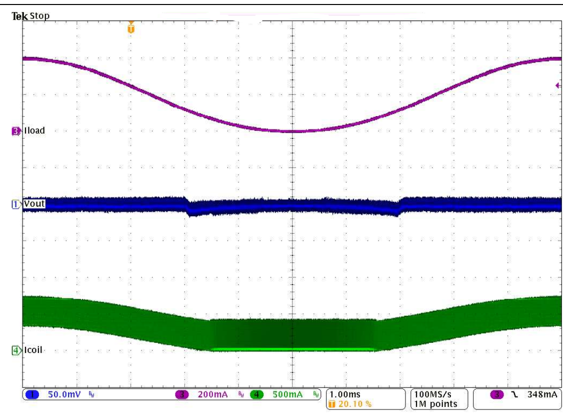


Figure 20. PWM / PSM Mode Transition

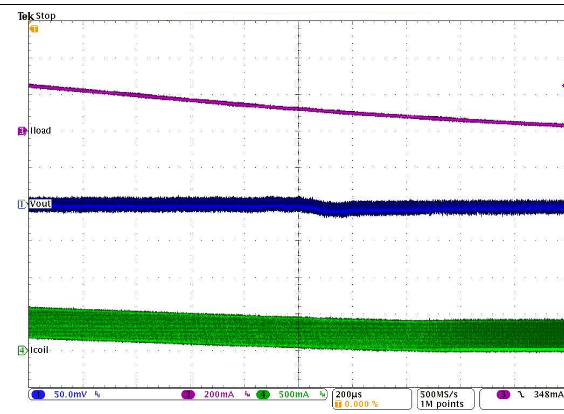
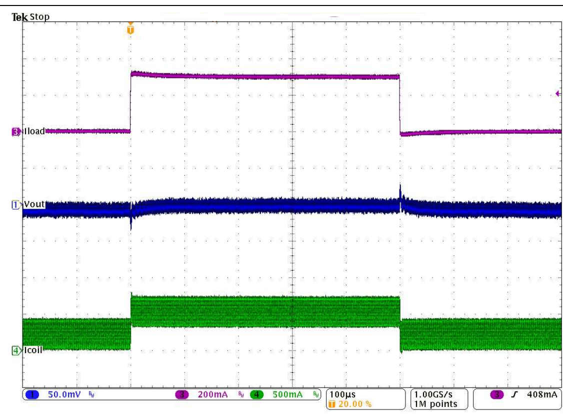
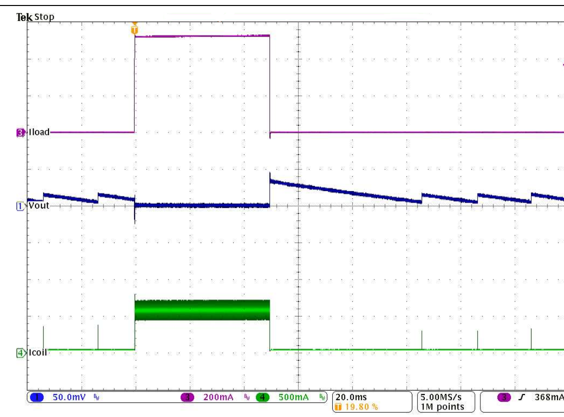


Figure 21. PWM to PSM Mode Transition



200 mA to 500 mA

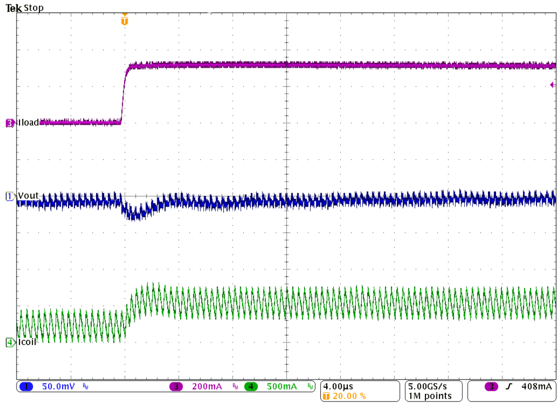
Figure 22. Load Transient Response in PWM Mode



100 mA to 500 mA

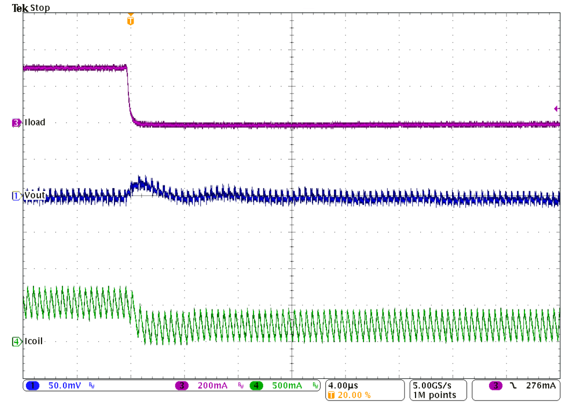
Figure 23. Load Transient Response from Power Save Mode

At V_{IN} = 12 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)



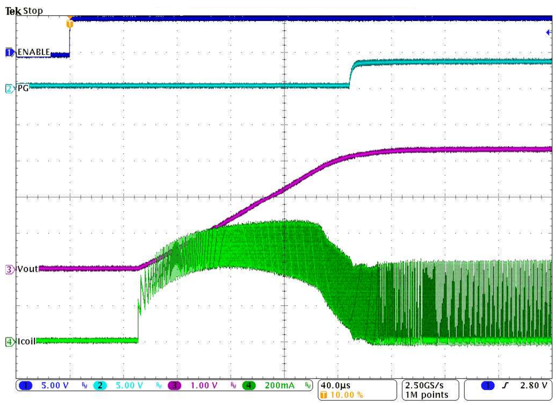
200 mA to 500 mA

Figure 24. Load Transient Response in PWM Mode, Rising Edge



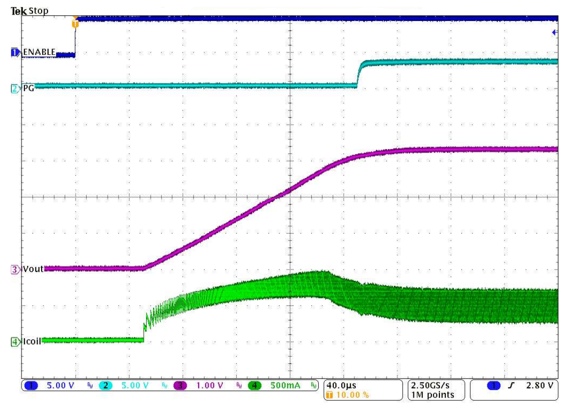
200 mA to 500 mA

Figure 25. Load Transient Response in PWM Mode, Falling Edge



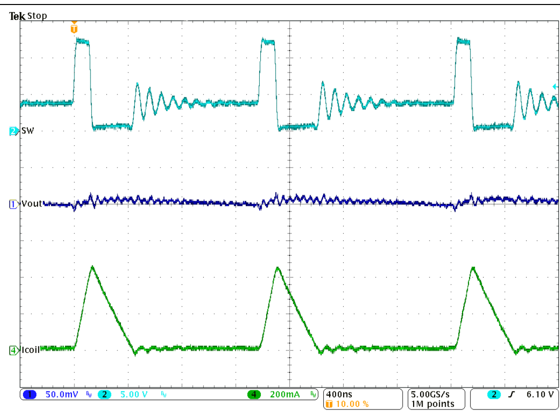
Iout = 100 mA

Figure 26. Startup to VOUT = 3.3 V



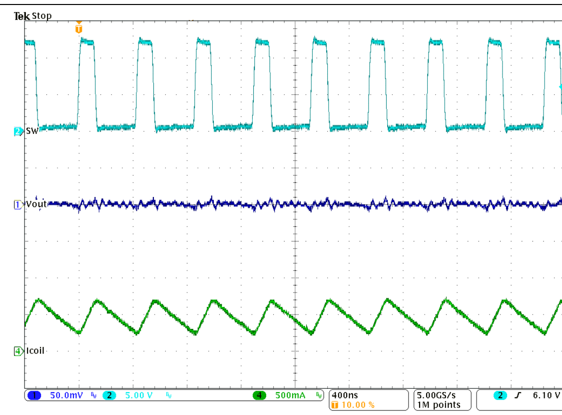
Iout = 500 mA

Figure 27. Startup to VOUT = 3.3 V



Iout = 66 mA

Figure 28. Typical Operation in Power Save Mode



Iout = 500 mA

Figure 29. Typical Operation in PWM Mode

9.3 System Examples

9.3.1 Inverting Power Supply

The TPS62170-Q1 can be used as inverting power supply by rearranging external circuitry as shown in Figure 30. As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} has to be limited for operation to the maximum supply voltage of 17 V (see Equation 13).

$$V_{IN} + |V_{OUT}| \le V_{IN\,max} \tag{13}$$

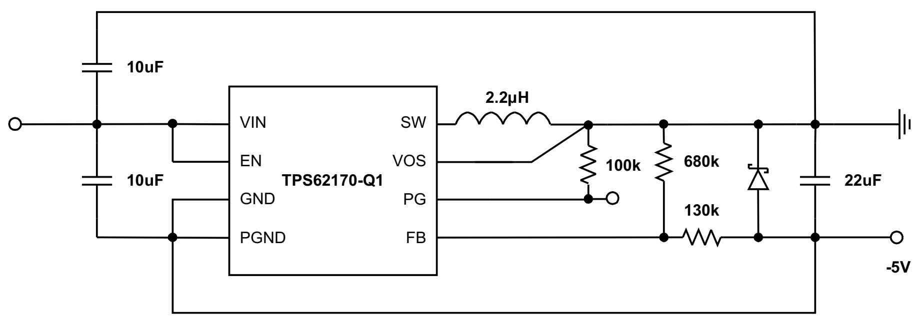


Figure 30. –5-V Inverting Power Supply

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted and an output capacitance of at least 22 µF is recommended. A detailed design example is given in SLVA469.

9.3.2 Various Output Voltages

The TPS62170-Q1 can be set for different output voltages between 0.9 V and 6 V. Some examples are shown below.

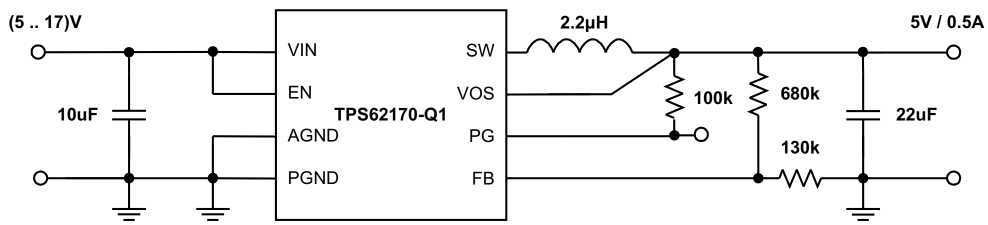


Figure 31. 5-V/0.5-A Power Supply

System Examples (continued)

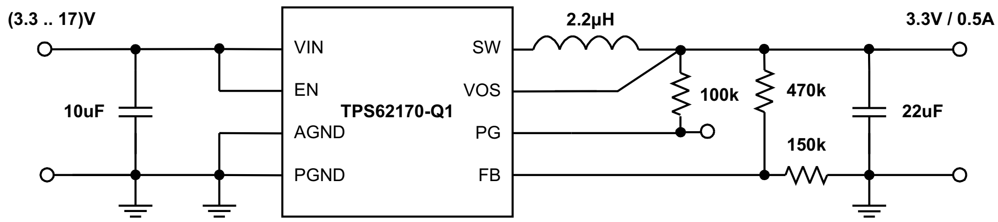


Figure 32. 3.3-V/0.5-A Power Supply

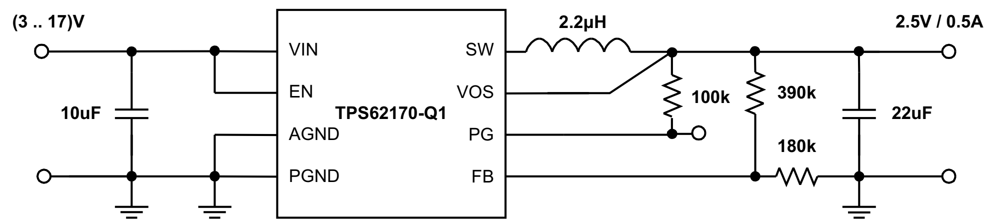


Figure 33. 2.5-V/0.5-A Power Supply

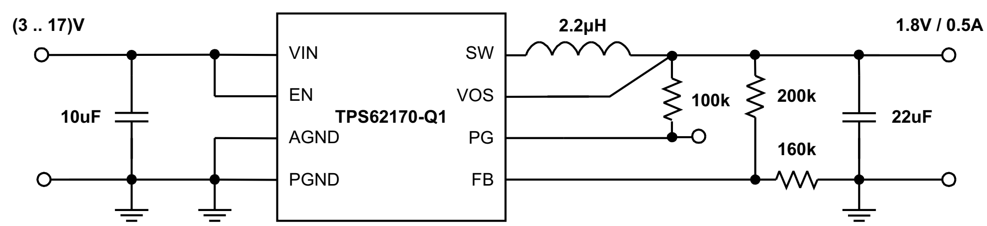


Figure 34. 1.8-V/0.5-A Power Supply

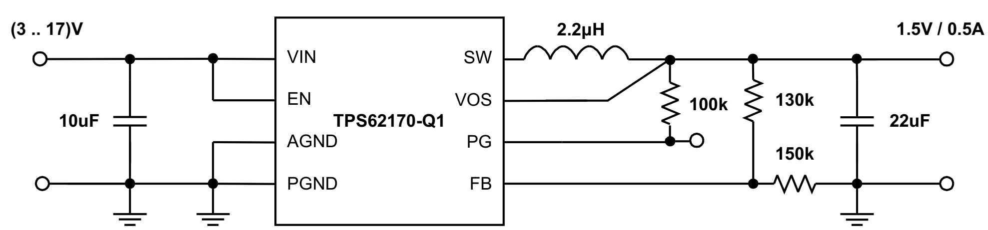


Figure 35. 1.5-V/0.5-A Power Supply

System Examples (continued)

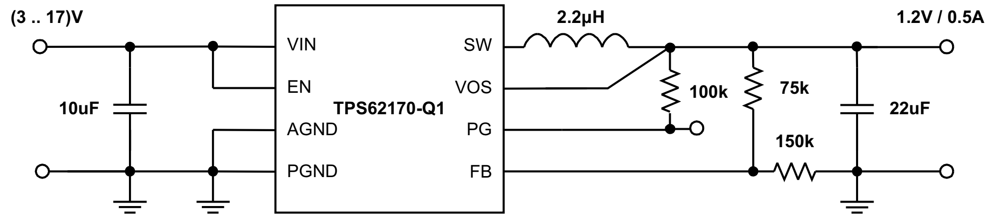


Figure 36. 1.2-V/0.5-A Power Supply

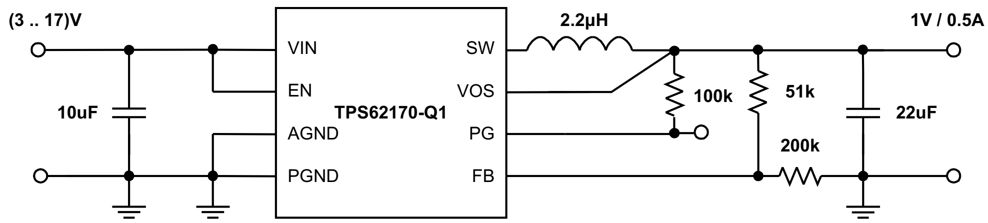


Figure 37. 1-V/0.5-A Power Supply

10 Power Supply Recommendations

The TPS6217x-Q1 are designed to operate from a 3-V to 17-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

11 Layout

11.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS6217x-Q1 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity. Considering the following topics ensures best electrical and optimized thermal performance:

1) The input capacitor must be placed as close as possible to the VIN and PGND pin of the IC. This provides low resistive and inductive path for the high di/dt input current.

2) The VOS pin must be connect in the shortest way to VOUT at the output capacitor - avoiding noise coupling.

3) The feedback resistors, R1 and R2 must be connected close to the FB and AGND pins - avoiding noise coupling.

4) The output capacitor should be placed such that its ground is as close as possible to the IC's PGND pins - avoiding additional voltage drop in traces.

5) The inductor should be placed close to the SW pin and connect directly to the output capacitor - minimizing the loop area between the SW pin, inductor, output capacitor and PGND pin.

More detailed information can be found in the *EVM Users Guide*, SLVU483.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation. Although the Exposed Thermal Pad can be connected to a floating circuit board trace, the device will have better thermal performance if it is connected to a larger ground plane. The Exposed Thermal Pad is electrically connected to AGND.

11.2 Layout Example

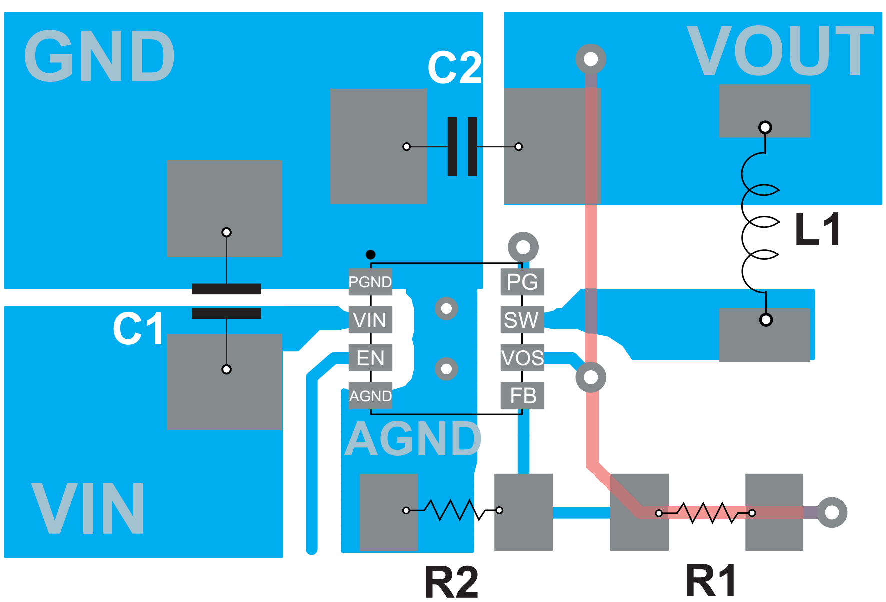


Figure 38. Layout Example

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the Exposed Thermal Pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note (SZZA017), and (SPRA953).

The TPS6217x-Q1 are designed for a maximum operating junction temperature (T_J) of 125°C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. Since the thermal resistance of the package is fixed, increasing the size of the surrounding copper area and improving the thermal connection to the IC can reduce the thermal resistance. To get an improved thermal behavior, it's recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

*12.1.1.1 使用 **WEBENCH®** 工具定制设计方案*

请单击此处，借助 WEBENCH® 电源设计器并使用 TPS62170-Q1 器件创建定制设计方案。

1. 在开始阶段键入输出电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

12.1.2 Third-Party Products Disclaimer

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12.2 文档支持

12.2.1 相关文档

应用报告《优化 TPS62130/40/50/60/70 输出滤波器》（文献编号：SLVA463）

应用报告《采用前馈电容优化内部补偿 DC-DC 转换器的瞬态响应》（文献编号：SLVA289）

应用报告《采用前馈电容优化 TPS62130/40/50/60/70 的稳定性和带宽》（文件编号：SLVA466）

应用报告《在反向降压/升压拓扑中使用 TPS6215x》（文献编号：SLVA469）

用户指南《TPS62160EVM-627 和 TPS62170EVM-627 评估模块》（文献编号：SLVU483）

应用报告《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》（文件编号：SZZA017）

应用报告《半导体和 IC 封装热指标》（文件编号：SPRA953）

12.3 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **4.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS62170-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62171-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62172-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 商标

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All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.7 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.8 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62170QDSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUEQ
TPS62170QDSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUEQ
TPS62170QDSGRQ1.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUEQ
TPS62170QDSGTQ1	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUEQ
TPS62170QDSGTQ1.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUEQ
TPS62170QDSGTQ1.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUEQ
TPS62171QDSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUFQ
TPS62171QDSGRQ1.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUFQ
TPS62171QDSGTQ1	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUFQ
TPS62171QDSGTQ1.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUFQ
TPS62172QDSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUGQ
TPS62172QDSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUGQ
TPS62172QDSGRQ1.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUGQ
TPS62172QDSGTQ1	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUGQ
TPS62172QDSGTQ1.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUGQ
TPS62172QDSGTQ1.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUGQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS62170-Q1, TPS62171-Q1, TPS62172-Q1 :

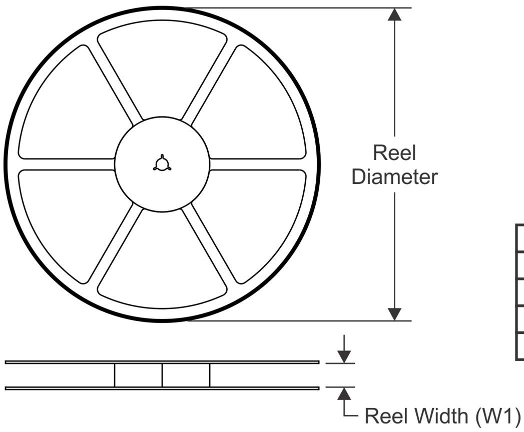
- Catalog : TPS62170, TPS62171, TPS62172

NOTE: Qualified Version Definitions:

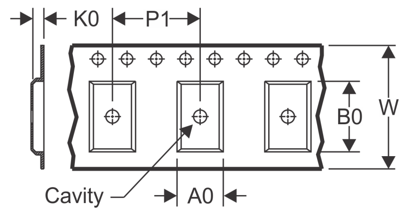
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

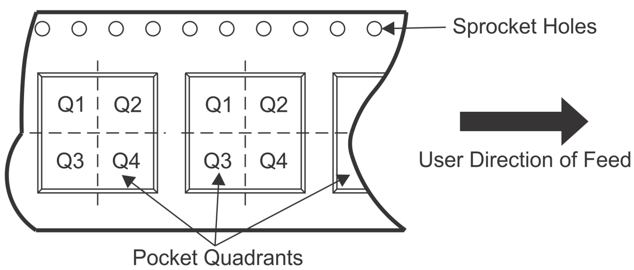


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

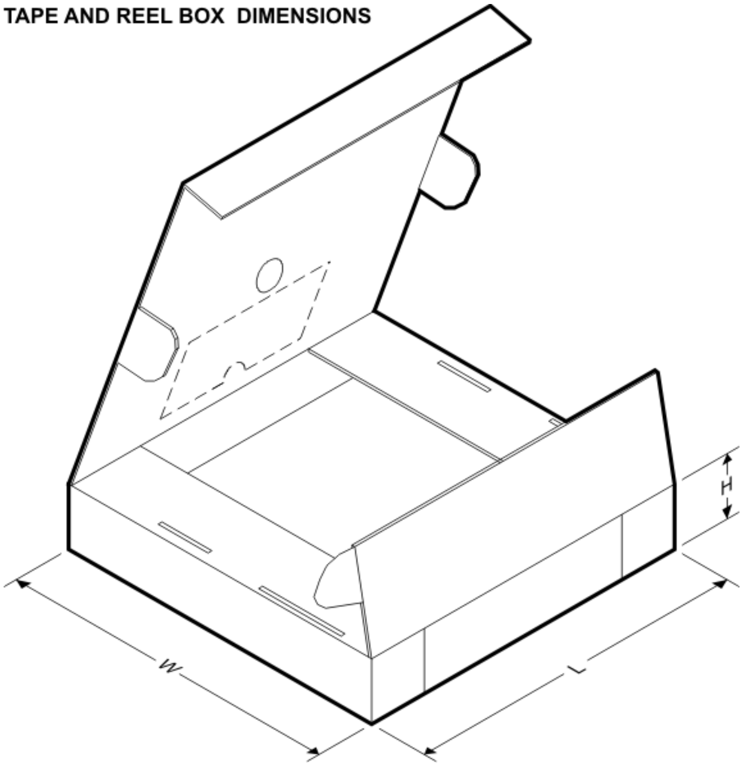
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62170QDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62170QDSGTQ1	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62171QDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62171QDSGTQ1	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62172QDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62172QDSGTQ1	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62170QDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62170QDSGTQ1	WSON	DSG	8	250	210.0	185.0	35.0
TPS62171QDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62171QDSGTQ1	WSON	DSG	8	250	210.0	185.0	35.0
TPS62172QDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62172QDSGTQ1	WSON	DSG	8	250	210.0	185.0	35.0

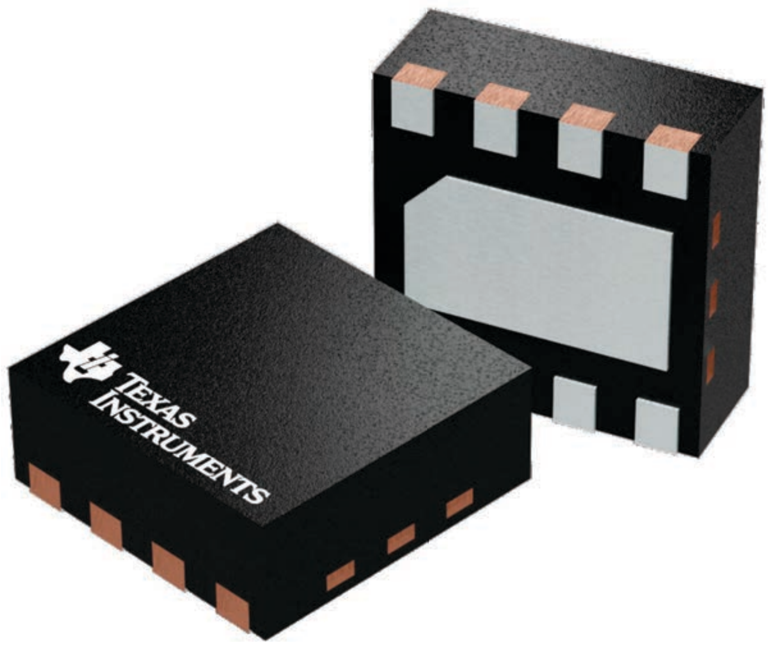
DSG 8

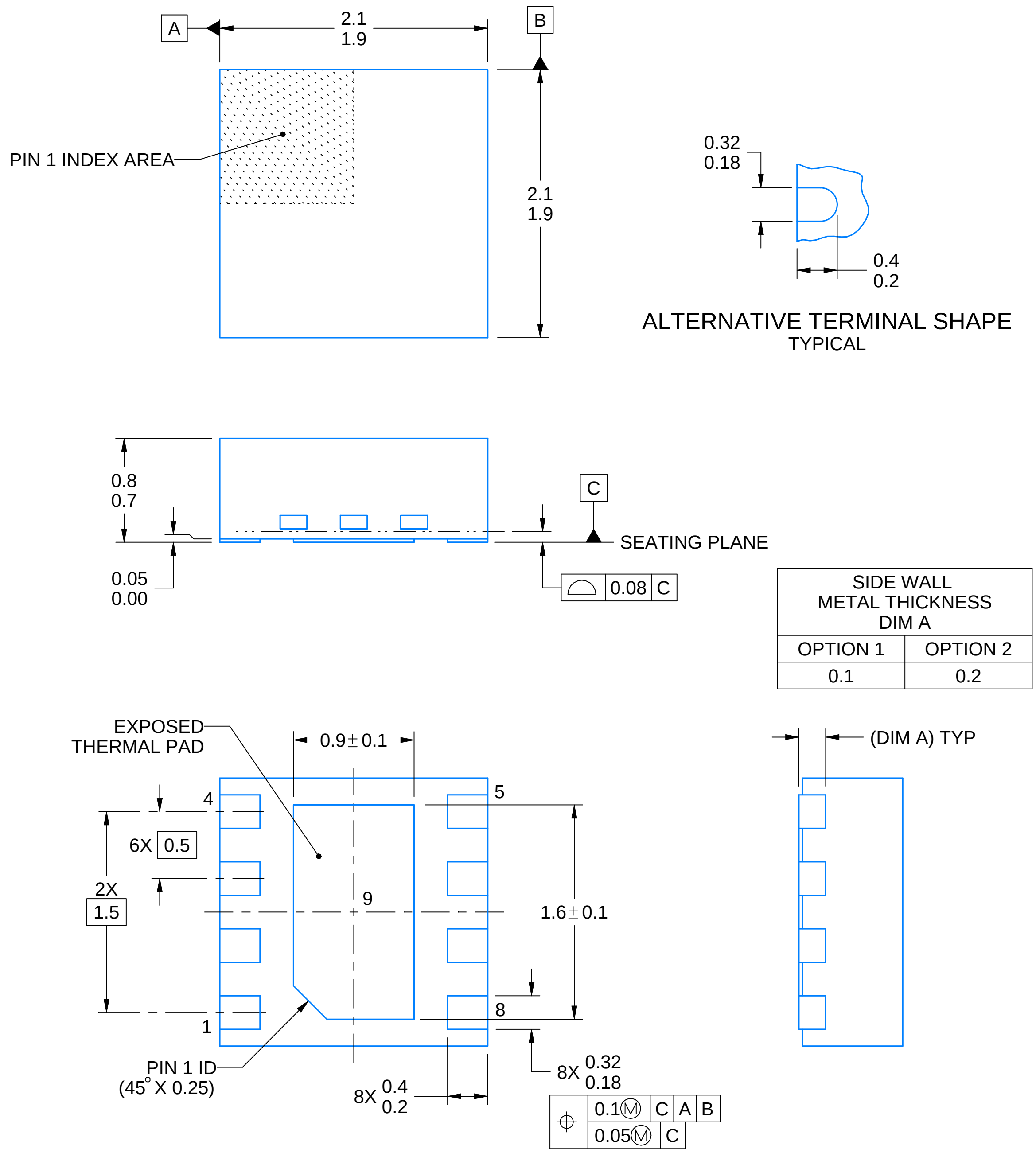
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



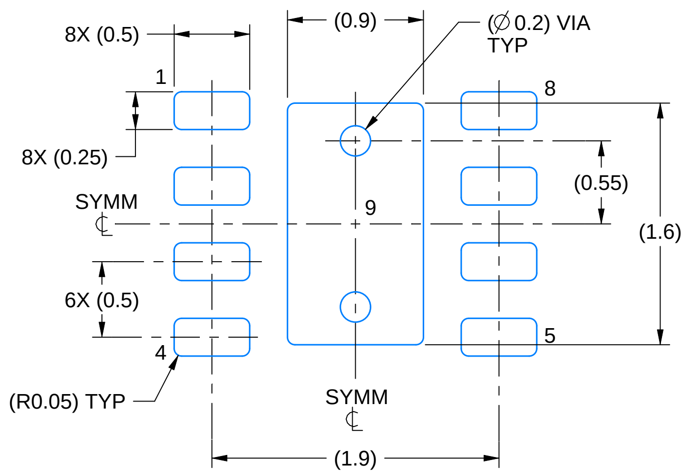


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

NON SOLDER MASK
DEFINED
(PREFERRED)

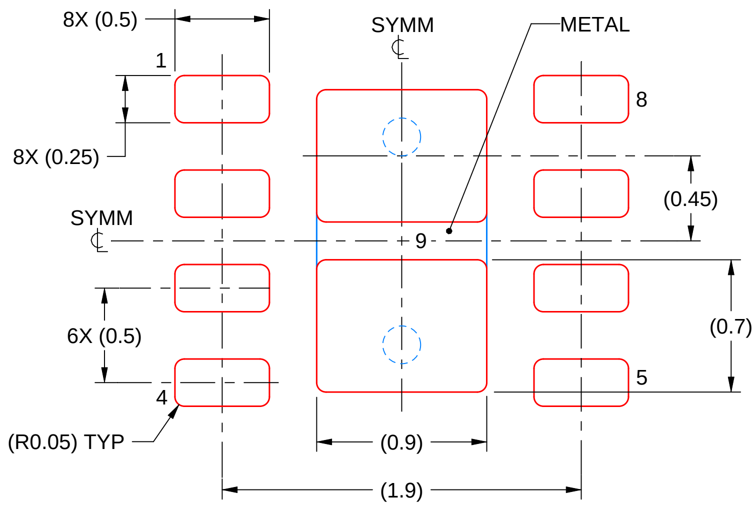
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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