TLV320x-Q1 40ns、微功耗、推挽式输出汽车比较器

1 特性

- 符合汽车应用 标准
- 具有符合 AEC Q100 的下列结果：
  - 器件温度等级 1：环境工作温度范围为 –40°C 至 +125°C
  - 器件 HBM ESD 分类等级 2 (TLV3201-Q1)
  - 器件 HBM ESD 分类等级 3A (TLV3202-Q1)
  - 器件 CDM ESD 分类等级 C5
- 低传播延迟：40ns
- 低静态电流：
  每通道 40µA
- 输入共模扩展范围扩展到任一电源轨之上 200mV
- 低输入偏移电压：1mV
- 推挽输出
- 电源范围：2.7V 至 5.5V
- 小型封装：
  5 引脚 SC70 和 8 引脚 VSSOP

2 应用

- 引擎控制单元 (ECU)
- 车身控制模块 (BCM)
- 电池管理系统 (BMS)
- HEV/EV 逆变器和电机控制
- 超声波测距和 LIDAR
- 转向和牵引控制器
- 乘员检测
- 信息娱乐系统

3 说明

TLV3201-Q1 和 TLV3202-Q1 分别属于单通道和双通道比较器，它们实现了高速度 (40ns) 与低功耗 (40µA) 的完美组合，两者均采用极小型封装，具有轨至轨输入、低偏移电压 (1mV) 和大输出驱动电流等 特性 。这些器件还很容易在响应时间至关重要的多种 应用 中实施。

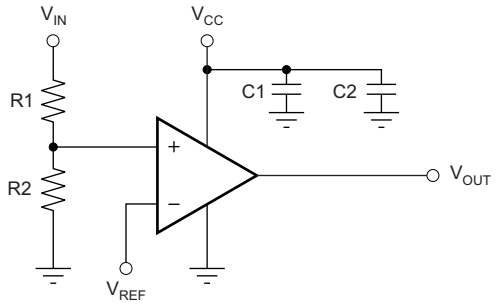
TLV320x-Q1 系列可提供单通道 (TLV3201-Q1) 和双通道 (TLV3202-Q1) 版本，这两个版本的器件都带有推挽输出。TLV3201-Q1 采用 5 引脚 SC70 封装。TLV3202-Q1 采用 8 引脚 VSSOP 封装。所有器件可在 -40°C 至 +125°C 的扩展工业温度范围内运行。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLV3201-Q1	SC70 (5)	2.00mm × 1.25mm
TLV3202-Q1	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

阈值检测器



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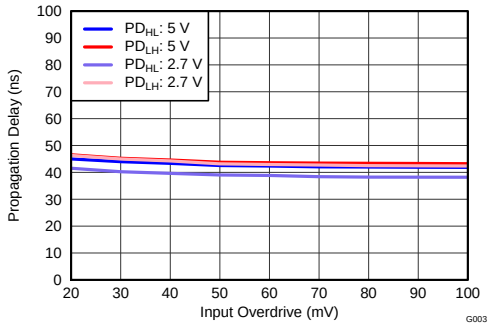
传播延迟与过驱动



目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 Device Comparison Table ... 2
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics: V_{CC} = 5 V ... 5
7.6 Electrical Characteristics: V_{CC} = 2.7 V ... 5
7.7 Switching Characteristics ... 6
7.8 Typical Characteristics ... 7
8 Detailed Description ... 11
8.1 Overview ... 11
8.2 Functional Block Diagram ... 11
8.3 Feature Description ... 11
8.4 Device Functional Modes ... 11
9 Application and Implementation ... 12
9.1 Application Information ... 12
9.2 Typical Applications ... 16
10 Power Supply Recommendations ... 18
11 Layout ... 19
11.1 Layout Guidelines ... 19
11.2 Layout Example ... 19
12 器件和文档支持 ... 20
12.1 器件支持 ... 20
12.2 文档支持 ... 20
12.3 相关链接 ... 20
12.4 接收文档更新通知 ... 21
12.5 社区资源 ... 21
12.6 商标 ... 21
12.7 静电放电警告 ... 21
12.8 Glossary ... 21
13 机械、封装和可订购信息 ... 21

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (February 2017) to Revision A	Page
• Changed figure 29	15

5 Device Comparison Table

DEVICE	DESCRIPTION
TLV3011	5-µA (maximum) open-drain, 1.8-V to 5.5-V with integrated voltage reference in 1.5-mm × 1.5-mm micro-sized packages
TLV3012	5-µA (maximum) push-pull, 1.8-V to 5.5-V with integrated voltage reference in micro-sized packages
TLV3501	4.5-ns, rail-to-rail, push-pull comparator in micro-sized packages
LMV7235	75-ns, 65-µA, 2.7-V to 5.5-V, rail-to-rail input comparator with open-drain output
LMV7239	75-ns, 65-µA, 2.7-V to 5.5-V, rail-to-rail input comparator with push-pull output
LMV7239-Q1	Automotive 75-ns, 65-µA, 2.7-V to 5.5-V, rail-to-rail input comparator with push-pull output
REF3333	30-ppm/°C drift, 3.9-µA, SOT23-3, SC70-3 voltage reference

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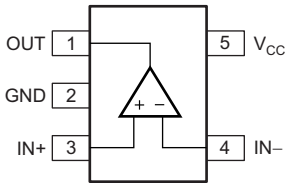
6 Pin Configuration and Functions

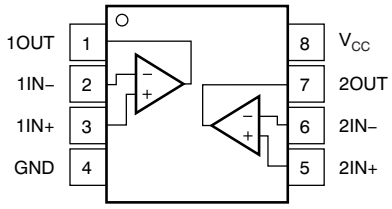
TLV3201-Q1 DCK Package
5-Pin SC70-5
Top View



Pin Functions: TLV3201-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Negative supply, ground
IN–	4	I	Negative input
IN+	3	I	Positive input
OUT	1	O	Output
V_{CC}	5	—	Positive supply

TLV3202-Q1 DGK Package
8-Pin VSSOP
Top View



Pin Functions: TLV3202-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Negative input, comparator 1
1IN+	3	I	Positive input, comparator 1
1OUT	1	O	Output, comparator 1
2IN–	6	I	Negative input, comparator 2
2IN+	5	I	Positive input, comparator 2
2OUT	7	O	Output, comparator 2
GND	4	—	Negative supply, ground
V_{CC}	8	—	Positive supply

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage		7	V
	Signal input pins(2)	–0.5	(V_{CC}) + 0.5	
Current	Signal input pins(2)	–10	10	mA
	Output short circuit(3)		100	
Temperature	Operating	–55	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground.

7.2 ESD Ratings

			VALUE	UNIT
TLV3201-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±3000	V
		Charged-device model (CDM), per AEC Q100-011	±750	
TLV3202-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V_{S+}) – ($V_{S–}$)	2.7 (±1.35)	5.5 (±2.75)	V
T_A	Specified temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLV3201-Q1 DCK (SC-70) 5 PINS	TLV3202-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	281.9	201.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.6	92.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.3	123.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	23	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.3	212.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics: V_{CC} = 5 V

at T_A = 25°C and V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input offset voltage	$V_{CM} = V_{CC} / 2$		1	5	mV
		T_A = –40°C to 125°C			6	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		1	10	µV/°C
PSRR	Power-supply rejection ratio	$V_{CM} = V_{CC} / 2$, V_{CC} = 2.5 V to 5.5 V	65	85		dB
	Input hysteresis			1.2		mV
INPUT BIAS CURRENT						
I_{IB}	Input bias current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			5	nA
I_{IO}	Input offset current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			2.5	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	T_A = –40°C to 125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio	–0.2 V < V_{CM} < 5.2 V	60	70		dB
INPUT IMPEDANCE						
	Common mode			10^{13} || 2		Ω || pF
	Differential			10^{13} || 4		Ω || pF
OUTPUT						
V_{OL}	Voltage output swing from lower rail	I_{SINK} = 4 mA		175	190	mV
		T_A = –40°C to 125°C			225	
V_{OH}	Voltage output swing from upper rail	I_{SOURCE} = 4 mA		120	140	mV
		T_A = –40°C to 125°C			170	
I_{SC}	Short-circuit current (per comparator)	I_{SC} sinking	40	48		mA
		T_A = –40°C to 125°C		See Figure 14		
		I_{SC} sourcing	52	60		
		T_A = –40°C to 125°C		See Figure 14		
POWER SUPPLY						
V_{CC}	Specified voltage		2.7		5.5	V
I_Q	Quiescent current	T_A = 25°C		40	50	µA
		T_A = –40°C to 125°C			65	

7.6 Electrical Characteristics: V_{CC} = 2.7 V

at T_A = 25°C and V_{CC} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input offset voltage	$V_{CM} = V_{CC} / 2$		1	5	mV
		T_A = –40°C to 125°C			6	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		1	10	µV/°C
PSRR	Power-supply rejection ratio	$V_{CM} = V_{CC} / 2$, V_{CC} = 2.5 V to 5.5 V	65	85		dB
	Input hysteresis			1.2		mV
INPUT BIAS CURRENT						
I_{IB}	Input bias current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			5	nA
I_{IO}	Input offset current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			2.5	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	T_A = –40°C to 125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio	–0.2 V < V_{CM} < 2.9 V	56	68		dB

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Electrical Characteristics: V_{CC} = 2.7 V (continued)

at T_A = 25°C and V_{CC} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT IMPEDANCE						
	Common mode			10^{13} || 2		Ω || pF
	Differential			10^{13} || 4		Ω || pF
OUTPUT						
V_{OL}	Voltage output swing from lower rail	I_{SINK} = 4 mA		230	260	mV
		T_A = –40°C to 125°C			325	
V_{OH}	Voltage output swing from upper rail	I_{SOURCE} = 4 mA		210	250	mV
		T_A = –40°C to 125°C			350	
I_{SC}	Short-circuit current (per comparator)	I_{SC} sinking	13	19		mA
		T_A = –40°C to 125°C	See Figure 14			
		I_{SC} sourcing	15	21		
		T_A = –40°C to 125°C	See Figure 14			
POWER SUPPLY						
V_{CC}	Specified voltage		2.7		5.5	V
I_Q	Quiescent current	T_A = 25°C		36	46	µA
		T_A = –40°C to 125°C			60	

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay time	Low to high	Input overdrive = 20 mV, C_L = 15 pF		47	50	ns
			Input overdrive = 100 mV, C_L = 15 pF		42	50	
			T_A = –40°C to 125°C			55	
		High to low	Input overdrive = 20 mV, C_L = 15 pF		40	50	
			Input overdrive = 100 mV, C_L = 15 pF		38	50	
			T_A = –40°C to 125°C			55	
	Propagation delay skew	Input overdrive = 20 mV, C_L = 15 pF			2		ns
	Propagation delay matching (TLV3202-Q1)	High to low or low to high, input overdrive = 20 mV, C_L = 15 pF				5	ns
t_R	Rise time	10% to 90%			2.9		ns
t_F	Fall time	10% to 90%			3.7		ns

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7.8 Typical Characteristics

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

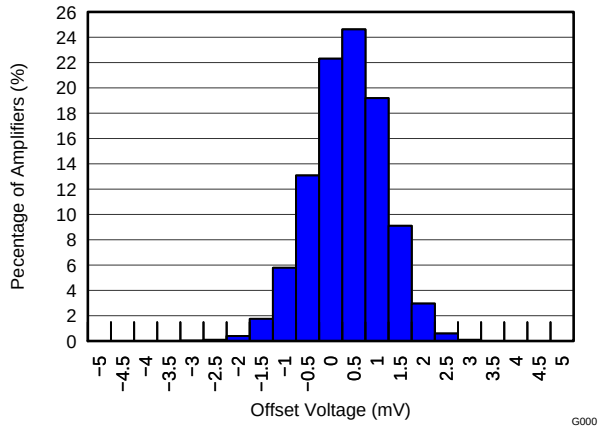

Figure 1. Offset Voltage Distribution

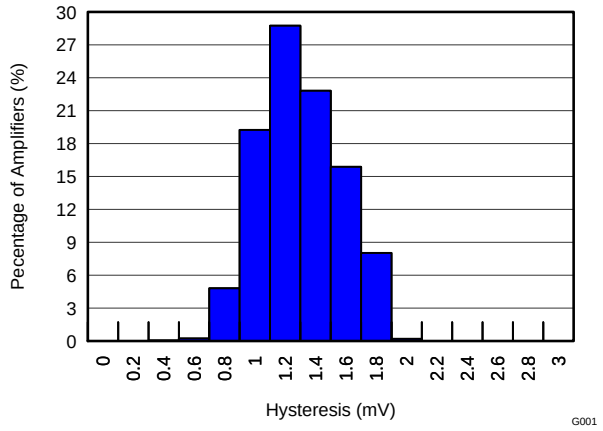

Figure 2. Hysteresis Distribution

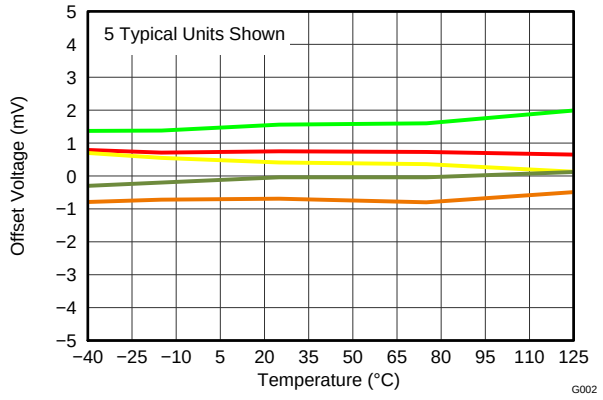

Figure 3. Offset Voltage vs Temperature

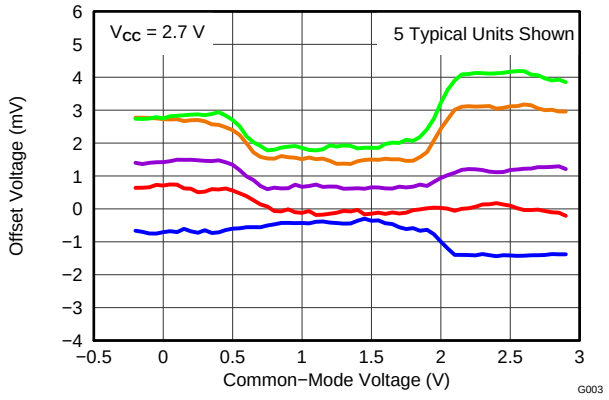

Figure 4. Offset Voltage vs Common-Mode Voltage

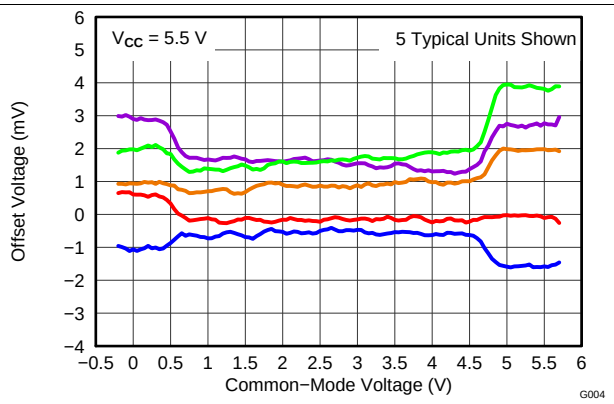

Figure 5. Offset Voltage vs Common-Mode Voltage

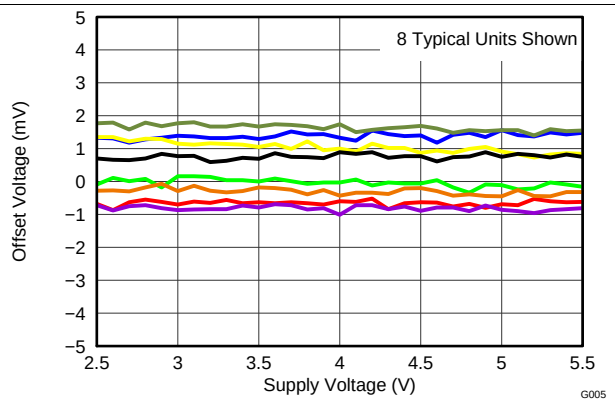

Figure 6. Offset Voltage vs Power Supply

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Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

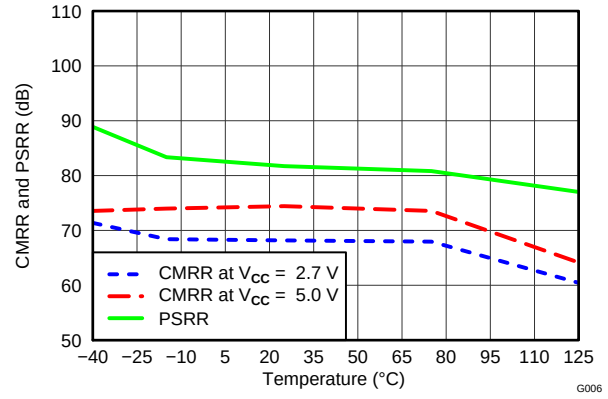

Figure 7. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

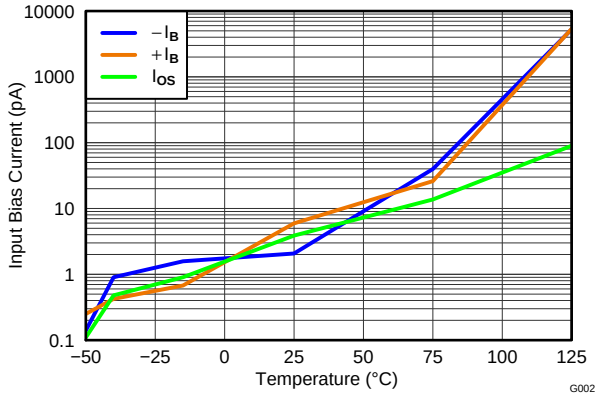

Figure 8. Input Bias Current and Input Offset Current vs Temperature

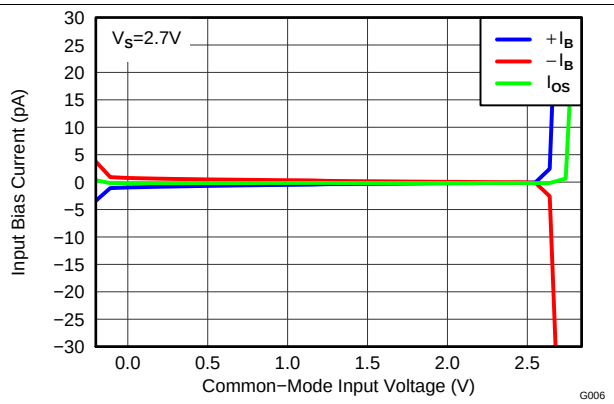

Figure 9. Input Bias Current and Input Offset Current vs Common-Mode Input Voltage

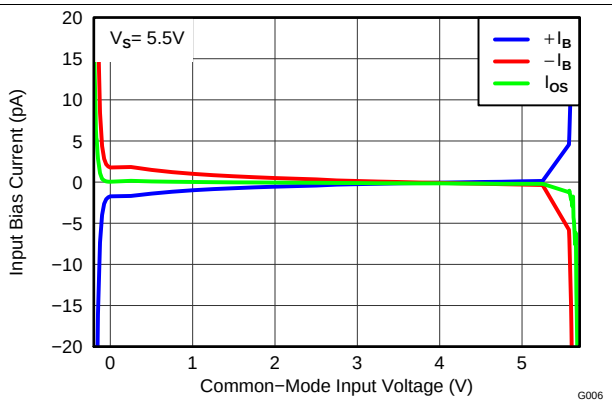

Figure 10. Input Bias Current and Input Offset Current vs Common-Mode Input Voltage

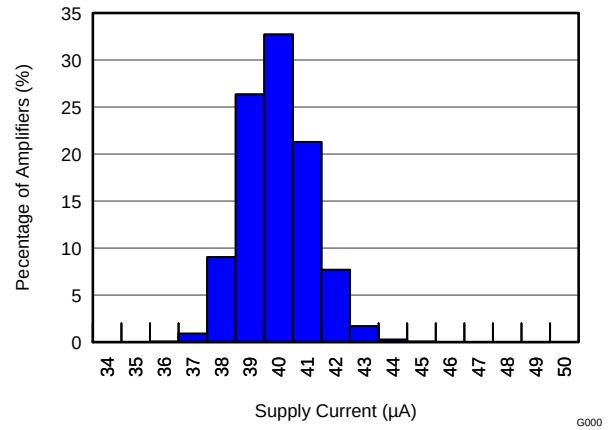

Figure 11. Quiescent Current Distribution

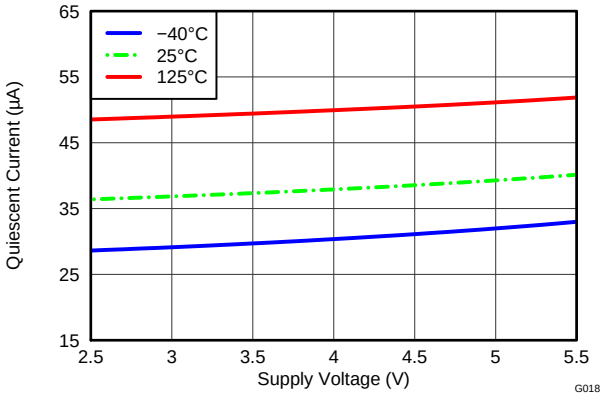

Figure 12. Quiescent Current vs Supply Voltage

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Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

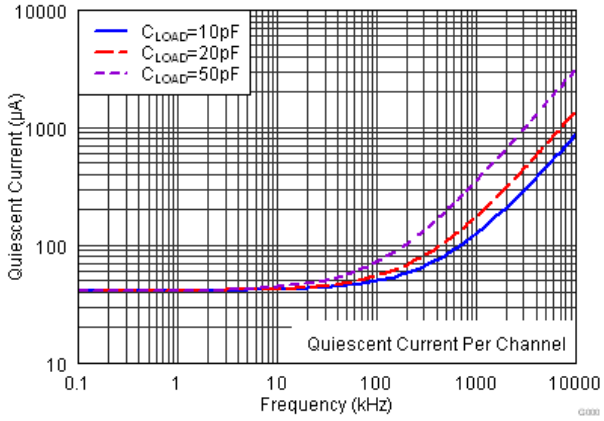

Figure 13. Quiescent Current vs Switching Frequency

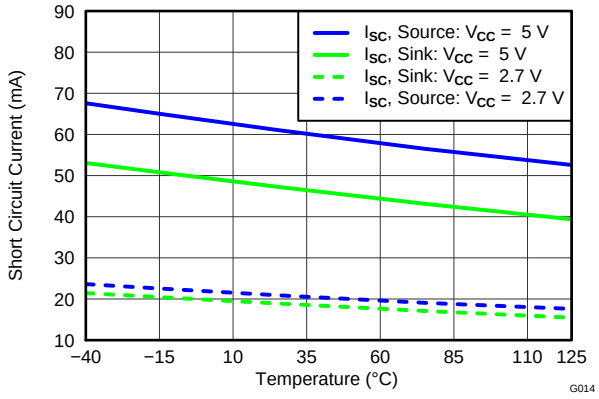

Figure 14. Short-Circuit Current vs Temperature

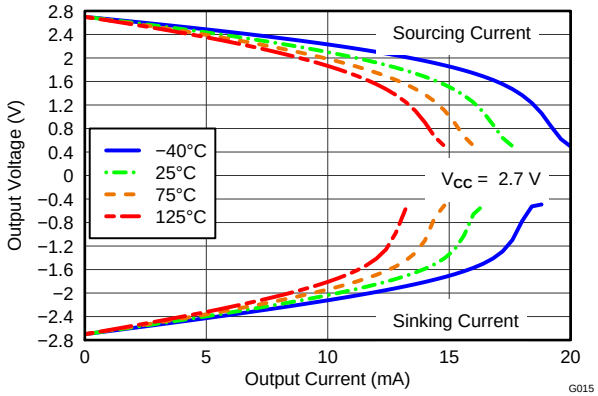

Figure 15. Output Voltage vs Output Current

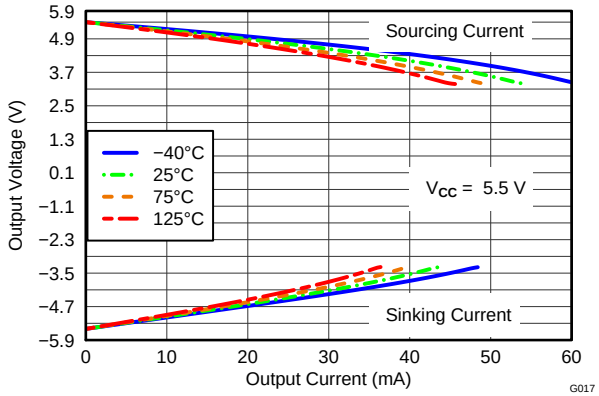

Figure 16. Output Voltage vs Output Current

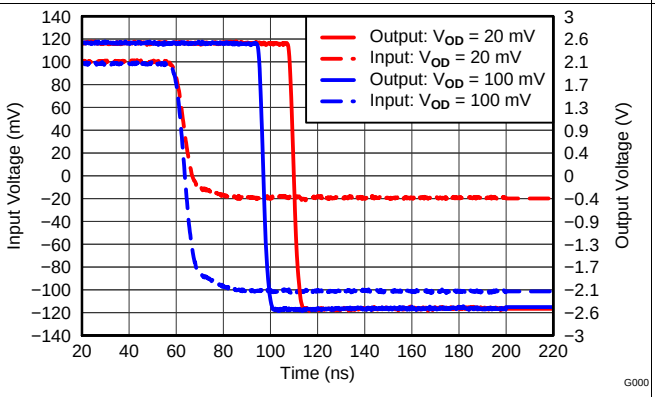

Figure 17. Propagation Delay Falling Edge

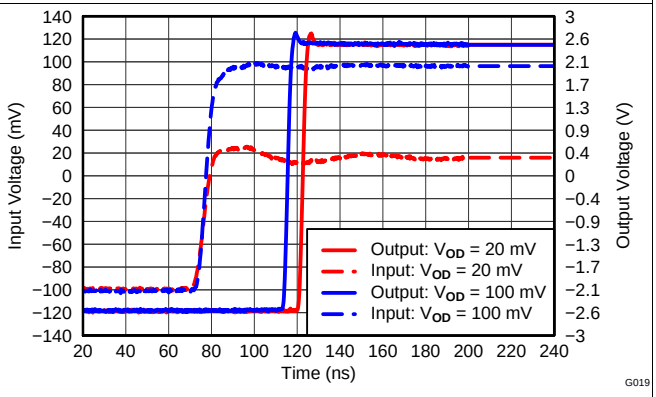

Figure 18. Propagation Delay Rising Edge

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Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

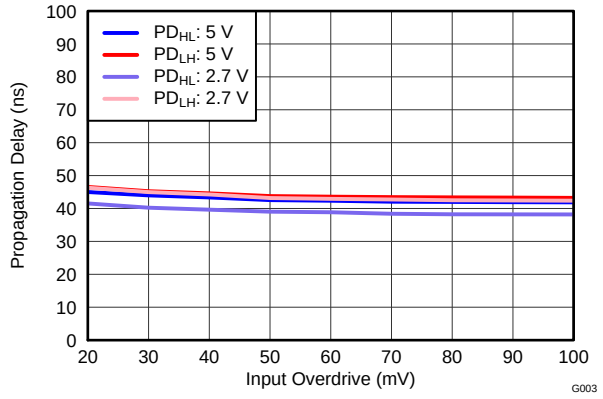

Figure 19. Propagation Delay vs Input Overdrive

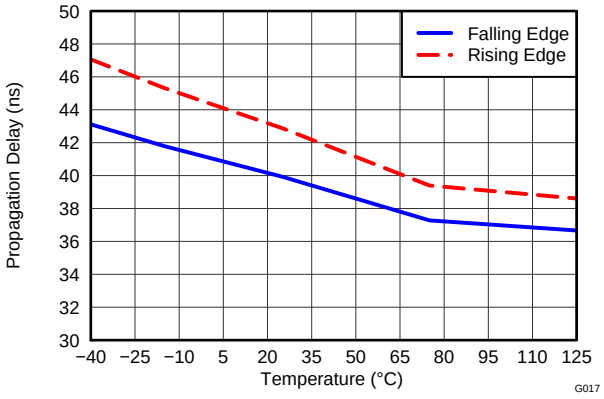

Figure 20. Propagation Delay vs Temperature

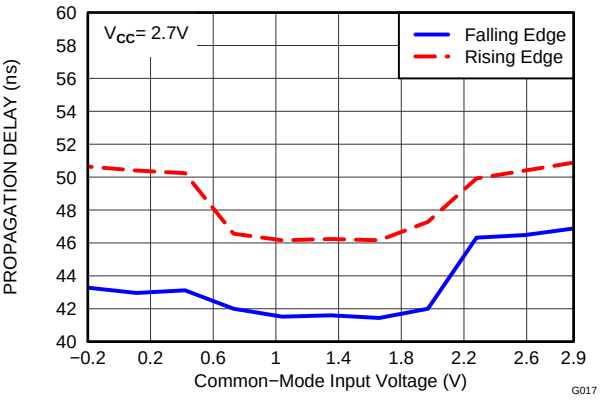

Figure 21. Propagation Delay vs Common-Mode Voltage

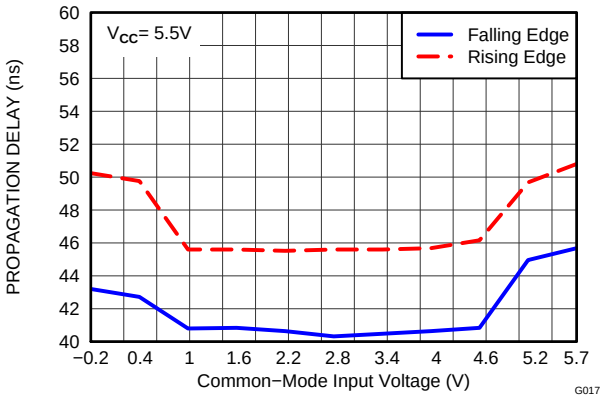

Figure 22. Propagation Delay vs Common-Mode Voltage

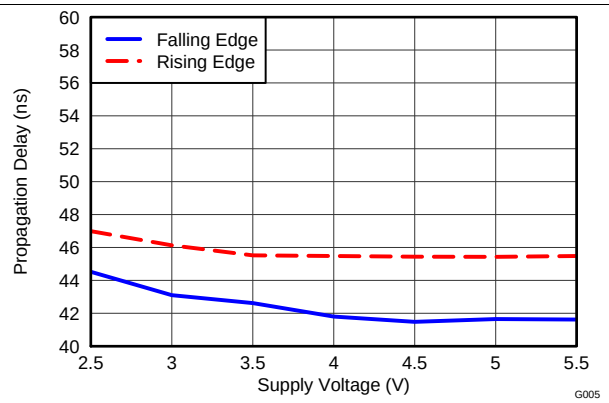

Figure 23. Propagation Delay vs Supply Voltage

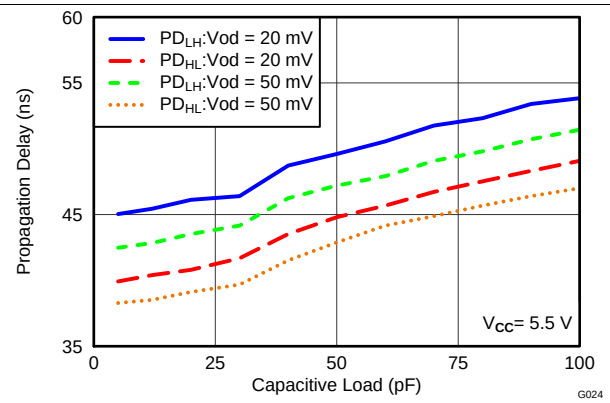

Figure 24. Propagation Delay vs Capacitive Load

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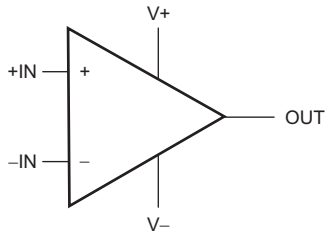
8 Detailed Description

8.1 Overview

The TLV3201-Q1 and TLV3202-Q1 devices feature 40-ns response time and include 1.2 mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.2 V beyond the power-supply rails.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Operating Voltage

The TLV3201-Q1 and TLV3202-Q1 comparators are specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ±1.35 V to ±2.75 V) over a temperature range of −40°C to +125°C. The device continues to function below this range, but performance is not specified.

8.3.2 Input Overvoltage Protection

The device inputs are protected by electrostatic discharge (ESD) diodes that conduct if the input voltages exceed the power supplies by more than approximately 300 mV. Momentary voltages greater than 300 mV beyond the power supply can be tolerated if the input current is limited to 10 mA. This limiting is easily accomplished with a small input resistor in series with the input to the comparator.

8.4 Device Functional Modes

The device is fully functional when powered by rail-to-rail supply voltage greater than 2.7 V.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV3201-Q1 and TLV3202-Q1 are single- and dual-supply (respectively), push-pull comparators featuring 40 ns of propagation delay on only 40 µA of supply current. This combination of fast response time and minimal power consumption make the TLV3201-Q1 and TLV3202-Q1 excellent comparators for portable, battery-powered applications as well as fast-switching threshold detection such as pulse-width modulation (PWM) output monitors and zero-cross detection.

9.1.1 Comparator Inputs

The TLV3201-Q1 and TLV3202-Q1 are rail-to-rail input comparators, with an input common-mode range that exceeds the supply rails by 200 mV for both positive and negative supplies. The devices are specified from 2.7 V to 5.5 V, with room temperature operation from 2.5 V to 5.5 V. The TLV3201-Q1 and TLV3202-Q1 are designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 25 shows the TLV320x-Q1 response when input voltages exceed the supply, resulting in no phase inversion.

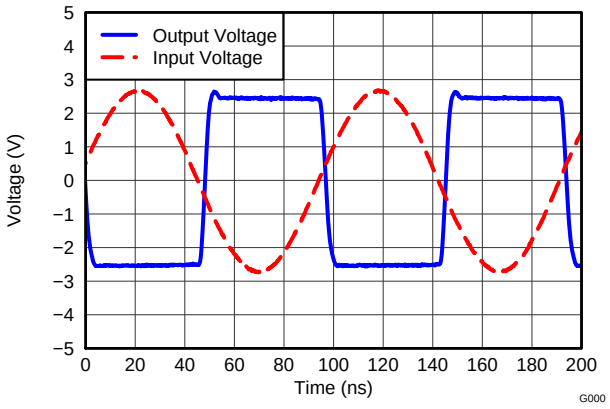

Figure 25. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

The ESD protection input structure of two back-to-back diodes and 1-kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed V_{CC} beyond the specified operating conditions. If potential overvoltage conditions that exceed absolute maximum ratings are present, the addition of external bypass diodes and resistors is recommended, as shown in Figure 26. Large differential voltages greater than the supply voltage must be avoided to prevent damage to the input stage.

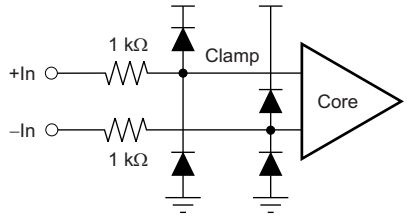

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Figure 26. TLV3201-Q1 Equivalent Input structure

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Application Information (continued)

9.1.2 External Hysteresis

The TLV3201-Q1 and TLV3202-Q1 have a hysteresis transfer curve (shown in Figure 27) that is a function of three components: V_{TH}, V_{OS}, and V_{HYST}.

- V_{TH}: the actual set voltage or threshold trip voltage
- V_{OS}: the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST}: internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

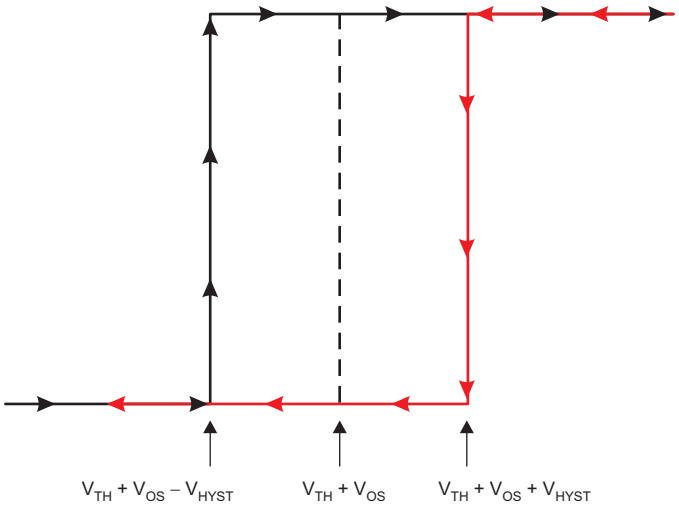

Figure 27. TLV320x-Q1 Hysteresis Transfer Curve

9.1.2.1 Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 28. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. The lower input trip voltage (V_{A1}) is defined by Equation 1.

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When V_{IN} is greater than [V_A × (V_{IN} > V_A)], the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. The upper trip voltage (V_{A2}) is defined by Equation 2.

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

The total hysteresis provided by the network is defined by Equation 3.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

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Application Information (continued)

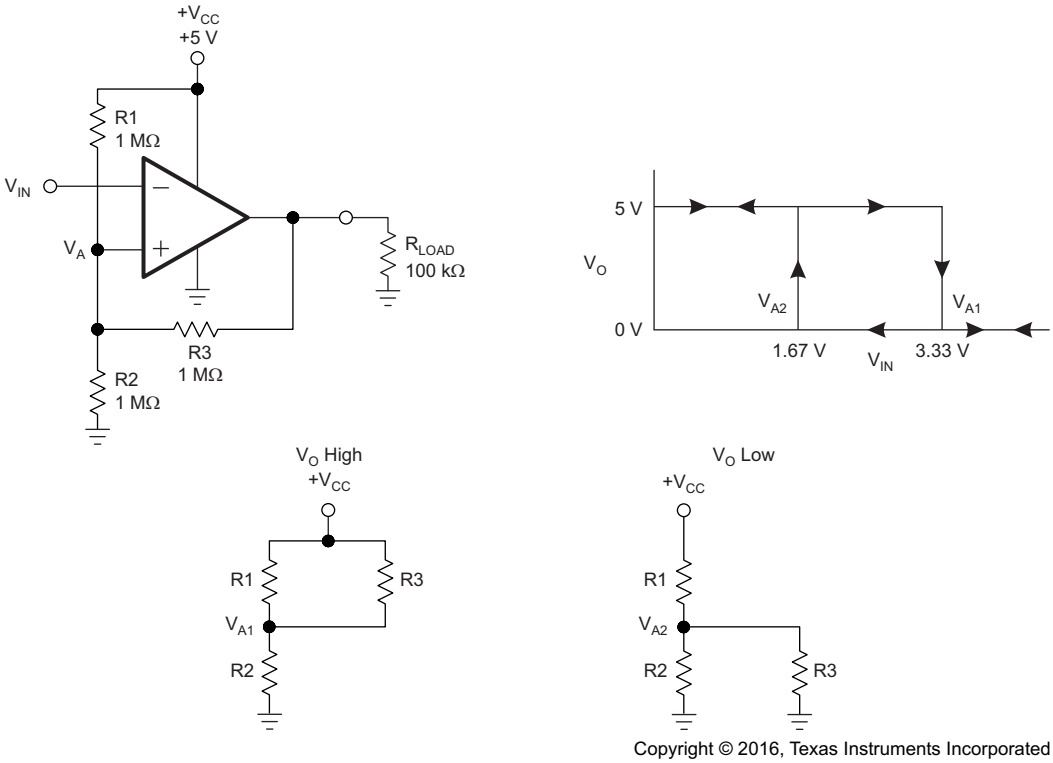

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Figure 28. TLV3201-Q1 in Inverting Configuration With Hysteresis

9.1.2.2 Noninverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 29 and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1}. V_{IN1} is calculated by Equation 4.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} \times V_{REF} \tag{4}$$

When V_{IN} is high, the output is also high. In order for the comparator to switch back to a low state, V_{IN} must equal V_{REF} before V_A is again equal to V_{REF}. V_{IN} can be calculated by Equation 5.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as defined by Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

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Application Information (continued)

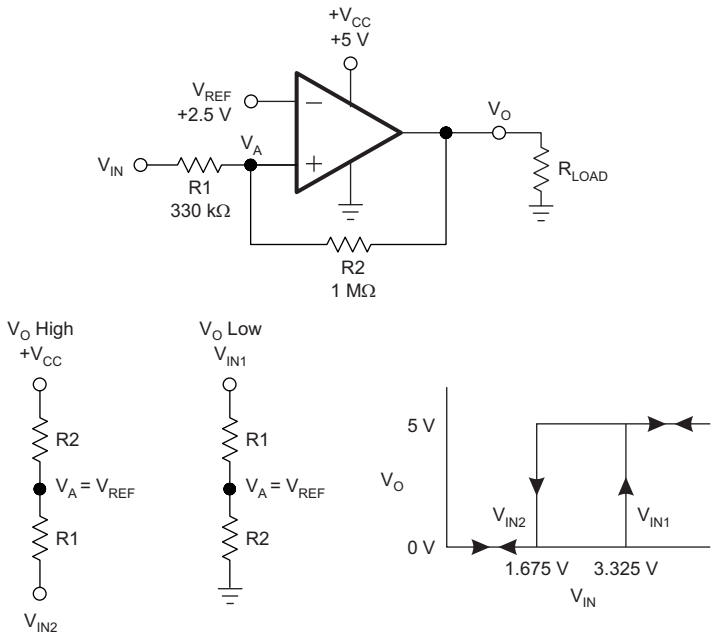

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Figure 29. TLV3201-Q1 in Noninverting Configuration With Hysteresis

9.1.3 Capacitive Loads

The TLV3201-Q1 and TLV3202-Q1 feature a push-pull output. When the output switches, there is a direct path between V_{CC} and ground, causing increased output sinking or sourcing current during the transition. Following the transition the output current decreases and supply current returns to 40 µA, thus maintaining low power consumption. Under reasonable capacitive loads, the TLV3201-Q1 and TLV3202-Q1 maintain specified propagation delay (see *Typical Characteristics*), but excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

9.2 Typical Applications

9.2.1 TLV3201-Q1 Configured as an AC-Coupled Comparator

One of the benefits of ac coupling a single-supply comparator circuit is that it can block dc offsets induced by ground-loop offsets that could potentially produce either a false trip or a common-mode input violation. Figure 30 shows the TLV3201-Q1 configured as an ac-coupled comparator.

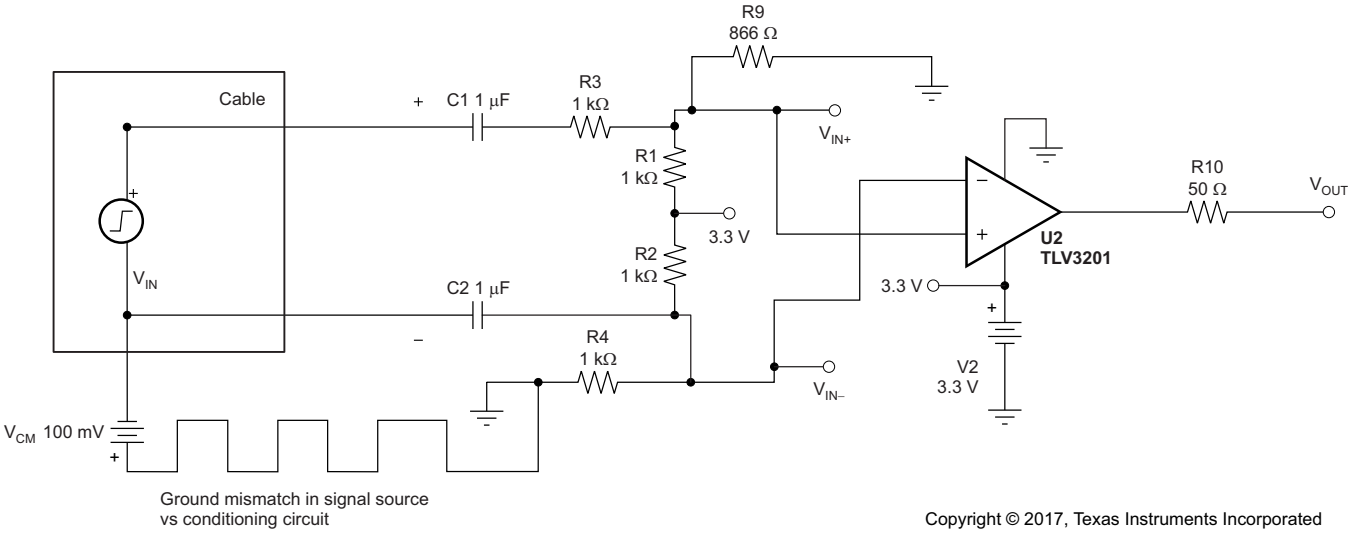

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Figure 30. TLV3201-Q1 Configured as an AC-Coupled Comparator (Schematic)

9.2.1.1 Design Requirements

Design requirements include:

- Ability to tolerate up to ±100 mV of common-mode signal.
- Trigger only on ac signals (such as zero-cross detection).

9.2.1.2 Detailed Design Procedure

Design analysis:

- AC-coupled, high-pass frequency
- Large capacitors require longer start-up time from device power on
- Use 1-µF capacitor to achieve high-pass frequency of approximately 159 Hz
- For high-pass equivalent, use C_{IN} = 0.5 µF, R_{IN} = 2 kΩ
  1. Set up input dividers initially for one-half supply (to be in center of acceptable common-mode range).
  2. Adjust either divider slightly upwards or downwards as desired to establish quiescent output condition.
  3. Select coupling capacitors based on lowest expected frequency.

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Typical Applications (continued)

9.2.1.3 Application Curve

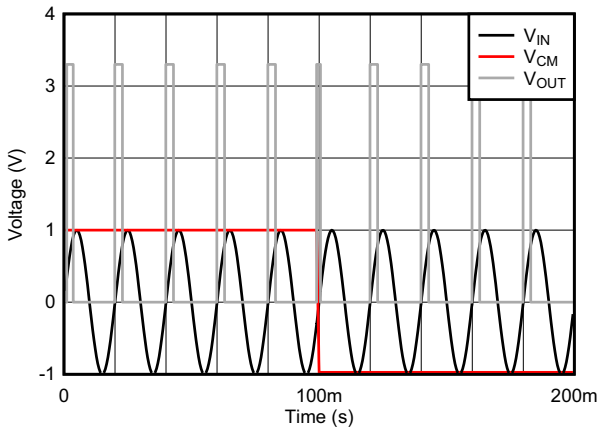

Figure 31. AC-Coupled Comparator Results

9.2.2 TLV3201-Q1 and OPA320 Configured as a Fast-Response Output Current Monitor

Figure 32 shows a single-supply current monitor configured as a difference amplifier with a gain of 50 to trip at 500µA. The OPA320 was chosen for this circuit because of its gain bandwidth (20 MHz), which allows higher speed triggering and monitoring of the current across the shunt resistor followed by the fast response of the TLV3201-Q1.

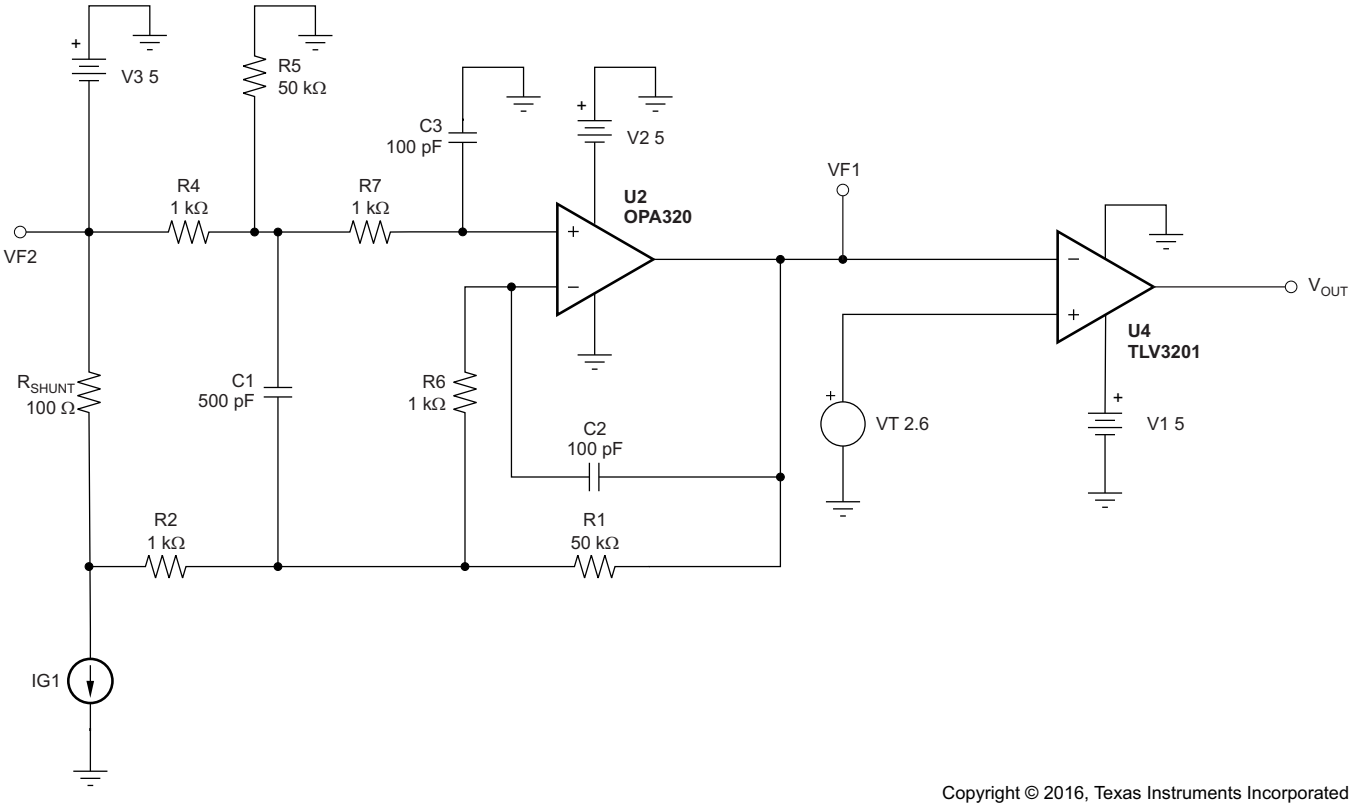

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Figure 32. TLV3201-Q1 and OPA320 Configured as a Fast-Response Output Current Monitor

Typical Applications (continued)

9.2.3 TLV3201-Q1 and TMP20 Configured as a Precision Analog Temperature Switch

Figure 33 shows the TMP20 and TLV3201-Q1 designed as a high-speed temperature switch. The TMP20 is an analog output temperature sensor where output voltage decreases with temperature. The comparator output is tripped when the output reaches a critical trip threshold.

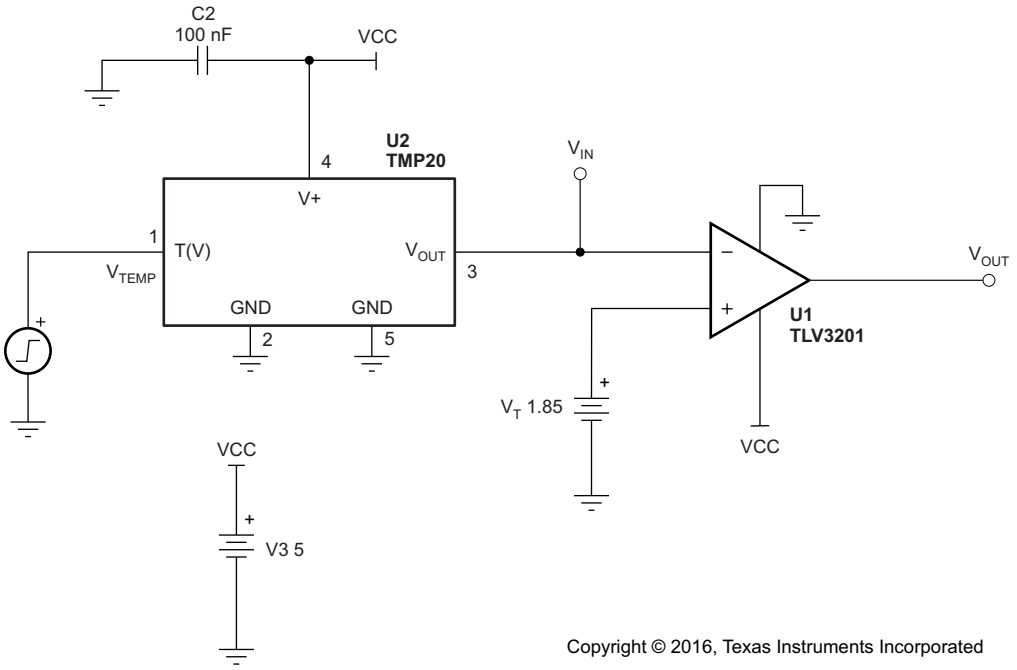

Figure 33. TLV3201-Q1 and TMP20 Configured as a Precision Analog Temperature Switch

10 Power Supply Recommendations

The TLV3201-Q1 and TLV3202-Q1 comparators are specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ±1.35 V to ±2.75 V) over a temperature range of −40°C to +125°C. The device continues to function below this range, but performance is not specified. Place bypass capacitors close to the power-supply pins to reduce noise coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

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11 Layout

11.1 Layout Guidelines

The TLV3201-Q1 and TLV3202-Q1 are fast-switching, high-speed comparators and require high-speed layout considerations. For best results, maintain the following layout guidelines:

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane.
- Place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane runs between the output and inputs.
- The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

11.2 Layout Example

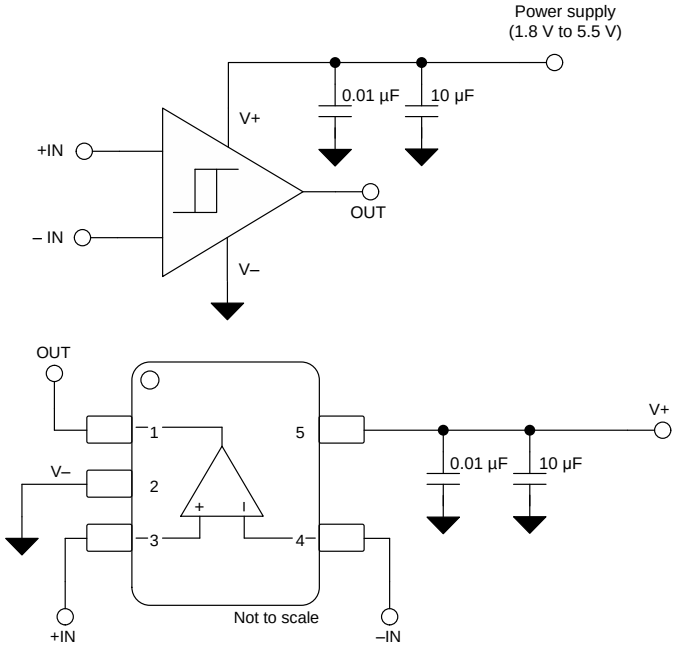

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Figure 34. TLV3201-Q1 SOT-23 Board Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 TINA-TI™ 仿真软件（免费下载）

TINA-TI™软件基于 SPICE 引擎，是一款简单易用、功能强大的电路仿真程序。TINA-TI 软件是 TINA 软件的一款免费的全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 软件提供所有传统的 SPICE 直流、瞬态和频域分析以及其他设计功能。

TINA-TI 软件可从模拟电子实验室设计中心免费下载，它可提供广泛的后处理功能，使用户能够以多种方式设置结果的格式。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

12.1.1.2 通用运算放大器评估模块 (EVM)

通用运放 EVM 是一系列通用空白电路板，可简化采用各种 IC 封装类型的电路板原型设计。虽然主要用于运算放大器，但引脚排列与 TLV320x-Q1 比较器相同，可用于轻松快速地对比较器电路进行原型设计。共有 5 个模型可供选用，每个模型都对应一种特定封装类型。支持 PDIP、SOIC、MSOP、TSSOP 和 SOT23 封装。

注

这些电路板均为空白电路板，用户必须自行提供 IC。TI 建议您在订购通用运算放大器 EVM 时申请几个运算放大器器件样品。

12.1.1.3 TI 高精度设计

TI 高精度设计的模拟设计方案是由 TI 公司高精度模拟实验室设计 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。

12.1.1.4 WEBENCH®滤波器设计器

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。WEBENCH Filter Designer 通过选择 TI 运算放大器以及 TI 供应商合作伙伴的无源组件来构建优化滤波器设计方案。在比较器前放置滤波器可以大大提升噪声抑制性能，避免错误触发。WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® Filter Designer。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

12.2 文档支持

12.2.1 相关文档

使用 TLV320x-Q1 时，建议参考下列相关文档。除非另外注明，否则这些文档均可从 www.ti.com 下载。

- *《使用 UCC28950 和 TLV3201 实现频率抖动》*
- *《使用 UCC28180 和 TLV3201 实现频率抖动》*
- *《具有迟滞功能的比较器参考设计》*

12.3 相关链接

表 1 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 1. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TLV3201-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

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相关链接 (接下页)

表 1. 相关链接 (接下页)

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TLV3202-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.6 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
DesignSoft is a trademark of DesignSoft, Inc.
TINA-TI is a trademark of Texas Insturments and DesignSoft, Inc..
All other trademarks are the property of their respective owners.

12.7 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV3201AQDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5HF
TLV3201AQDCKRQ1.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5HF
TLV3202AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1C8Q
TLV3202AQDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1C8Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLV3201-Q1, TLV3202-Q1 :

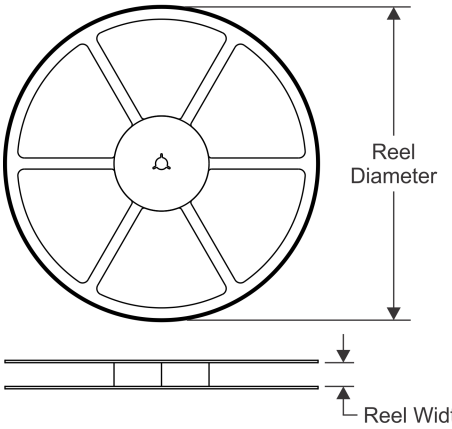
- Catalog : TLV3201, TLV3202

NOTE: Qualified Version Definitions:

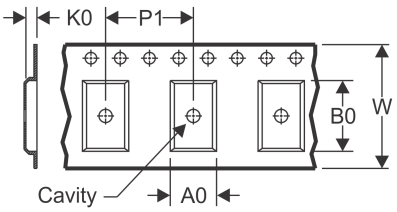
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

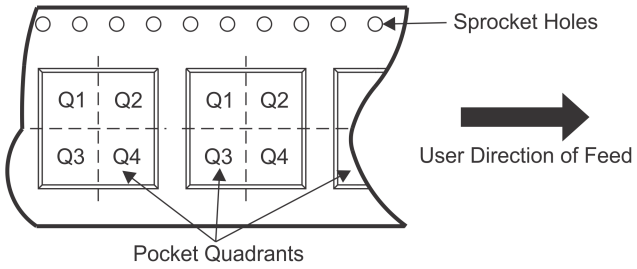


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

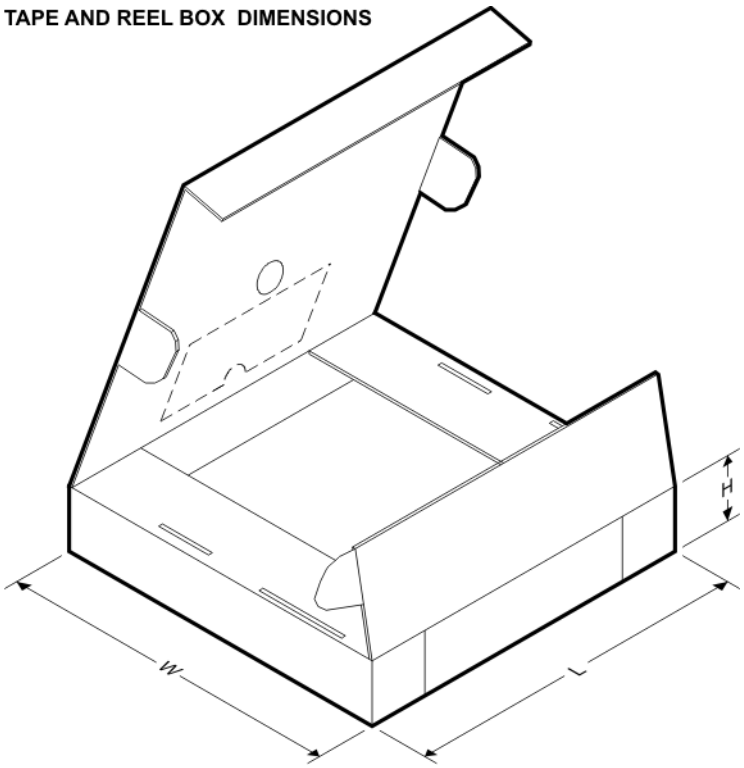
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3201AQDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3202AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

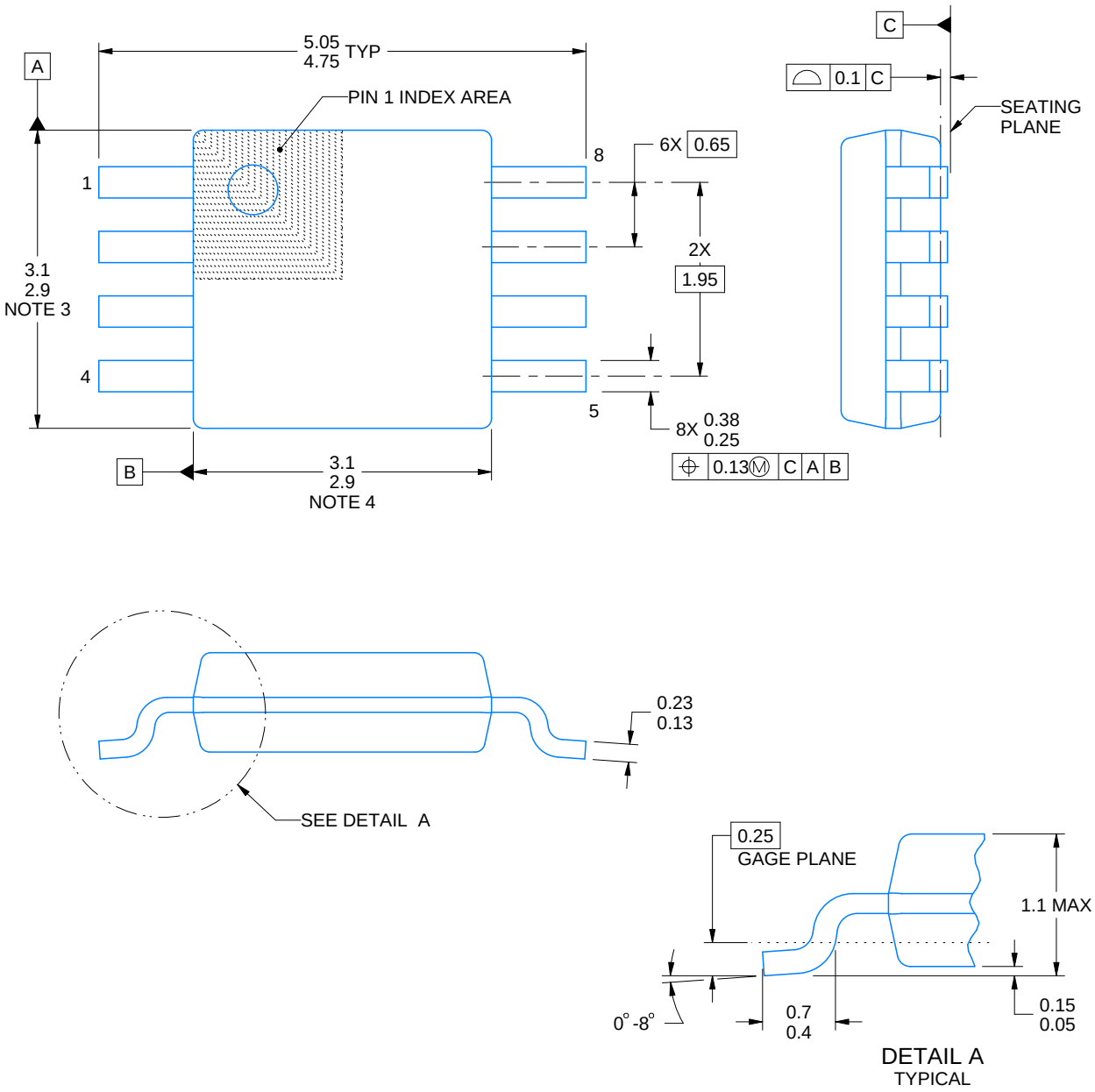
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3201AQDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
TLV3202AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

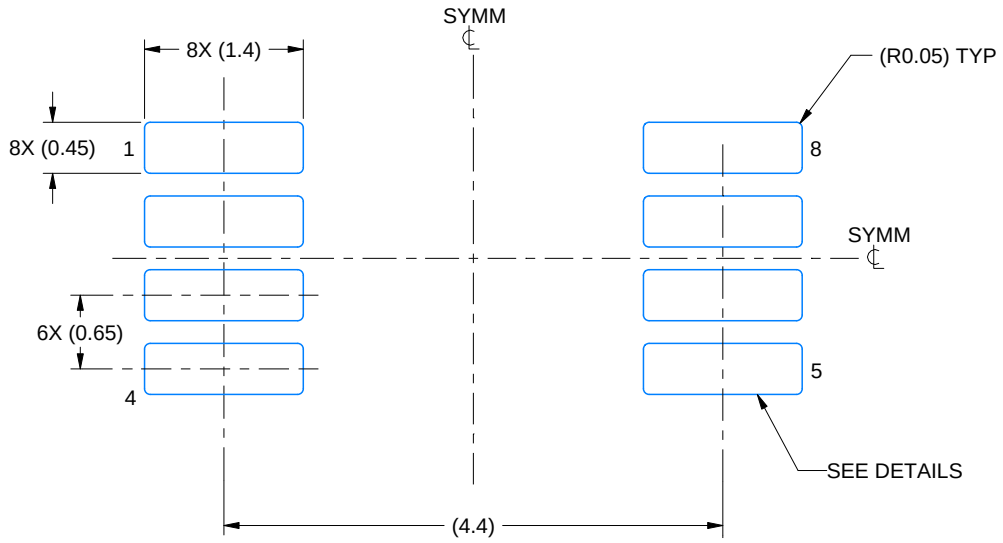
SMALL OUTLINE PACKAGE



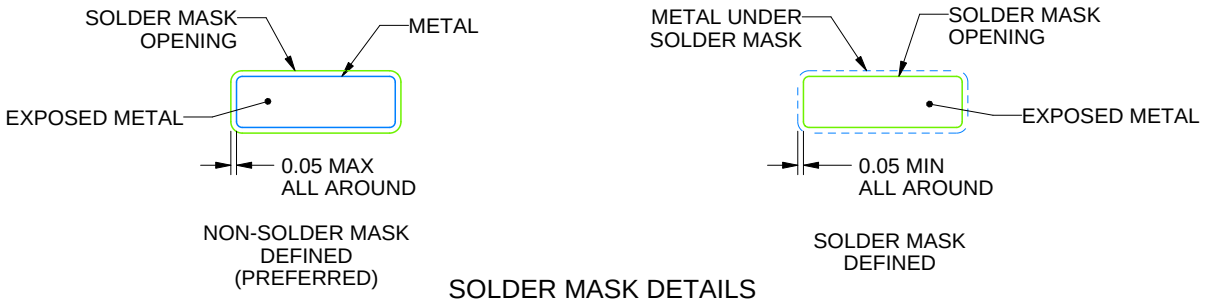
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

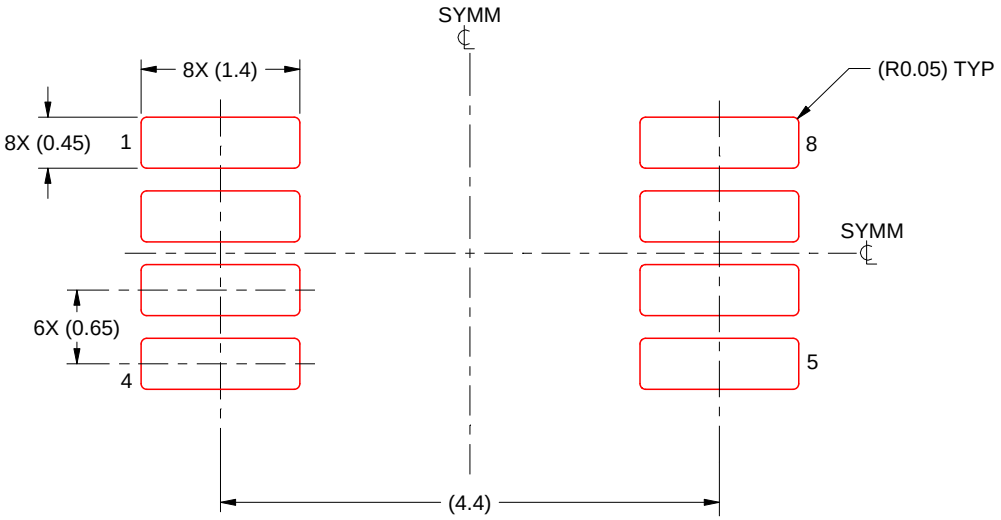


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

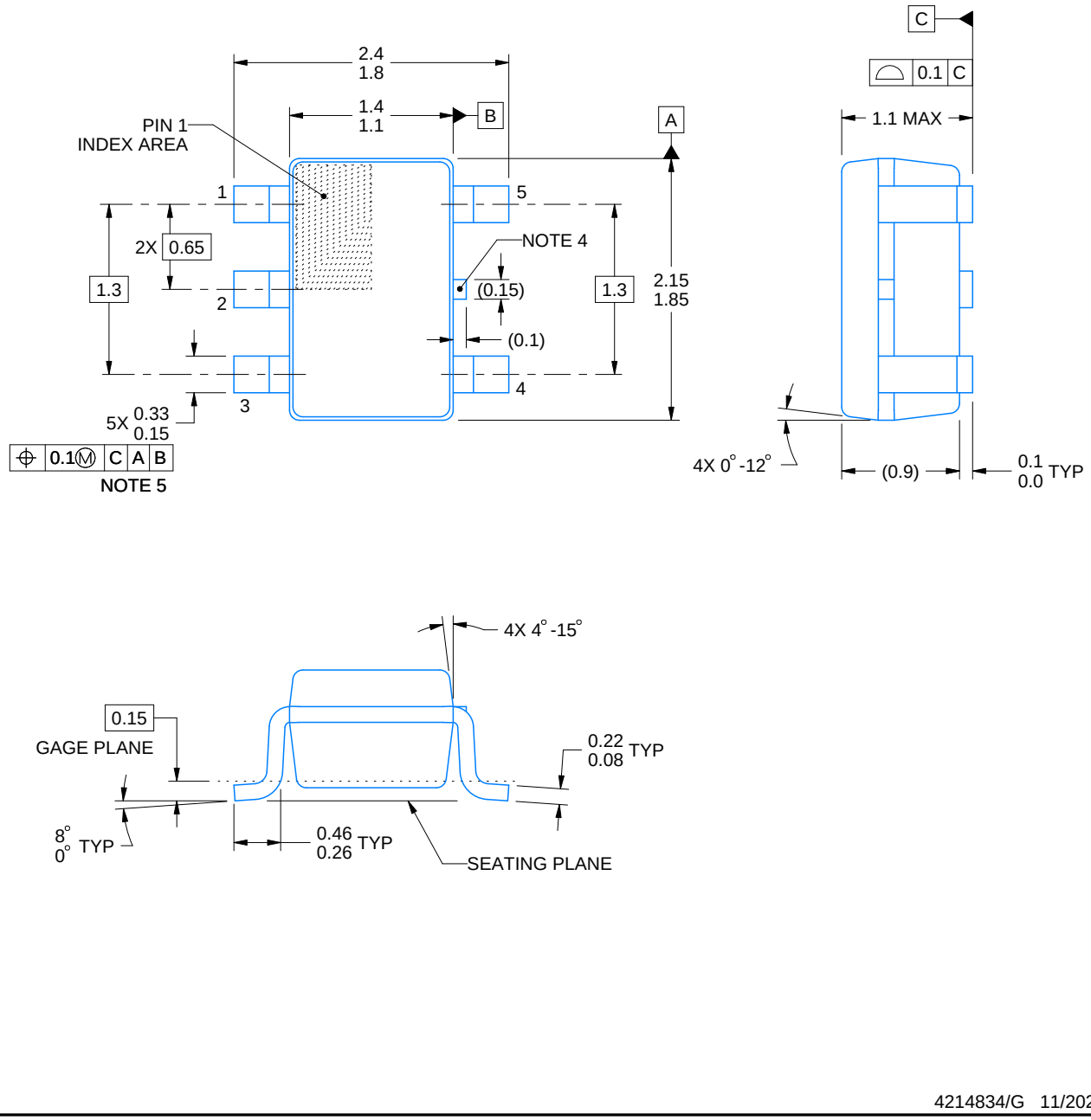
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

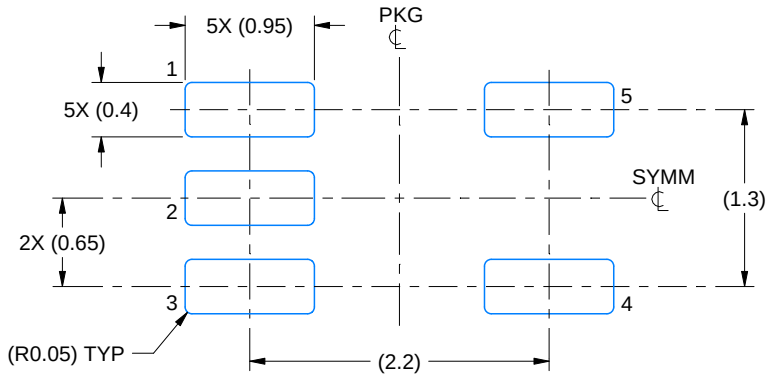
SMALL OUTLINE TRANSISTOR



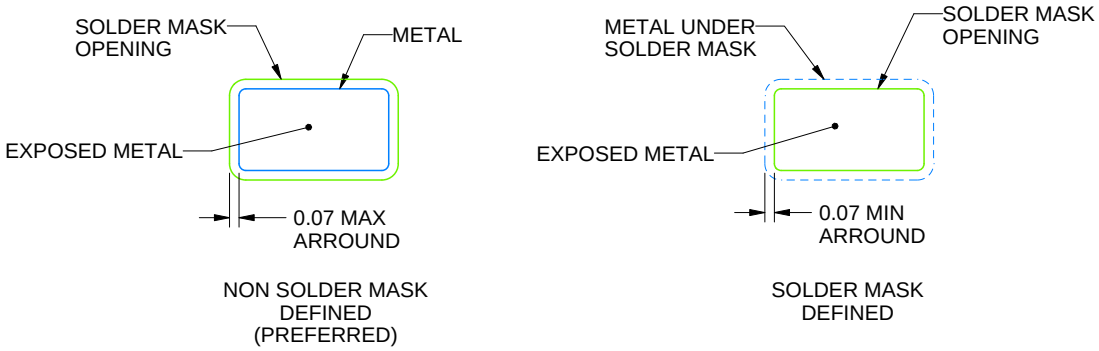
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

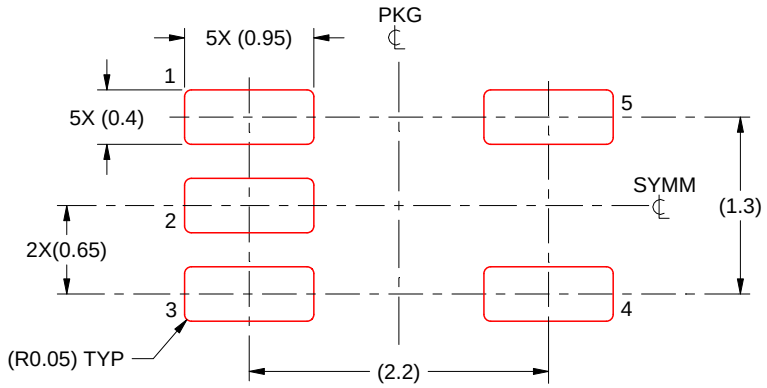


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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