

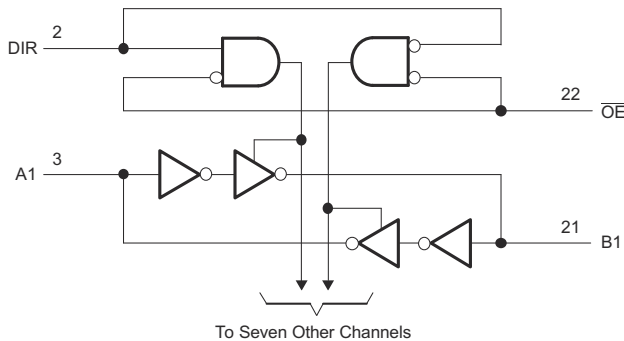
SN74LVCH8T245 具有可配置电平转换、电压转换和三态输出的 8 位双电源总线收发器

1 特性

- 控制输入 (DIR 和 $\overline{OE}$) V_{IH} 和 V_{IL} 电平以 V_{CCA} 为基准
- 总线保持数据输入消除了对外部上拉或下拉电阻器的需求
- V_{CC} 隔离
- 完全可配置的双轨设计
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 100mA, 符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求

2 应用

- 个人电子产品
- 工业
- 企业
- 电信



逻辑图 (正逻辑)

3 说明

SN74LVCH8T245 是一款采用两个独立可配置电源轨的 8 位同相总线收发器。A 端口设计用于跟踪 V_{CCA} , 该端口可接受 1.65V 至 5.5V 范围内的任何电源电压。B 端口设计用于跟踪 V_{CCB} , 该端口也可接受 1.65V 至 5.5V 范围内的任何电源电压。这样可实现 1.8V、2.5V、3.3V 和 5.5V 电压节点之间进行通用低压双向转换。

SN74LVCH8T245 旨在实现两条数据总线间的异步通信。方向控制 (DIR) 输入和输出使能 ($\overline{OE}$) 输入的逻辑电平会激活 B 端口输出或 A 端口输出, 或者将两个输出端口都置于高阻抗状态。当 B 端口输出被激活时, 此器件将数据从 A 总线发送到 B 总线, 而当 A 端口输出被激活时, 此器件将数据从 B 总线发送到 A 总线。A 端口和 B 端口上的输入电路始终处于运行状态。

有源总线保持电路会将未使用或未驱动的输入保持在有效逻辑状态。不建议在总线保持电路上使用上拉或下拉电阻器。该器件完全符合使用 I_{off} 的部分断电应用的规范要求。 I_{off} 电路禁用输出, 从而可防止破坏性电流从该器件回流。 V_{CC} 隔离特性可确保 V_{CCA} 或 V_{CCB} 接地时, 输出都处于高阻抗状态。为了确保加电或断电期间呈高阻态, $\overline{OE}$ 应通过一个上拉电阻器被连接至 V_{CCA} ; 该电阻器的最小值由驱动器的电流吸入能力来决定。

SN74LVCH8T245 旨在使控制引脚 (DIR 和 $\overline{OE}$) 以 V_{CCA} 为基准。

封装信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
SN74LVCH8T245	DB (SSOP , 24)	8.65mm × 3.90mm
	DGV (TVSOP , 24)	5.00mm × 4.40mm
	PW (TSSOP , 24)	7.80mm × 4.40mm
	RHL (VQFN , 24)	5.50mm × 3.50mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (January 2016) to Revision C (December 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Updated thermals for PW package.....	5
• Removed the <i>Supports High-Speed Translation</i> and added the <i>Balanced High-Drive CMOS Push-Pull Outputs</i> section.....	13
Changes from Revision A (February 2007) to Revision B (January 2016)	Page
• 添加了 <i>ESD</i> 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1

5 Pin Configuration and Functions

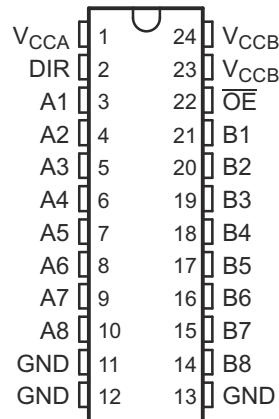


图 5-1. DB, DGV, or PW Packages, 24-Pin SSOP, TVSOP, or TSSOP (Top View)

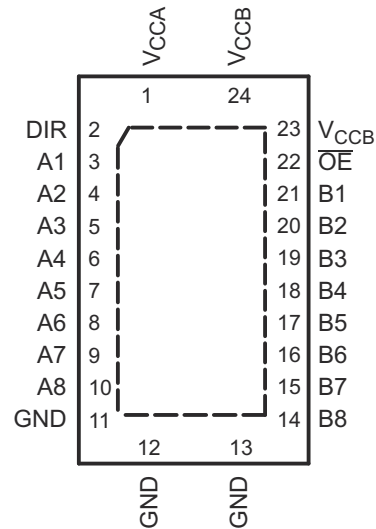


图 5-2. RHL Package, 24-Pin VQFN (Top View)

表 5-1. Pin Functions

PIN			TYPE ⁽¹⁾	DESCRIPTION
NAME	SSOP, TVSOP, TSSOP	VQFN		
A1	3	3	I/O	Input/output A1. Referenced to V _{CCA} .
A2	4	4	I/O	Input/output A2. Referenced to V _{CCA} .
A3	5	5	I/O	Input/output A3. Referenced to V _{CCA} .
A4	6	6	I/O	Input/output A4. Referenced to V _{CCA} .
A5	7	7	I/O	Input/output A5. Referenced to V _{CCA} .
A6	8	8	I/O	Input/output A6. Referenced to V _{CCA} .
A7	9	9	I/O	Input/output A7. Referenced to V _{CCA} .
A8	10	10	I/O	Input/output A8. Referenced to V _{CCA} .
B1	21	21	I/O	Input/output B1. Referenced to V _{CCB} .
B2	20	20	I/O	Input/output B2. Referenced to V _{CCB} .
B3	19	19	I/O	Input/output B3. Referenced to V _{CCB} .
B4	18	18	I/O	Input/output B4. Referenced to V _{CCB} .
B5	17	17	I/O	Input/output B5. Referenced to V _{CCB} .
B6	16	16	I/O	Input/output B6. Referenced to V _{CCB} .
B7	15	15	I/O	Input/output B7. Referenced to V _{CCB} .
B8	14	14	I/O	Input/output B8. Referenced to V _{CCB} .
DIR	2	2	I	Direction-control signal. Referenced to V _{CCA} .
OE	22	22	I	3-state output-mode enables. Pull OE high to place all outputs in 3-state mode. Referenced to V _{CCA} .
V _{CCA}	1	1	—	A-port supply voltage. 1.65 V ≤ V _{CCA} ≤ 5.5 V
V _{CCB}	23, 24	23, 24	—	B-port supply voltage. 1.65 V ≤ V _{CCA} ≤ 5.5 V
GND	11, 12, 13	11, 12, 13	—	Ground

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage	V_{CCA} and V_{CCB}	- 0.5	6.5	V
Input voltage ⁽²⁾	I/O ports (A port)	- 0.5	6.5	V
	I/O ports (B port)	- 0.5	6.5	
	Control inputs	- 0.5	6.5	
Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	A port	- 0.5	6.5	V
	B port	- 0.5	6.5	
Voltage range applied to any output in the high or low state ^{(2) (3)}	A port	- 0.5	$V_{CCA} + 0.5$	V
	B port	- 0.5	$V_{CCB} + 0.5$	
Input clamp current	$V_I < 0$		- 50	mA
Output clamp current	$V_O < 0$		- 50	mA
Continuous output current, I_O			±50	mA
Continuous through current	V_{CCA} , V_{CCB} , and GND		±100	mA
Junction temperature, T_J		- 40	150	°C
Storage temperature, T_{stg}		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [§ 6.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	
	Machine model (MM)	±200	

- (1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		1.65	5.5	V
V_{CCB}			1.65	5.5	
V_{IH} High-level input voltage ⁽¹⁾	Data inputs ⁽⁴⁾	$V_{CCI} = 1.65 \text{ V to } 4.5 \text{ V}$	$V_{CCI} \times 0.65$		V
		$V_{CCI} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
		$V_{CCI} = 3 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CCI} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CCI} \times 0.7$		
V_{IL} Low-level input voltage ⁽¹⁾	Data inputs ⁽⁴⁾	$V_{CCI} = 1.65 \text{ V to } 4.5 \text{ V}$	$V_{CCI} \times 0.35$		V
		$V_{CCI} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7		
		$V_{CCI} = 3 \text{ V to } 3.6 \text{ V}$	0.8		
		$V_{CCI} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CCI} \times 0.3$		

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

			MIN	MAX	UNIT
V _{IH}	High-level input voltage	Control inputs (referenced to V _{CCA}) ⁽⁵⁾	V _{CCI} = 1.65 V to 4.5 V	V _{CCA} × 0.65	V
			V _{CCI} = 2.3 V to 2.7 V	1.7	
			V _{CCI} = 3 V to 3.6 V	2	
			V _{CCI} = 4.5 V to 5.5 V	V _{CCA} × 0.7	
V _{IL}	Low-level input voltage	Control inputs (referenced to V _{CCA}) ⁽⁵⁾	V _{CCI} = 1.65 V to 4.5 V	V _{CCA} × 0.35	V
			V _{CCI} = 2.3 V to 2.7 V	0.7	
			V _{CCI} = 3 V to 3.6 V	0.8	
			V _{CCI} = 4.5 V to 5.5 V	V _{CCA} × 0.3	
V _I	Input voltage	Control inputs ⁽³⁾	0	5.5	V
V _{I/O}	Input/output voltage ⁽²⁾	Active state	0	V _{CCO}	V
		3-State	0	5.5	
I _{OH}	High-level output current		V _{CCO} = 1.65 V to 4.5 V	- 4	mA
			V _{CCO} = 2.3 V to 2.7 V	- 8	
			V _{CCO} = 3 V to 3.6 V	- 24	
			V _{CCO} = 4.5 V to 5.5 V	- 32	
I _{OL}	Low-level output current		V _{CCO} = 1.65 V to 4.5 V	4	mA
			V _{CCO} = 2.3 V to 2.7 V	8	
			V _{CCO} = 3 V to 3.6 V	24	
			V _{CCO} = 4.5 V to 5.5 V	32	
Δt / Δv	Input transition rise or fall rate	Data inputs	V _{CCI} = 1.65 V to 4.5 V	20	ns/V
			V _{CCI} = 2.3 V to 2.7 V	20	
			V _{CCI} = 3 V to 3.6 V	10	
			V _{CCI} = 4.5 V to 5.5 V	5	
T _A	Operating free-air temperature		- 40	85	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) All unused control inputs of the device must be held at V_{CCA} or GND to ensure proper device operation and minimize power consumption. See *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} (max) = V_{CCI} × 0.3 V.

(5) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} (max) = V_{CCA} × 0.3 V.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVCH8T245				UNIT
		DB (SSOP)	DGV (TVSOP)	PW (TSSOP)	RHL (VQFN)	
		24 PINS	24 PINS	24 PINS	24 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	88.5	91.1	100.6	37.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	48.7	23.7	44.7	38.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	44.1	44.5	55.8	15.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	12.8	0.6	6.8	0.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	43.6	44.1	55.4	15.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	—	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

All typical limits apply over $T_A = 25^\circ\text{C}$, and all maximum and minimum limits apply over $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted).^{(1) (2)}

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage ⁽¹⁾	$I_{OH} = -100\ \mu\text{A}$, $V_I = V_{IH}$	$V_{CCA} = V_{CCB} = 1.65\text{ V to }4.5\text{ V}$	$V_{CCO} = 0.1$			V
		$I_{OH} = -4\text{ mA}$, $V_I = V_{IH}$	$V_{CCA} = V_{CCB} = 1.65\text{ V}$	1.2			
		$I_{OH} = -8\text{ mA}$, $V_I = V_{IH}$	$V_{CCA} = V_{CCB} = 2.3\text{ V}$	1.9			
		$I_{OH} = -24\text{ mA}$, $V_I = V_{IH}$	$V_{CCA} = V_{CCB} = 3\text{ V}$	2.4			
		$I_{OH} = -32\text{ mA}$, $V_I = V_{IH}$	$V_{CCA} = V_{CCB} = 4.5\text{ V}$	3.8			
V_{OL}	Low-level output voltage	$I_{OL} = 100\ \mu\text{A}$, $V_I = V_{IL}$	$V_{CCA} = V_{CCB} = 1.65\text{ V to }4.5\text{ V}$			0.1	V
		$I_{OL} = 4\text{ mA}$, $V_I = V_{IL}$	$V_{CCA} = V_{CCB} = 1.65\text{ V}$			0.45	
		$I_{OL} = 8\text{ mA}$, $V_I = V_{IL}$	$V_{CCA} = V_{CCB} = 2.3\text{ V}$			0.3	
		$I_{OL} = 24\text{ mA}$, $V_I = V_{IL}$	$V_{CCA} = V_{CCB} = 3\text{ V}$			0.55	
		$I_{OL} = 32\text{ mA}$, $V_I = V_{IL}$	$V_{CCA} = V_{CCB} = 4.5\text{ V}$			0.55	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	$V_{CCA} = V_{CCB} = 1.65\text{ V to }4.5\text{ V}$		± 0.5	± 2	μA
I_{BHL} ⁽³⁾	Bus-hold low sustaining current	$V_I = 0.58\text{ V}$	$V_{CCA} = V_{CCB} = 1.65\text{ V}$		15		μA
		$V_I = 0.7\text{ V}$	$V_{CCA} = V_{CCB} = 2.3\text{ V}$		45		
		$V_I = 0.8\text{ V}$	$V_{CCA} = V_{CCB} = 3\text{ V}$		75		
		$V_I = 1.35\text{ V}$	$V_{CCA} = V_{CCB} = 4.5\text{ V}$		100		
I_{BHH} ⁽⁴⁾	Bus-hold high sustaining current	$V_I = 1.07\text{ V}$	$V_{CCA} = V_{CCB} = 1.65\text{ V}$	-15			μA
		$V_I = 1.7\text{ V}$	$V_{CCA} = V_{CCB} = 2.3\text{ V}$	-45			
		$V_I = 2\text{ V}$	$V_{CCA} = V_{CCB} = 3\text{ V}$	-75			
		$V_I = 3.15\text{ V}$	$V_{CCA} = V_{CCB} = 4.5\text{ V}$	-100			
I_{BHLO} ⁽⁵⁾	Bus-hold low overdrive current	$V_I = 0\text{ to }V_{CC}$	$V_{CCA} = V_{CCB} = 1.95\text{ V}$		200		μA
			$V_{CCA} = V_{CCB} = 2.7\text{ V}$		300		
			$V_{CCA} = V_{CCB} = 3.6\text{ V}$		500		
			$V_{CCA} = V_{CCB} = 5.5\text{ V}$		900		
I_{BHHO} ⁽⁶⁾	Bus-hold high overdrive current	$V_I = 0\text{ to }V_{CC}$	$V_{CCA} = V_{CCB} = 1.95\text{ V}$	-200			μA
			$V_{CCA} = V_{CCB} = 2.7\text{ V}$	-300			
			$V_{CCA} = V_{CCB} = 3.6\text{ V}$	-500			
			$V_{CCA} = V_{CCB} = 5.5\text{ V}$	-900			
I_{off}	Input and output power-off leakage current	V_I or $V_O = 0\text{ to }5.5\text{ V}$	$V_{CCA} = 0\text{ V}$, $V_{CCB} = 0\text{ to }5.5\text{ V}$	A Port	± 0.5	± 2	μA
			$V_{CCA} = 0\text{ to }5.5\text{ V}$, $V_{CCB} = 0\text{ V}$	B Port	± 0.5	± 2	
I_{OZ}	Off-state output current	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	$\overline{OE} = V_{IH}$	$V_{CCA} = V_{CCB} = 1.65\text{ V to }4.5\text{ V}$	A Port, B Port	± 2	μA
			$\overline{OE} = X$	$V_{CCA} = 0\text{ V}$, $V_{CCB} = 5.5\text{ V}$	B Port	± 2	
			$\overline{OE} = X$	$V_{CCA} = 5.5\text{ V}$, $V_{CCB} = 0\text{ V}$	A Port	± 2	
I_{CCA}	Supply current A port	$V_I = V_{CCI}$ or GND, $I_O = 0$	$V_{CCA} = V_{CCB} = 1.65\text{ V to }4.5\text{ V}$			20	μA
			$V_{CCA} = 5\text{ V}$, $V_{CCB} = 0\text{ V}$			20	
			$V_{CCA} = 0\text{ V}$, $V_{CCB} = 5\text{ V}$			-2	
I_{CCB}	Supply current B port	$V_I = V_{CCI}$ or GND, $I_O = 0$	$V_{CCA} = V_{CCB} = 1.65\text{ V to }4.5\text{ V}$			20	μA
			$V_{CCA} = 5\text{ V}$, $V_{CCB} = 0\text{ V}$			-2	
			$V_{CCA} = 0\text{ V}$, $V_{CCB} = 5\text{ V}$			20	

6.5 Electrical Characteristics (continued)

All typical limits apply over $T_A = 25^\circ\text{C}$, and all maximum and minimum limits apply over $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted).^{(1) (2)}

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Combined supply current	$V_I = V_{CCI}$ or GND, $I_O = 0$	$V_{CCA} = V_{CCB} = 1.65\text{ V to }4.5\text{ V}$			30	μA
ΔI_{CCA} Supply-current change DIR	DIR at $V_{CCA} - 0.6\text{ V}$, B port = open, A port at V_{CCA} or GND	$V_{CCA} = V_{CCB} = 3\text{ to }5.5\text{ V}$			50	μA
C_i Input capacitance control inputs	$V_I = V_{CCA}$ or GND	$V_{CCA} = V_{CCB} = 3.3\text{ V}$		4	5	pF
C_{io} Input and output capacitance A or B port	$V_O = V_{CCA/B}$ or GND	$V_{CCA} = V_{CCB} = 3.3\text{ V}$		8.5	10	pF

- (1) V_{CCO} is the V_{CC} associated with the output port.
- (2) V_{CCI} is the V_{CC} associated with the input port.
- (3) The bus-hold circuit can sink at least the minimum low sustaining current at the V_{IL} maximum. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} maximum.
- (4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
- (5) An external driver must source at least I_{BHLO} to switch this node from low to high.
- (6) An external driver must sink at least I_{BHLO} to switch this node from high to low.

6.6 Switching Characteristics: $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.7	21.9	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.3	9.2	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	7.4	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.4	7.1	
t_{PLH}, t_{PHL}	B	A	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.9	23.8	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.8	23.6	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.7	23.4	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.7	23.4	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.5	29.6	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.5	29.4	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1.5	29.3	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1.4	29.2	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	2.4	32.2	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.9	13.1	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1.7	12	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1.3	10.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.4	24	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.4	23.8	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.4	23.7	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.4	23.7	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.8	32	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.5	16	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1.2	12.6	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.9	10.8	

6.7 Switching Characteristics: $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} , t_{PHL}	A	B	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.5	21.4	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.2	9	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.8	6.2	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.6	4.8	
t_{PLH} , t_{PHL}	B	A	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.2	9.3	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1	9.1	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	8.9	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.9	8.8	
t_{PHZ} , t_{PLZ}	$\overline{OE}$	A	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.4	9	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.4	9	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1.4	9	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1.4	9	
t_{PHZ} , t_{PLZ}	$\overline{OE}$	B	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	2.3	29.6	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.8	11	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1.7	9.3	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.9	6.9	
t_{PZH} , t_{PZL}	$\overline{OE}$	A	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1	10.9	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1	10.9	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	10.9	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	10.9	
t_{PZH} , t_{PZL}	$\overline{OE}$	B	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.7	28.2	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.5	12.9	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1.2	9.4	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	1	6.9	

6.8 Switching Characteristics: $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} , t_{PHL}	A	B	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1.5	21.2	ns
			$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1.1	8.8	
			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.8	6.2	
			$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$	0.5	4.4	
t_{PLH} , t_{PHL}	B	A	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	0.8	7.2	ns
			$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$	0.8	6.2	
			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.7	6.1	
			$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$	0.6	6	
t_{PHZ} , t_{PLZ}	$\overline{OE}$	A	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1.6	8.2	ns
			$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1.6	8.2	
			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.6	8.2	
			$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$	1.6	8.2	
t_{PHZ} , t_{PLZ}	$\overline{OE}$	B	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	2.1	29	ns
			$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1.7	10.3	
			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.5	8.6	
			$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$	0.8	6.3	
t_{PZH} , t_{PZL}	$\overline{OE}$	A	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	0.8	8.1	ns
			$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$	0.8	8.1	
			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.8	8.1	
			$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$	0.8	8.1	
t_{PZH} , t_{PZL}	$\overline{OE}$	B	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1.8	27.7	ns
			$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$	1.4	12.4	
			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.1	8.5	
			$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$	0.9	6.4	

6.9 Switching Characteristics: $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} , t_{PHL}	A	B	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.5	21.4	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1	8.8	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.7	6	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.4	4.2	
t_{PLH} , t_{PHL}	B	A	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.7	7	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.4	4.8	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.3	4.5	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.3	4.3	
t_{PHZ} , t_{PLZ}	$\overline{OE}$	A	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.3	5.4	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.3	5.4	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.3	5.4	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.3	5.4	
t_{PHZ} , t_{PLZ}	$\overline{OE}$	B	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	2	28.7	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.6	9.7	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1.4	8	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.7	5.7	
t_{PZH} , t_{PZL}	$\overline{OE}$	A	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	0.7	6.4	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	0.7	6.4	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	0.7	6.4	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.7	6.4	
t_{PZH} , t_{PZL}	$\overline{OE}$	B	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	1.5	27.6	ns
			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	1.3	11.4	
			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	1	8.1	
			$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$	0.9	6.5	

6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER ⁽¹⁾		TEST CONDITIONS		TYP	UNIT
C_{pdA} ⁽²⁾	A-port input, B-port output	$C_L = 0$, $f = 10\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	$V_{CCA} = V_{CCB} = 1.8\text{ V}$	2	pF
			$V_{CCA} = V_{CCB} = 2.5\text{ V}$	2	
			$V_{CCA} = V_{CCB} = 3.3\text{ V}$	2	
			$V_{CCA} = V_{CCB} = 5\text{ V}$	3	
	B-port input, A-port output	$C_L = 0$, $f = 10\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	$V_{CCA} = V_{CCB} = 1.8\text{ V}$	12	
			$V_{CCA} = V_{CCB} = 2.5\text{ V}$	13	
			$V_{CCA} = V_{CCB} = 3.3\text{ V}$	13	
			$V_{CCA} = V_{CCB} = 5\text{ V}$	16	
C_{pdB} ⁽²⁾	A-port input, B-port output	$C_L = 0$, $f = 10\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	$V_{CCA} = V_{CCB} = 1.8\text{ V}$	13	pF
			$V_{CCA} = V_{CCB} = 2.5\text{ V}$	13	
			$V_{CCA} = V_{CCB} = 3.3\text{ V}$	14	
			$V_{CCA} = V_{CCB} = 5\text{ V}$	16	
	B-port input, A-port output	$C_L = 0$, $f = 10\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	$V_{CCA} = V_{CCB} = 1.8\text{ V}$	2	
			$V_{CCA} = V_{CCB} = 2.5\text{ V}$	2	
			$V_{CCA} = V_{CCB} = 3.3\text{ V}$	2	
			$V_{CCA} = V_{CCB} = 5\text{ V}$	3	

(1) See *CMOS Power Consumption and Cpd Calculation*, [SCAA035](#).

(2) Power dissipation capacitance per transceiver.

6.11 Typical Characteristics

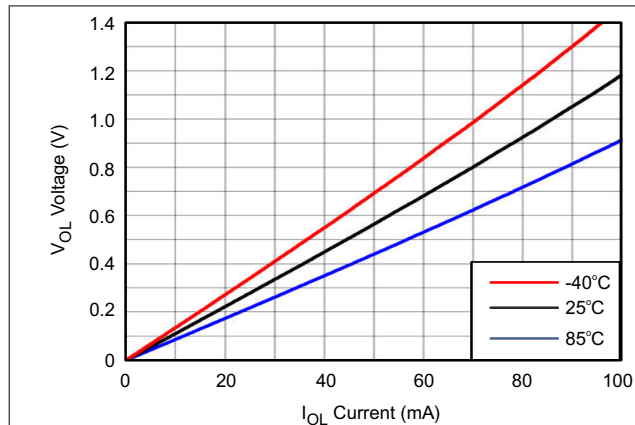


图 6-1. Voltage vs Current

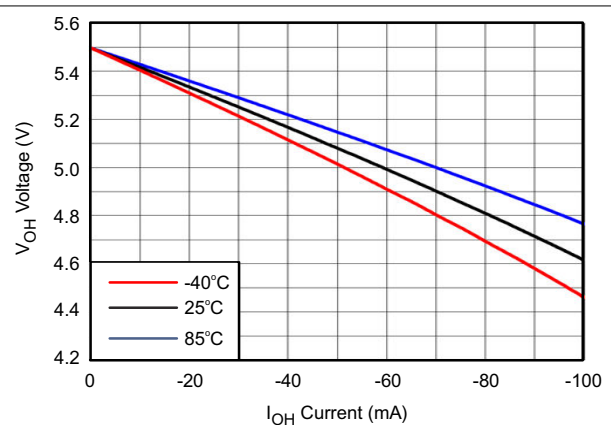
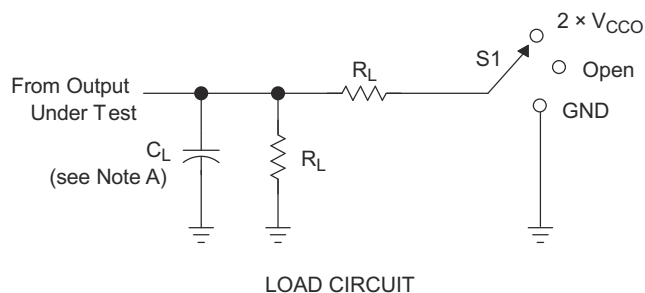


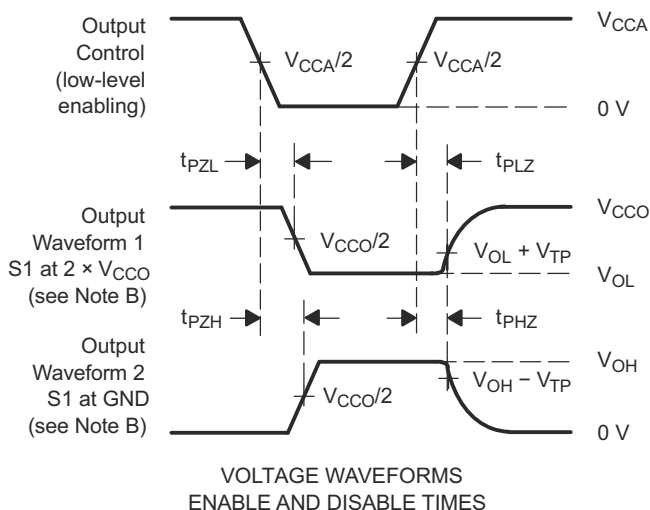
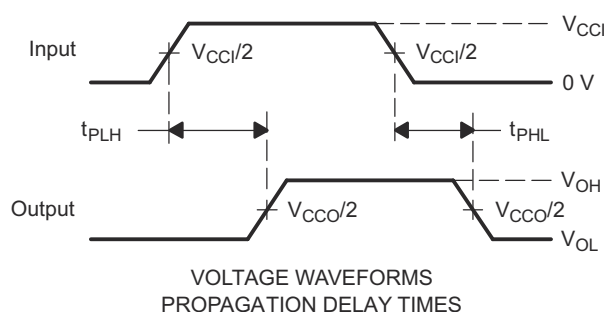
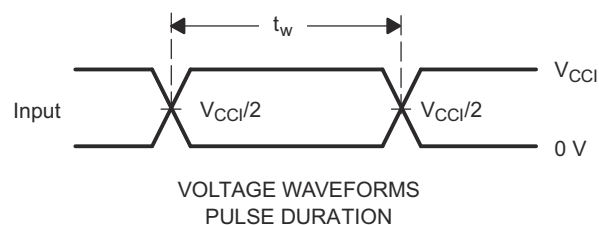
图 6-2. Voltage vs Current

7 Parameter Measurement Information



V_{CCO}	C_L	R_L	V_{TP}
$1.8\text{ V} \pm 0.15\text{ V}$	15 pF	2 kW	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	15 pF	2 kW	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	15 pF	2 kW	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	15 pF	2 kW	0.3 V

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz, $Z_O = 50\ \Omega$, $dv/dt \geq 1\text{ V/ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. V_{CCI} is the V_{CC} associated with the input port.
 I. V_{CCO} is the V_{CC} associated with the output port.
 J. All parameters and waveforms are not applicable to all devices.

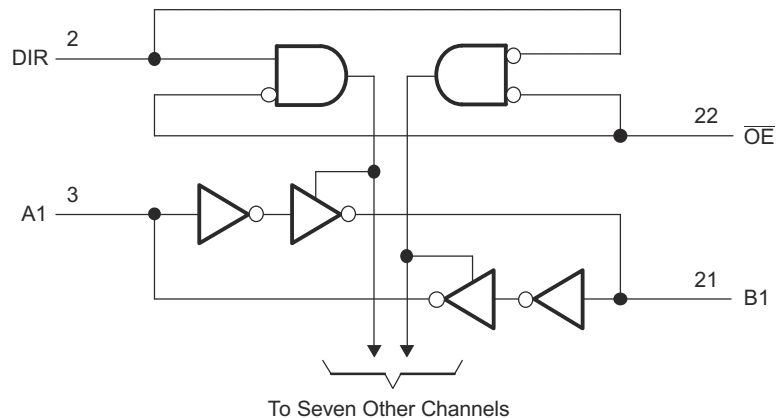
图 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVCH8T245 is an 8-bit, dual supply noninverting voltage level translator. Pins A1 through A4, and the control pins (DIR and $\overline{OE}$) are referenced to V_{CCA} , while pins B1 through B4 are referenced to V_{CCB} . Both the A port and B port can accept I/O voltages ranging from 1.65 V to 5.5 V. The high on DIR allows data transmission from Port A to Port B, and a low on DIR allows data transmission from Port B to Port A. For more information, see [AVC Logic Family Technology and Applications](#).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 1.65 V to 5.5 V, making the device suitable for translating between any of the voltage nodes: 1.8 V, 2.5 V, 3.3 V, and 5 V.

8.3.2 Partial-Power-Down Mode Operation

I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. This can occur in applications where subsections of a system are powered down (partial power down) to reduce power consumption. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Electrical Characteristics](#).

8.3.3 Active Bus Hold Circuitry

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state, which helps with board space savings and reduced component costs. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended as this eliminates the bus-hold feature.

8.3.4 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Two outputs can be connected together for 2X stronger output drive strength. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

8.3.5 V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND (or < 0.4 V), both ports will be in a high-impedance state (I_{OZ} shown in [Electrical Characteristics](#)). This prevents false logic levels from being presented to either bus.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74LVCH8T245.

表 8-1. Function Table (Each 8-Bit Section)

CONTROL INPUTS ⁽¹⁾		OUTPUT CIRCUITS		OPERATION
OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

备注

以下应用部分中的信息不属于 TI 器件规格的范围, TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计, 以确保系统功能。

The SN74LVCH8T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum output current can be up to 32 mA when device is powered by 5 V.

The diagram illustrates a level shifter circuit. On the left, a block labeled "1.8-V Controller" has a "GND" pin at the bottom and eight "Data" pins on the right. These data pins are connected to the input pins A1 through A8 of a central buffer IC labeled "SN74LVCH8T245". The buffer IC has two power pins at the top: "V_{CCA}" and "V_{CCB}". "V_{CCA}" is connected to a "1.8 V" supply rail, which also includes a pull-up resistor and a 0.1 μF capacitor to ground. "V_{CCB}" is connected to a "5 V" supply rail, which includes a pull-up resistor, a 0.1 μF capacitor, and a 1 μF capacitor to ground. The buffer IC also has a "DIR" pin (connected to the 1.8 V rail via a resistor) and an "OE" pin (connected to the 1.8 V rail via a resistor). The output pins B1 through B8 of the buffer are connected to the "Data" pins of a block on the right labeled "5-V System". This block also has a "GND" pin at the bottom. A common ground line runs along the bottom, connecting the GND pins of the controller, the buffer, and the system.

图 9-1. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETERS	VALUES
Input voltage	1.65 V to 5.5 V
Output voltage	1.65 V to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the SN74LVCH8T245 to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
 - Use the supply voltage of the device that the SN74LVCH8T245 is driving to determine the output voltage range.

9.2.2.1 Enable Times

Calculate the enable times for the SN74LVCH8T245 using 方程式 1, 方程式 2, 方程式 3, and 方程式 4:

$$t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)} \quad (1)$$

$$t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)} \quad (2)$$

$$t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)} \quad (3)$$

$$t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)} \quad (4)$$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the device initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

9.2.3 Application Curve

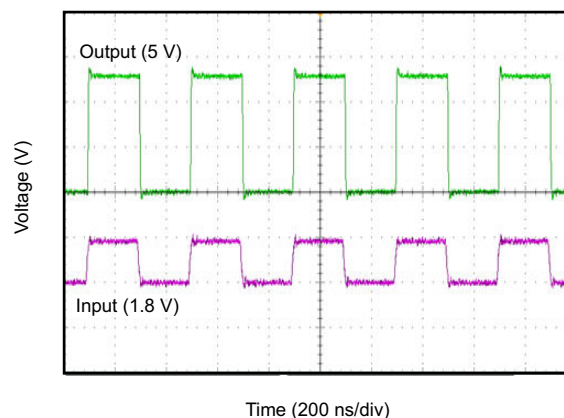


图 9-2. Translation Up (1.8 V to 5 V) at 2.5 MHz

10 Power Supply Recommendations

The output-enable ($\overline{OE}$) input circuit is designed so that it is supplied by V_{CCA} and when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

V_{CCA} or V_{CCB} can be powered up first. If the SN74LVCH8T245 is powered up in a permanently enabled state (for example $\overline{OE}$ is always kept low), pullup resistors are recommended at the input. This ensures proper, glitch-free, power-up. For more information, see [Designing with SN4LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters](#). In addition, the $\overline{OE}$ pin may be shorted to GND if the application does not require use of the high-impedance state at any time.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, TI recommends the following common printed-circuit board layout guidelines.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors helps adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

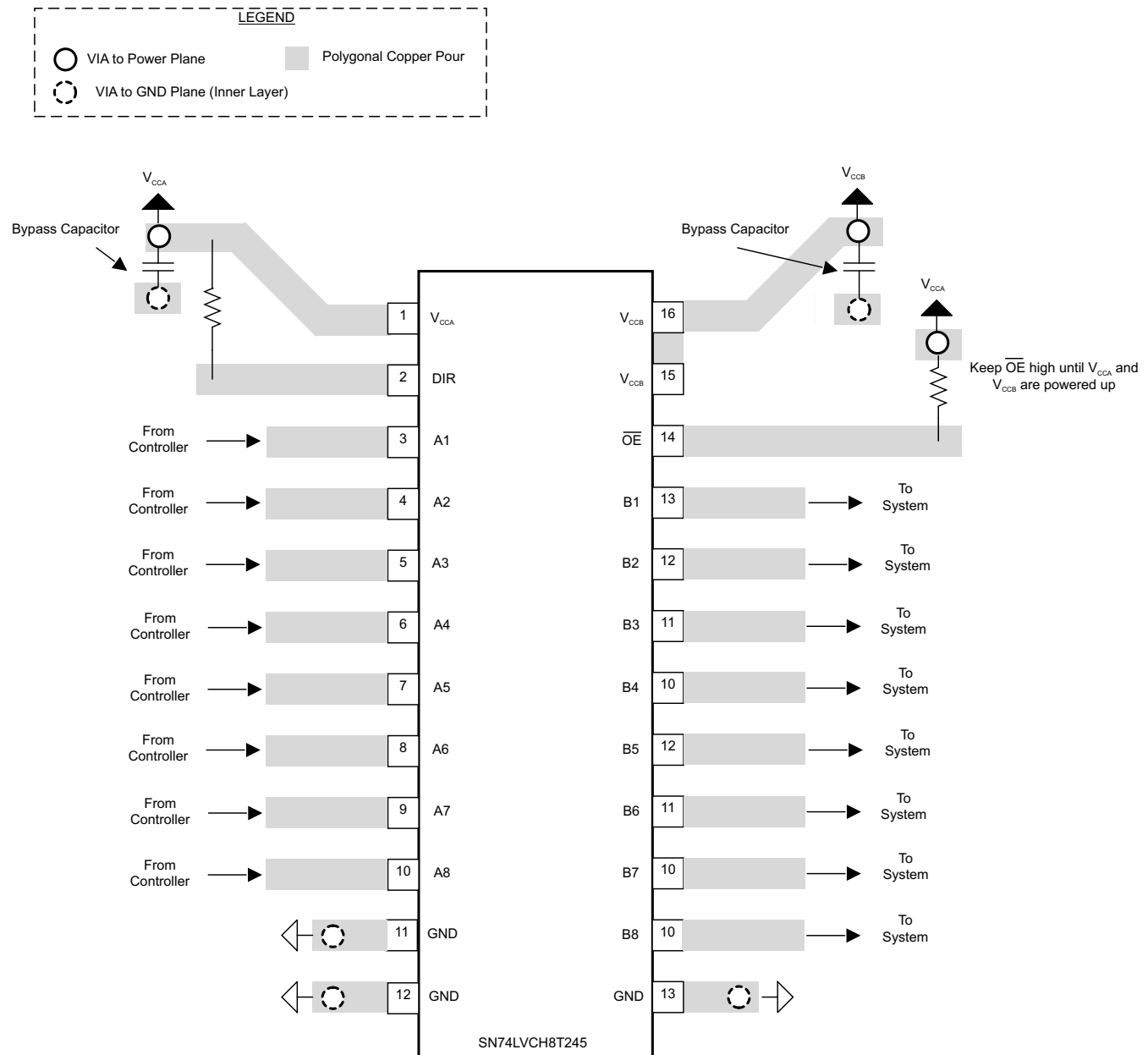


图 11-1. SN74LVCH8T245 Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters](#)
- Texas Instruments, [Bus-Hold Circuit](#)
- Texas Instruments, [AVC Logic Family Technology and Applications](#)
- Texas Instruments, [CMOS Power Consumption and Cpd Calculation](#)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVCH8T245DGVRG4	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
74LVCH8T245DGVRG4.B	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
74LVCH8T245RHRLRG4	Active	Production	VQFN (RHL) 24	1000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NJ245
74LVCH8T245RHRLRG4.B	Active	Production	VQFN (RHL) 24	1000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NJ245
SN74LVCH8T245DBR	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245DBR.B	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245DBRG4	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245DBRG4.B	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245DGVR	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245DGVR.B	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245PW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245PW.B	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245PWE4	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245PWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245PWR.A	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245PWRG4	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245PWRG4.A	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245
SN74LVCH8T245RHRLR	Active	Production	VQFN (RHL) 24	1000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NJ245
SN74LVCH8T245RHRLR.B	Active	Production	VQFN (RHL) 24	1000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NJ245

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

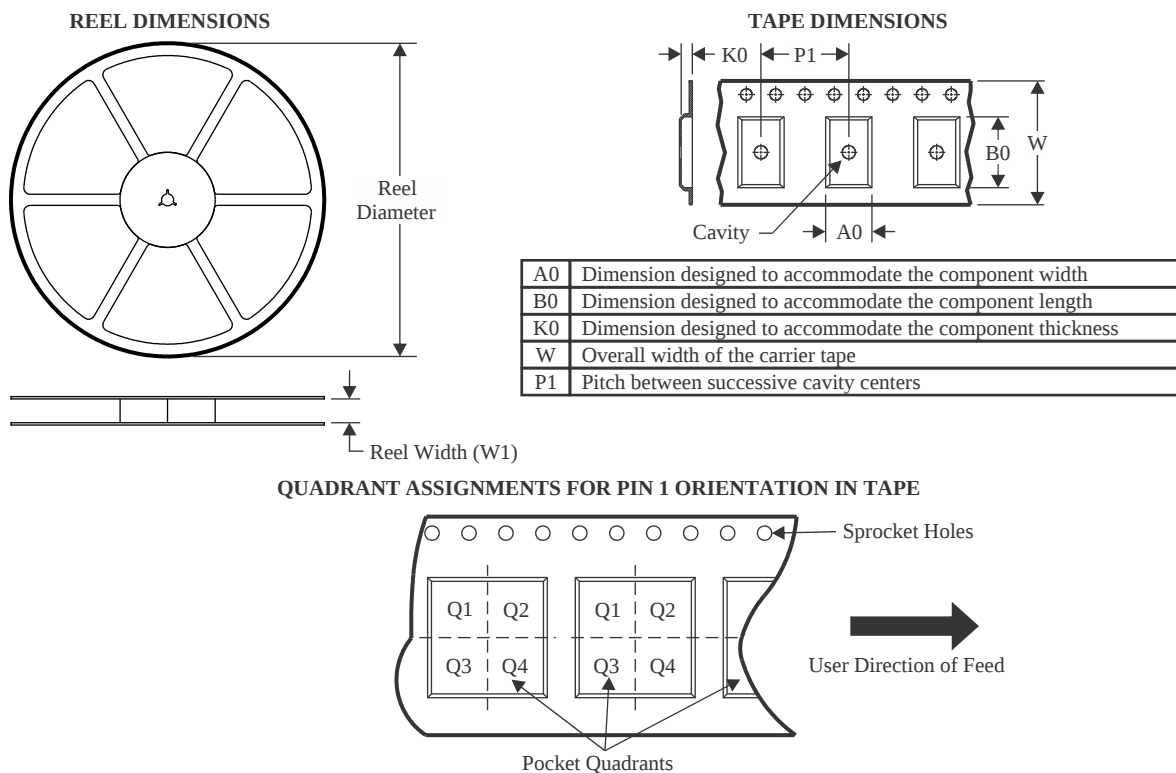
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVCH8T245DGVRG4	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
74LVCH8T245RHRLRG4	VQFN	RHL	24	1000	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
SN74LVCH8T245DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVCH8T245DBRG4	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVCH8T245DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVCH8T245PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCH8T245PWRG4	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCH8T245PWRG4	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCH8T245RHRLR	VQFN	RHL	24	1000	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

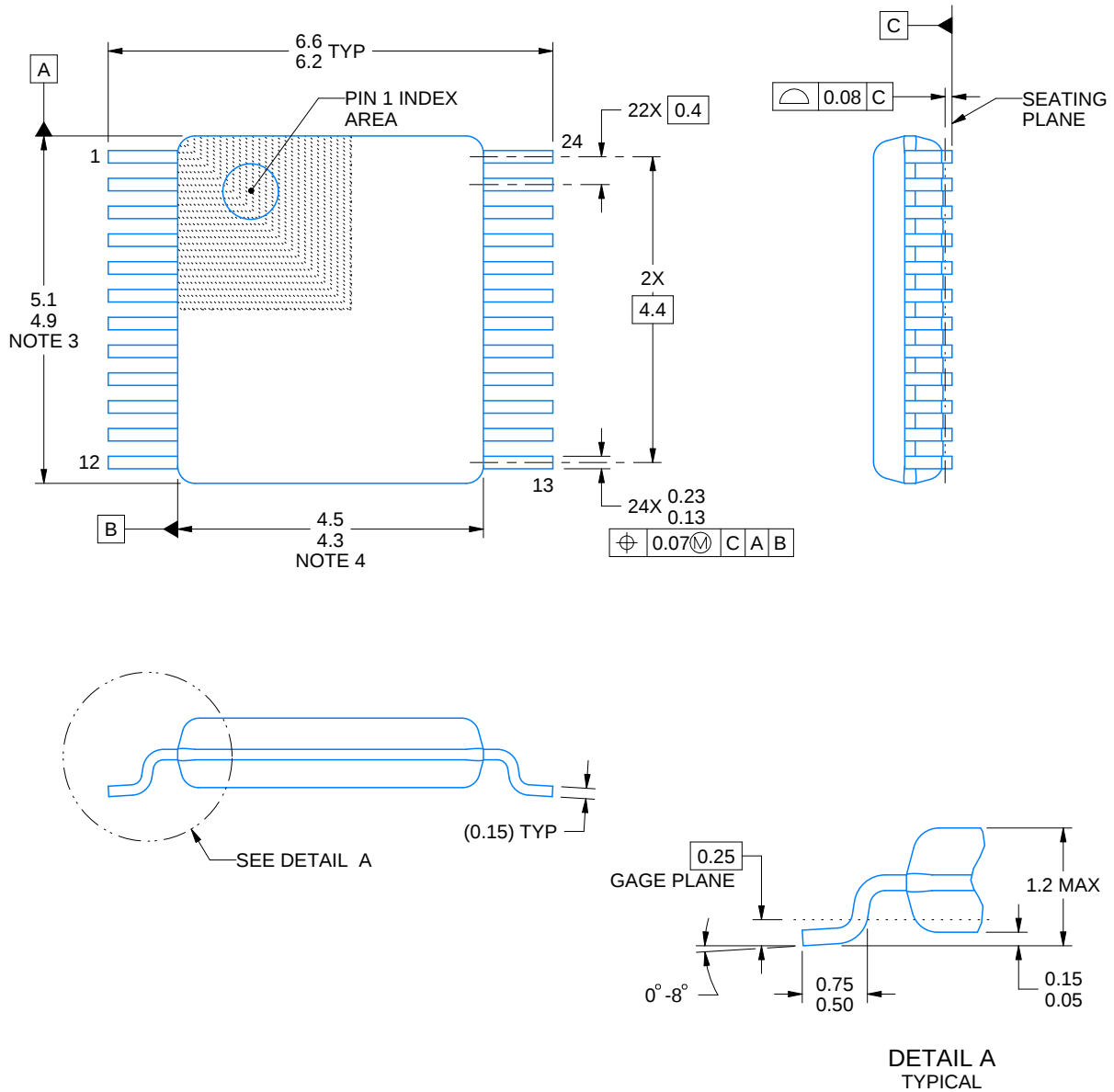
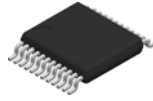
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVCH8T245DGVRG4	TVSOP	DGV	24	2000	356.0	356.0	35.0
74LVCH8T245RHLRG4	VQFN	RHL	24	1000	210.0	185.0	35.0
SN74LVCH8T245DBR	SSOP	DB	24	2000	356.0	356.0	35.0
SN74LVCH8T245DBRG4	SSOP	DB	24	2000	356.0	356.0	35.0
SN74LVCH8T245DGVR	TVSOP	DGV	24	2000	356.0	356.0	35.0
SN74LVCH8T245PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74LVCH8T245PWRG4	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74LVCH8T245PWRG4	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74LVCH8T245RHLR	VQFN	RHL	24	1000	213.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVCH8T245PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVCH8T245PW.B	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVCH8T245PWE4	PW	TSSOP	24	60	530	10.2	3600	3.5



4229221/A 12/2022

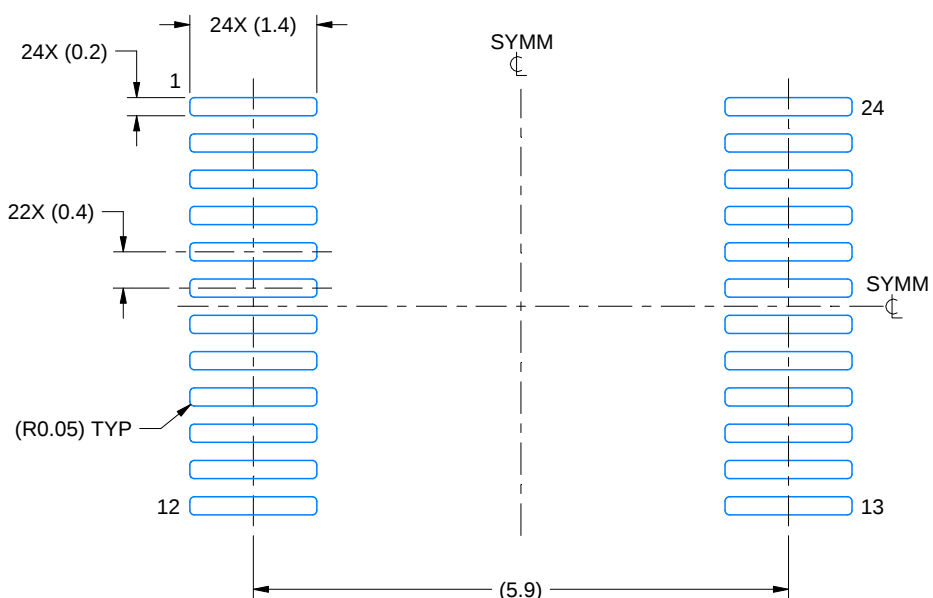
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

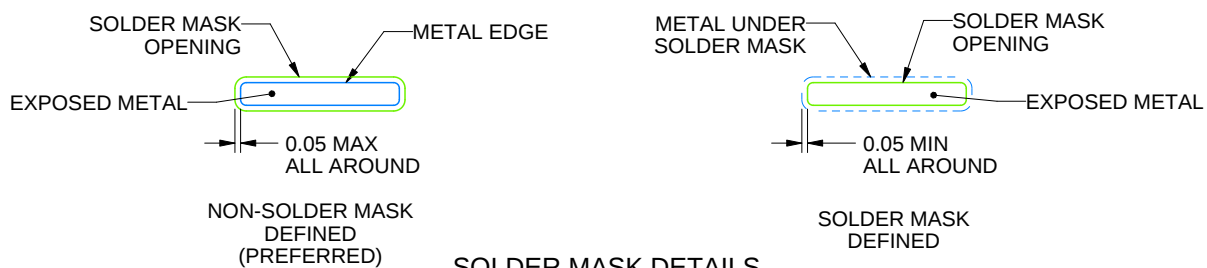
DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

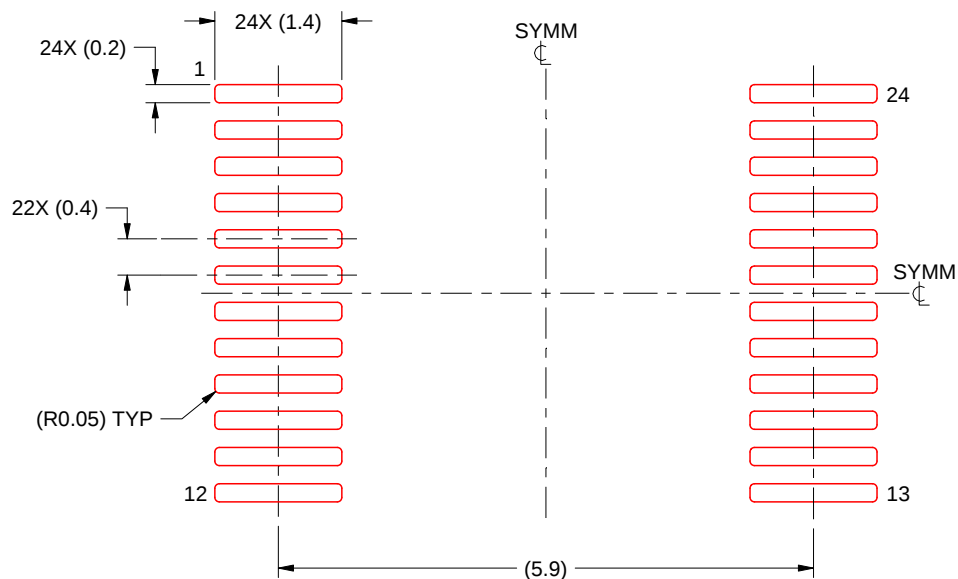
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4229221/A 12/2022

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

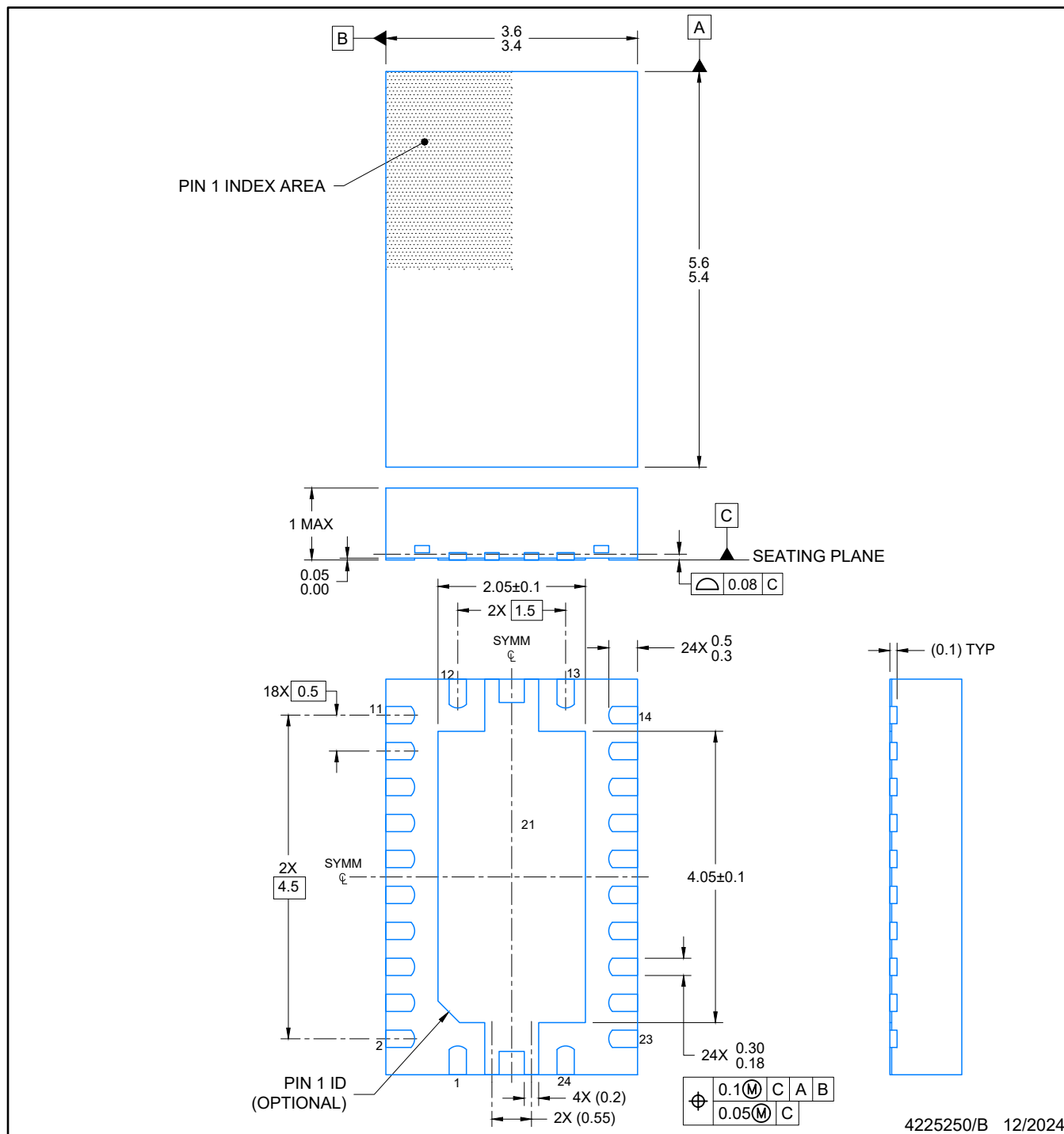
DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

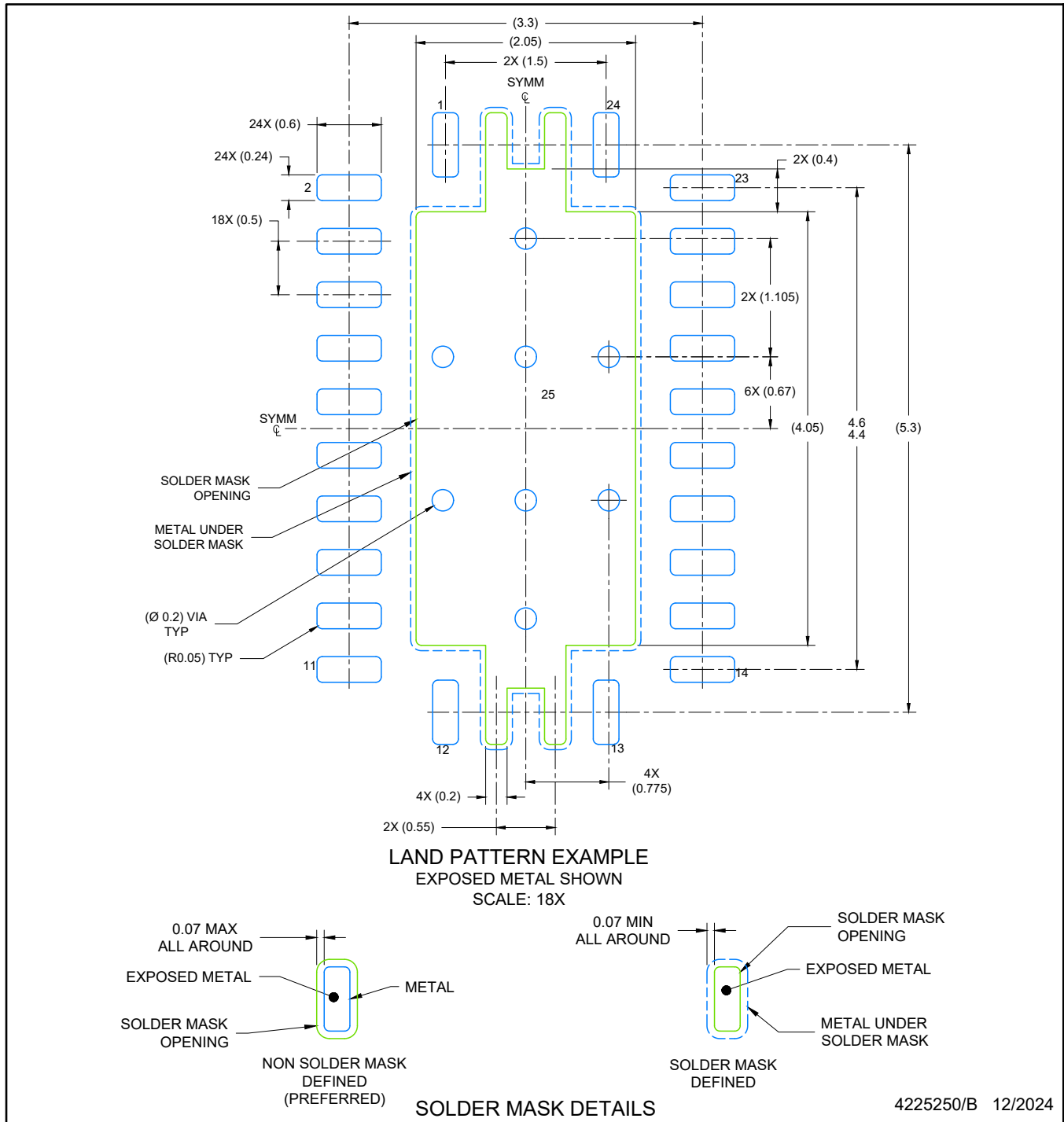


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150



NOTES:

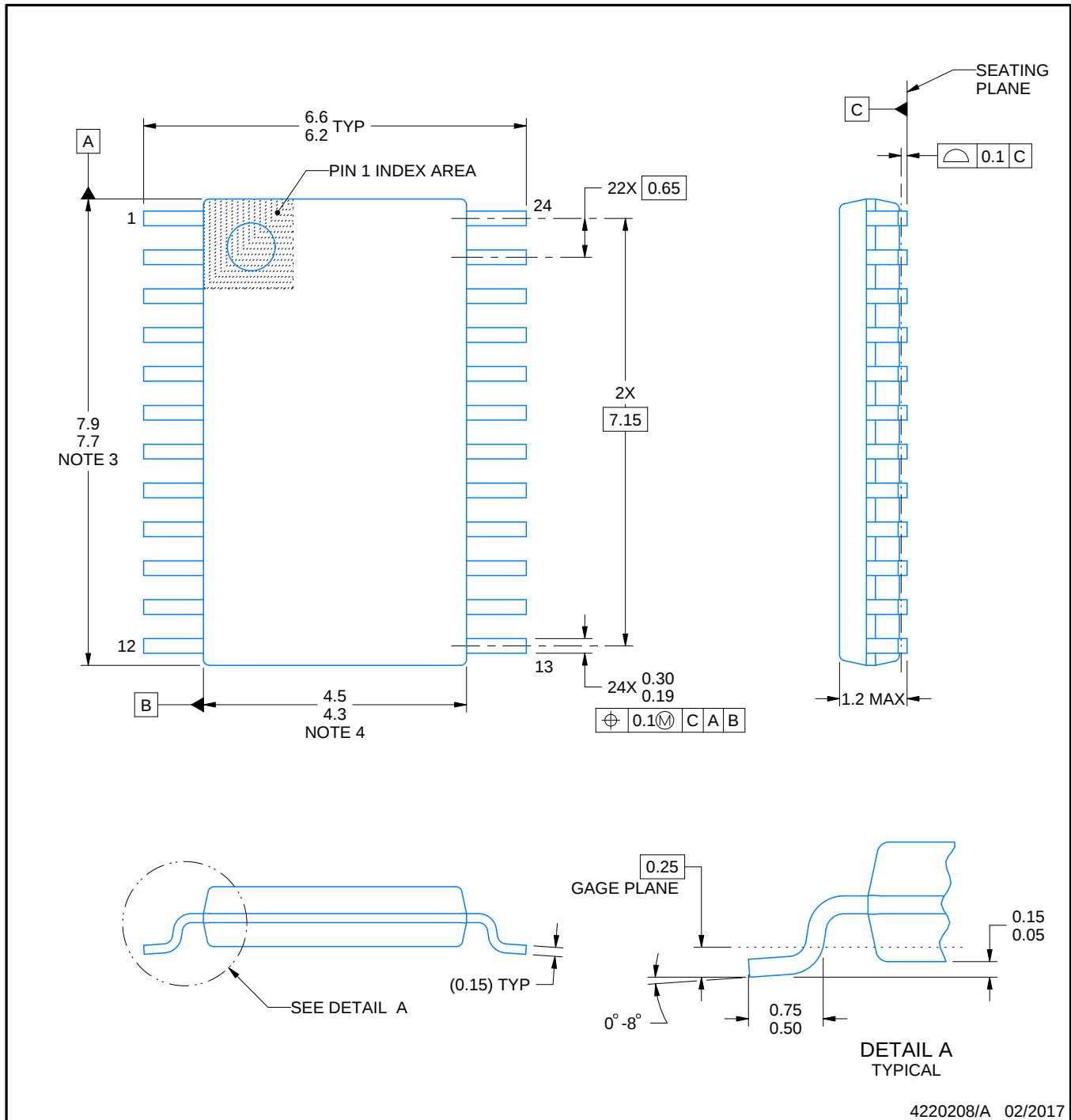
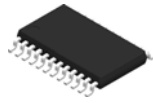
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

PLASTIC QUAD FLATPACK- NO LEAD



4220208/A 02/2017

NOTES:

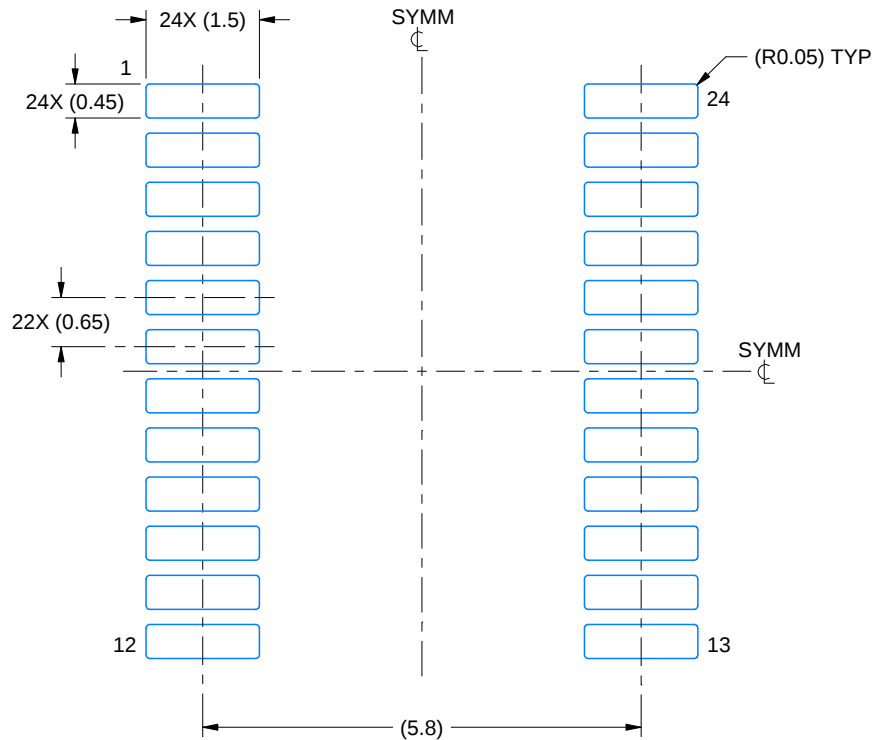
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

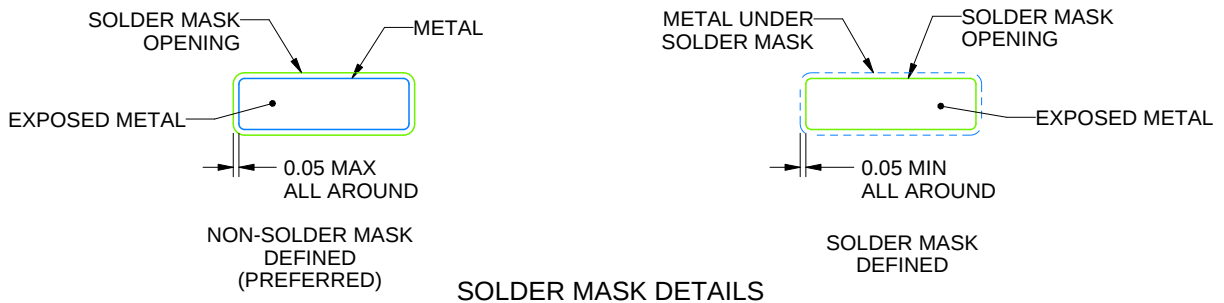
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

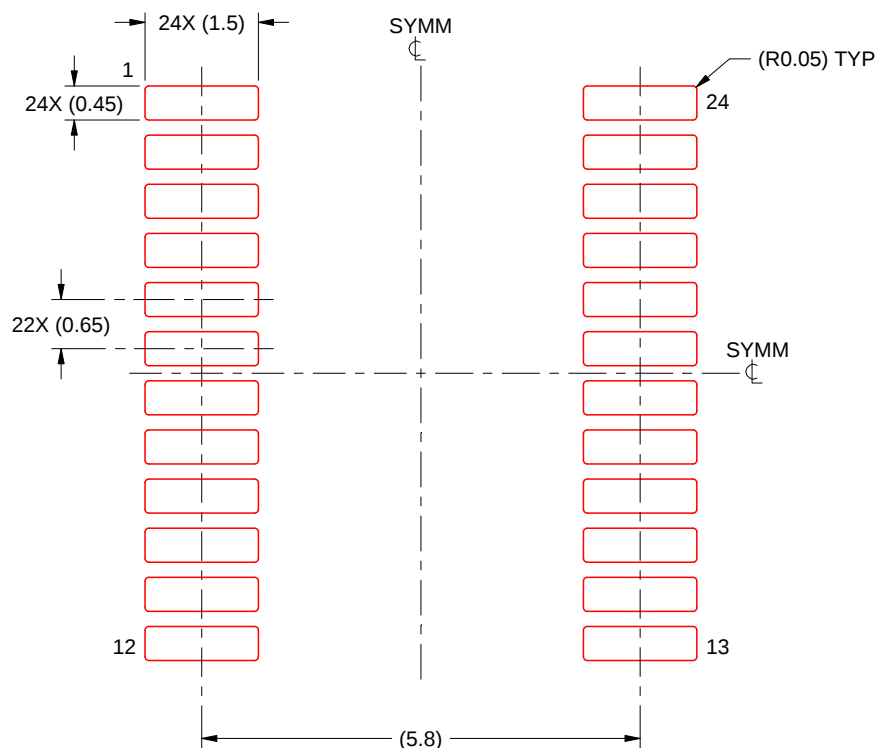
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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