# LM828 Switched Capacitor Voltage Converter

**Check for Samples: LM828**

## FEATURES

- **Inverts Input Supply Voltage**
- **SOT-23 Package**
- **20Ω Typical Output Impedance**
- **97% Typical Conversion Efficiency at 5 mA**

## APPLICATIONS

- **Cellular Phones**
- **Pagers**
- **PDAs**
- **Operational Amplifier Power Supplies**
- **Interface Power Supplies**
- **Handheld Instruments**

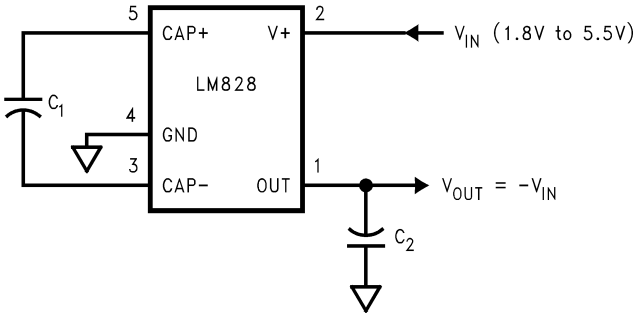
## DESCRIPTION

The LM828 CMOS charge-pump voltage converter inverts a positive voltage in the range of +1.8V to +5.5V to the corresponding negative voltage of −1.8V to −5.5V. The LM828 uses two low cost capacitors to provide up to 25 mA of output current.

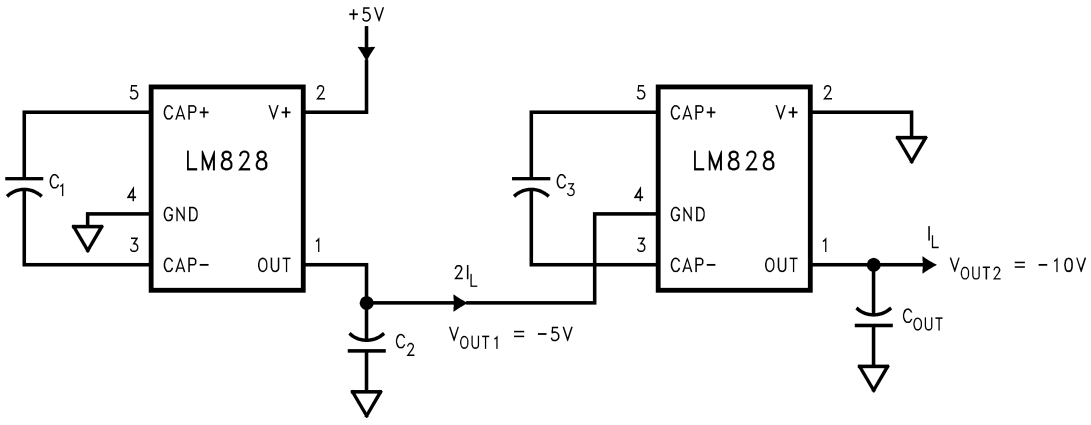
The LM828 operates at 12 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 40 µA (operating efficiency greater than 96% with most loads), the LM828 provides ideal performance for battery powered systems. The device is in a tiny SOT-23 package.

### Basic Application Circuits

**Voltage Inverter**




**+5V to −10V Converter**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings[1][2]

| | |
|---|---|
| Supply Voltage (V+ to GND, or GND to OUT) | 5.8V |
| V+ and OUT Continuous Output Current | 50 mA |
| Output Short-Circuit Duration to GND[3] | 1 sec. |
| Continuous Power Dissipation ($T_A$ = 25°C)[4] | 240 mW |
| $T_{JMax}$[4] | 150°C |
| $\theta_{JA}$[4] | 300°C/W |
| Operating Junction Temperature Range | −40°C to 85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 300°C |
| ESD Rating[5] | 2kV |

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V+, or the device may be damaged.
(4) The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A)/\theta_{JA}$, where $T_{JMax}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance of the package.
(5) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

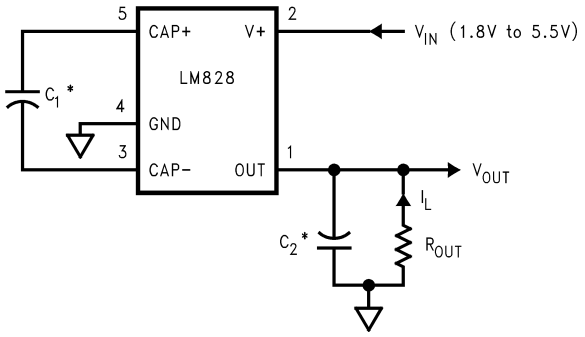
## Electrical Characteristics

Limits in standard typeface are for $T_J$ = 25°C, and limits in **boldface** type apply over the full operating temperature range. Unless otherwise specified: V+ = 5V, $C_1 = C_2$ = 10 µF.[1]

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| V+ | Supply Voltage | $R_L$ =10kΩ | **1.8** | | **5.5** | V |
| $I_Q$ | Supply Current | No Load | | 40 | 75 | µA |
| | | | | | **115** | |
| $R_{OUT}$ | Output Resistance[2] | $I_L$ = 5 mA | | 20 | **65** | Ω |
| $f_{OSC}$ | Oscillator Frequency[3] | Internal | **12** | 24 | **56** | kHz |
| $f_{SW}$ | Switching Frequency[3] | Measured at CAP+ | **6** | 12 | **28** | kHz |
| $P_{EFF}$ | Power Efficiency | $I_L$ = 5 mA | | 97 | | % |
| $V_{OEFF}$ | Voltage Conversion Efficiency | No Load | **95** | 99.96 | | % |

(1) In the test circuit, capacitors $C_1$ and $C_2$ are 10 µF, 0.3Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.
(2) Specified output resistance includes internal switch resistance and capacitor ESR. See the details in the application information.
(3) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2f_{SW}$.

## Test Circuit




*$C_1$ and $C_2$ are 10 µF capacitors.

**Figure 1. LM828 Test Circuit**

## Typical Performance Characteristics

(Circuit of Figure 1, V+ = 5V unless otherwise specified)

**Supply Current vs Supply Voltage**

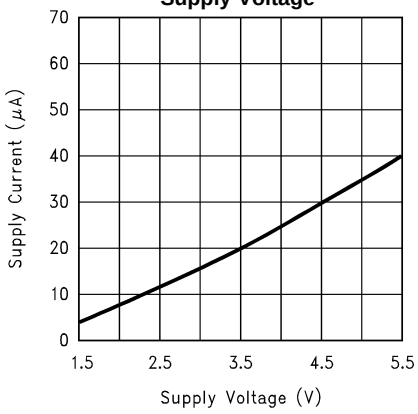



**Figure 2.**

**Supply Current vs Temperature**

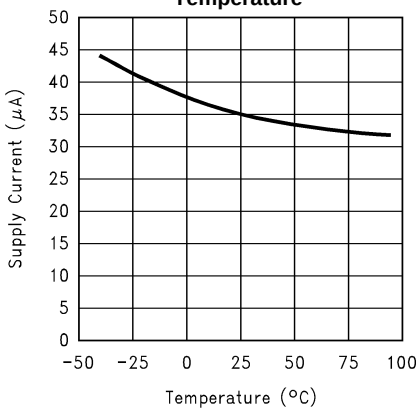



**Figure 3.**

**Output Source Resistance vs Supply Voltage**

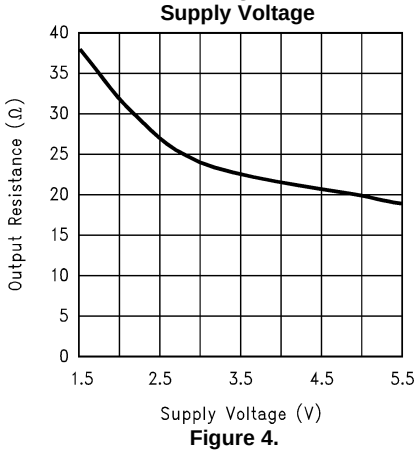



**Figure 4.**

**Output Source Resistance vs Temperature**

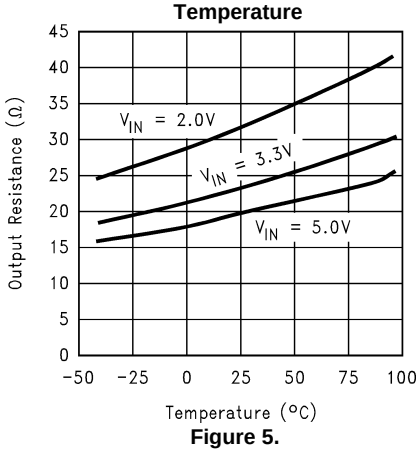



**Figure 5.**

## Typical Performance Characteristics (continued)

(Circuit of Figure 1, V+ = 5V unless otherwise specified)

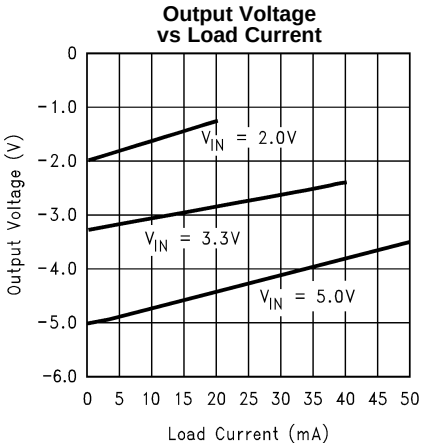



**Figure 6.**

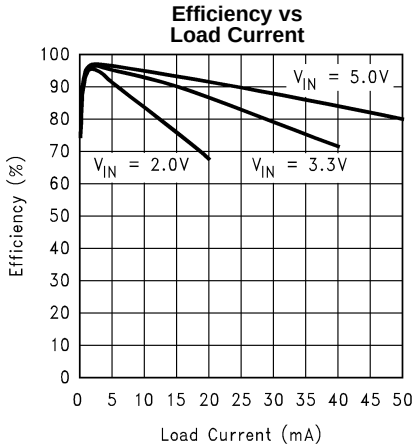



**Figure 7.**

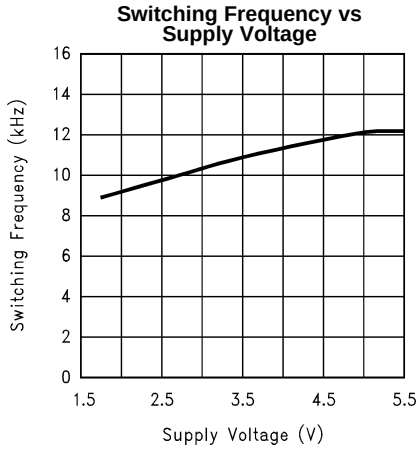



**Figure 8.**

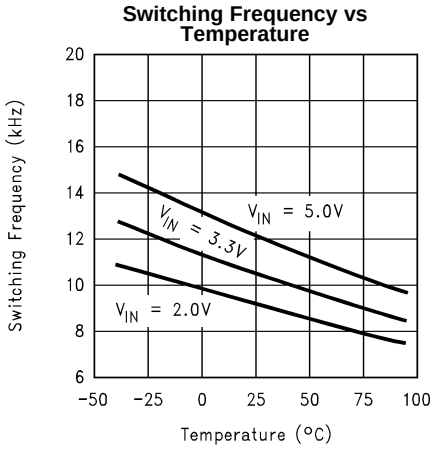



**Figure 9.**

## CONNECTION DIAGRAMS

### 5-Lead SOT-23 Package (DBV)

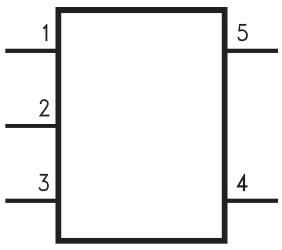



**Figure 10. SOT-23 Package – Top View**
**See Package Number DBV0005A**

**Figure 11. Actual Size**

## Pin Functions

**PIN DESCRIPTIONS**

| Pin | Name | Function |
|---|---|---|
| 1 | OUT | Negative voltage output. |
| 2 | V+ | Power supply positive input. |
| 3 | CAP− | Connect this pin to the negative terminal of the charge-pump capacitor. |
| 4 | GND | Power supply ground input. |
| 5 | CAP+ | Connect this pin to the positive terminal of the charge-pump capacitor. |

## Circuit Description

The LM828 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 12 illustrates the voltage conversion scheme. When $S_1$ and $S_3$ are closed, $C_1$ charges to the supply voltage V+. During this time interval, switches $S_2$ and $S_4$ are open. In the second time interval, $S_1$ and $S_3$ are open; at the same time, $S_2$ and $S_4$ are closed, $C_1$ is charging $C_2$. After a number of cycles, the voltage across $C_2$ will be pumped to V+. Since the anode of $C_2$ is connected to ground, the output at the cathode of $C_2$ equals −(V+) when there is no load current. The output voltage drop when a load is added is determined by the parasitic resistance ($R_{ds(on)}$ of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors.

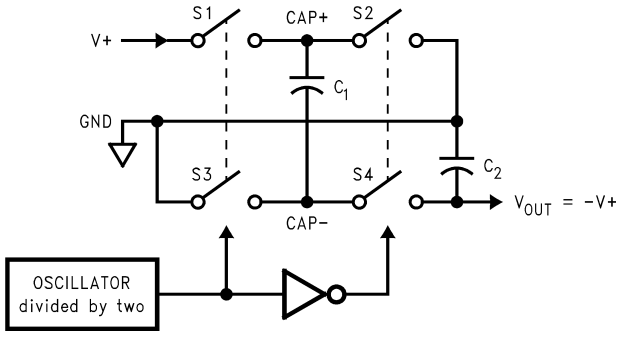



**Figure 12. Voltage Inverting Principle**

## Application Information

### SIMPLE NEGATIVE VOLTAGE CONVERTER

The main application of LM828 is to generate a negative supply voltage. The voltage inverter circuit uses only two external capacitors as shown in the Basic Application Circuits. The range of the input supply voltage is 1.8V to 5.5V.

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals −(V+). The output resistance, $R_{out}$ , is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, the capacitance and the ESR of both $C_1$ and $C_2$. Since the switching current charging and discharging $C_1$ is approximately twice as the output current, the effect of the ESR of the pumping capacitor $C_1$ will be multiplied by four in the output resistance. The output capacitor $C_2$ is charging and discharging at a current approximately equal to the output current, therefore, this ESR term only counts once in the output resistance. A good approximation of $R_{out}$ is:

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2} \quad (1)$$

where $R_{SW}$ is the sum of the ON resistance of the internal MOSFET switches shown in Figure 12.

High capacitance, low ESR capacitors will reduce the output resistance.

The peak-to-peak output voltage ripple is determined by the oscillator frequency, the capacitance and ESR of the output capacitor $C_2$:

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2} \quad (2)$$

Again, using a low ESR capacitor will result in lower ripple.

## CAPACITOR SELECTION

The output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_L{}^2 R_L}{I_L{}^2 R_L + I_L{}^2 R_{OUT} + I_Q (V+)} \quad (3)$$

Where $I_Q(V+)$ is the quiescent power loss of the IC device, and $I_L{}^2R_{out}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

The selection of capacitors is based on the specifications of the dropout voltage (which equals $I_{out}$ $R_{out}$), the output voltage ripple, and the converter efficiency. Low ESR capacitors (following table) are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

**Low ESR Capacitor Manufacturers**

| Manufacturer | Phone | Capacitor Type |
|---|---|---|
| Nichicon Corp. | (708)-843-7500 | PL & PF series, through-hole aluminum electrolytic |
| AVX Corp. | (803)-448-9411 | TPS series, surface-mount tantalum |
| Sprague | (207)-324-4140 | 593D, 594D, 595D series, surface-mount tantalum |
| Sanyo | (619)-661-6835 | OS-CON series, through-hole aluminum electrolytic |
| Murata | (800)-831-9172 | Ceramic chip capacitors |
| Taiyo Yuden | (800)-348-2496 | Ceramic chip capacitors |
| Tokin | (408)-432-8020 | Ceramic chip capacitors |

## Other Applications

### *PARALLELING DEVICES*

Any number of LM828s can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor $C_1$, while only one output capacitor $C_{out}$ is needed as shown in Figure 13. The composite output resistance is:

$$R_{OUT} = \frac{R_{OUT} \text{ of each LM828}}{\text{Number of Devices}} \quad (4)$$

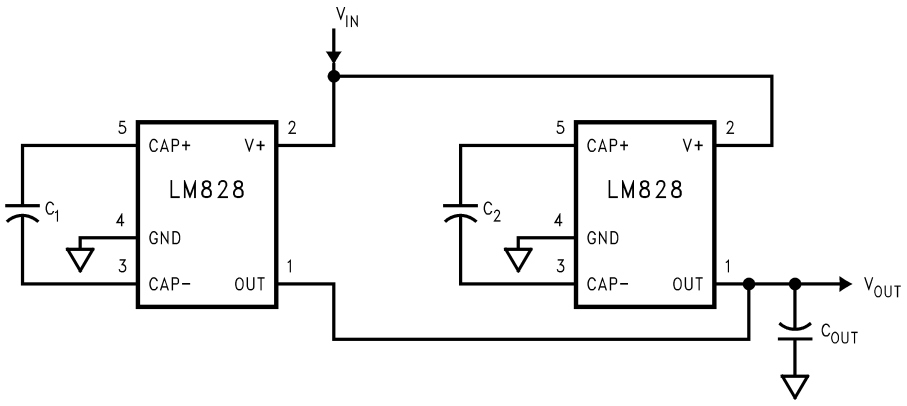



**Figure 13. Lowering Output Resistance by Paralleling Devices**

### CASCADING DEVICES

Cascading the LM828s is an easy way to produce a greater negative voltage (e.g. A two-stage cascade circuit is shown in Figure 14).

If n is the integer representing the number of devices cascaded, the unloaded output voltage $V_{out}$ is ($-nV_{in}$). The effective output resistance is equal to the weighted sum of each individual device:

$$R_{out} = nR_{out\_1} + n/2\ R_{out\_2} + ... + R_{out\_n} \quad (5)$$

This can be seen by first assuming that each device is 100 percent efficient. Since the output voltage is different on each device the output current is as well. Each cascaded device sees less current at the output than the previous so the $R_{OUT}$ voltage drop is lower in each device added. Note that, the number of n is practically limited since the increasing of n significantly reduces the efficiency, and increases the output resistance and output voltage ripple.

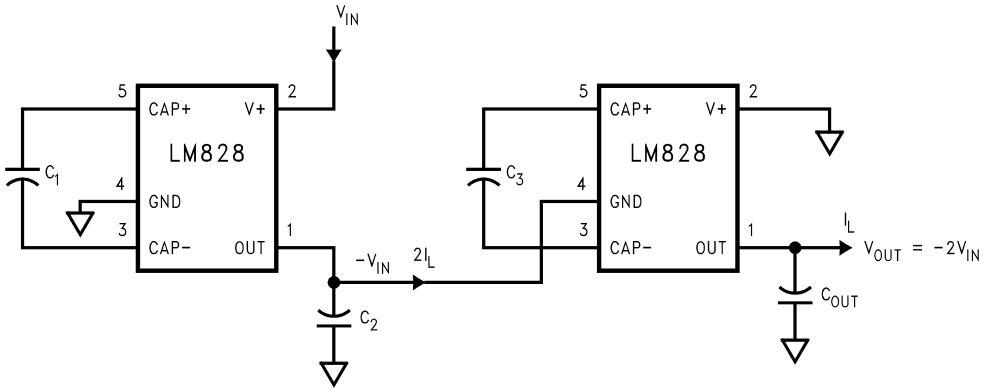



**Figure 14. Increasing Output Voltage by Cascading Devices**

### COMBINED DOUBLER AND INVERTER

In Figure 15, the LM828 is used to provide a positive voltage doubler and a negative voltage converter. Note that the total current drawn from the two outputs should not exceed 40 mA.

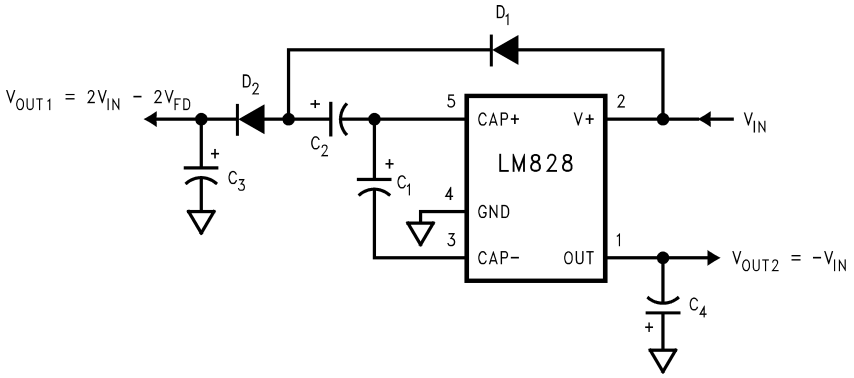



**Figure 15. Combined Voltage Doubler and Inverter**

### *REGULATING $V_{OUT}$*

It is possible to regulate the negative output of the LM828 by use of a low dropout regulator (such as the LP2980). The whole converter is depicted in Figure 16. This converter can give a regulated output from −1.8V to −5.5V by choosing the proper resistor ratio:

$$V_{out} = V_{ref} (1 + R_1/R_2) \quad (6)$$

where, $V_{ref} = 1.23V$ (7)

Note that the following conditions must be satisfied simultaneously for worst case design:

$$V_{in\_min} > V_{out\_min} + V_{drop\_max} \text{ (LP2980)} \quad (8)$$

$$+ I_{out\_max} \times R_{out\_max} \text{ (LM828)} \quad (9)$$

$$V_{in\_max} < V_{out\_max} + V_{drop\_min} \text{ (LP2980)} \quad (10)$$

$$+ I_{out\_min} \times R_{out\_min} \text{ (LM828)} \quad (11)$$

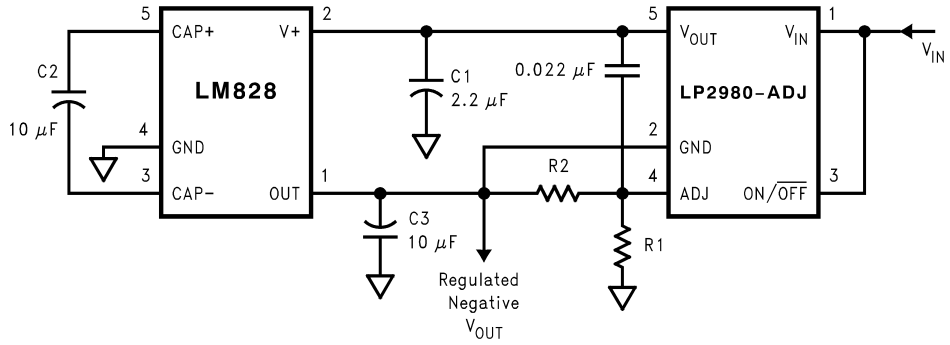



**Figure 16. Combining LM828 with LP2980 to Make a Negative Adjustable Regulator**

## REVISION HISTORY

| Changes from Revision C (May 2013) to Revision D | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 8 |

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM828M5/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | S08A |
| LM828M5X/NOPB | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | S08A |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

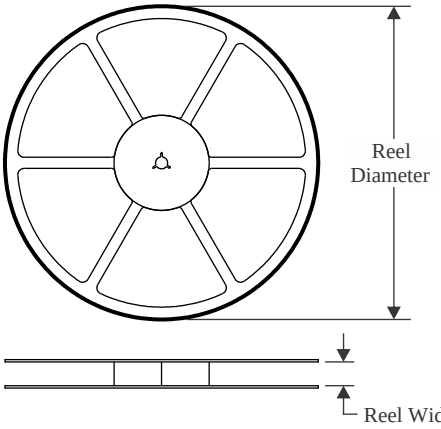
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

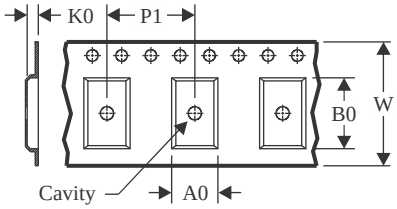
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

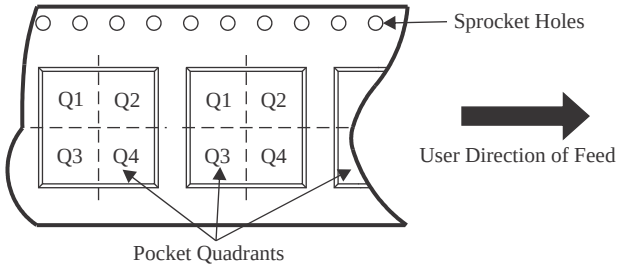



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

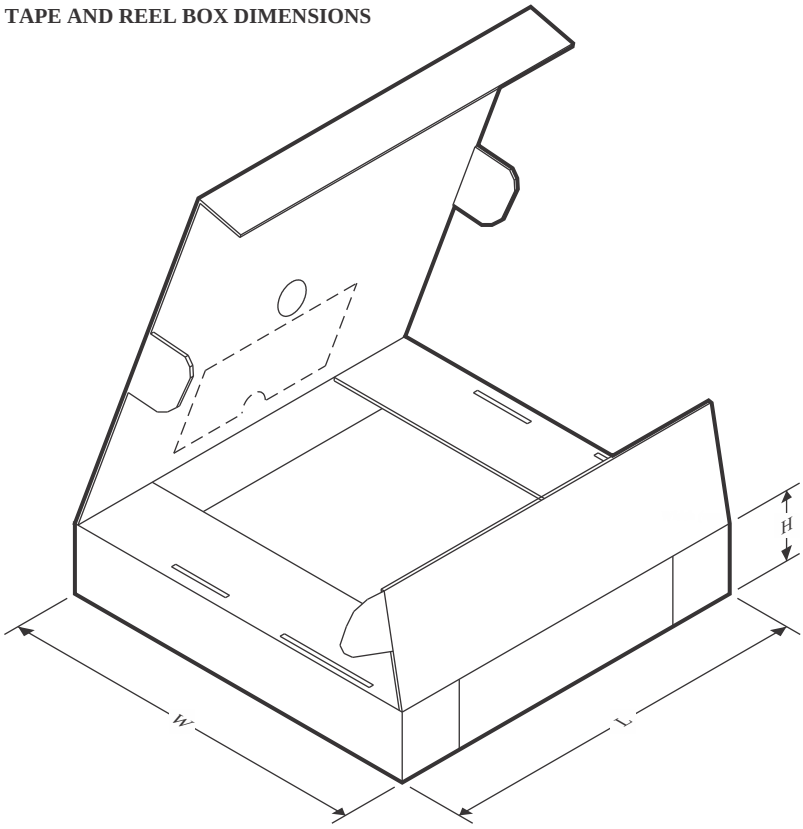
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM828M5/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q2 |
| LM828M5X/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

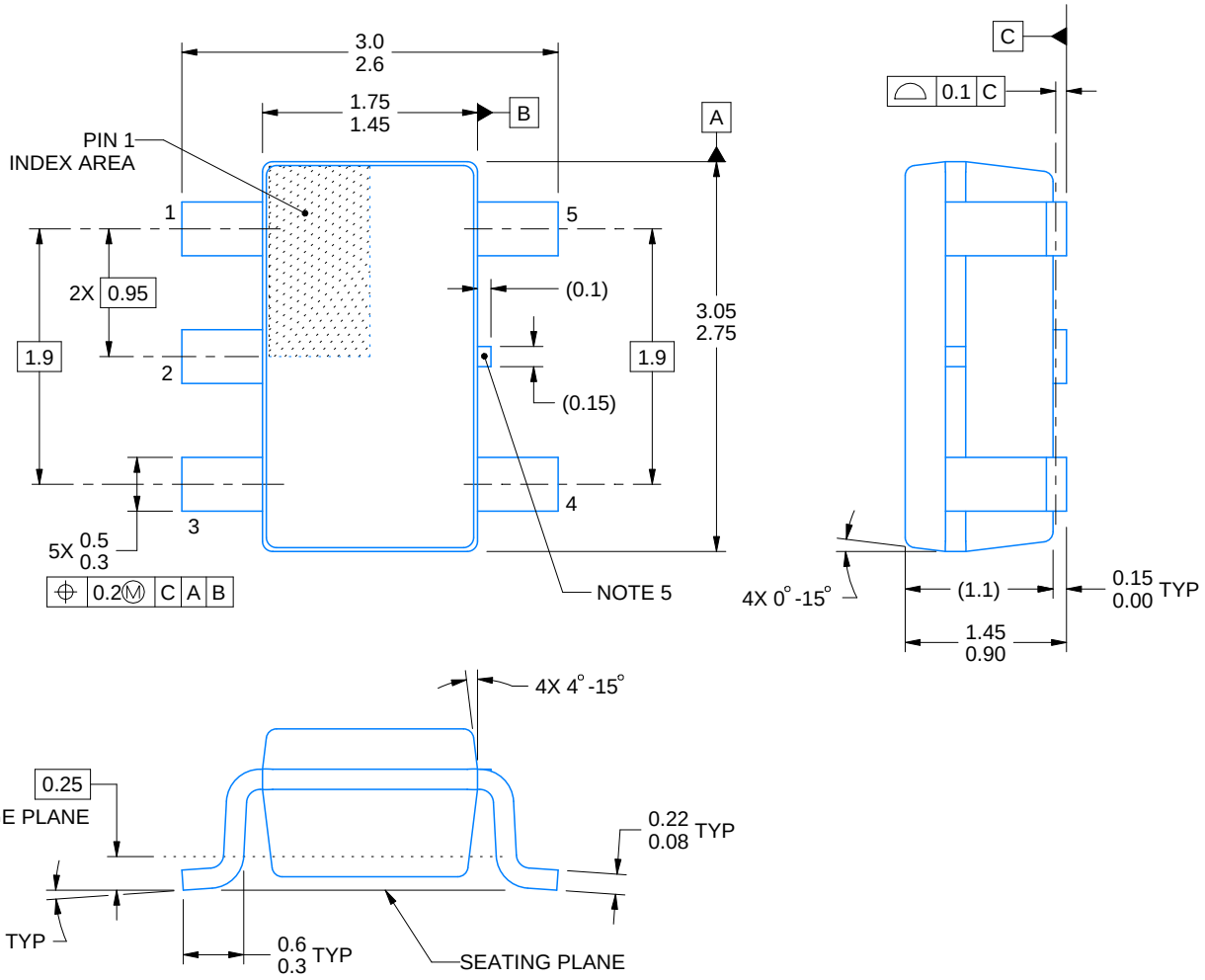
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM828M5/NOPB | SOT-23 | DBV | 5 | 1000 | 208.0 | 191.0 | 35.0 |
| LM828M5X/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

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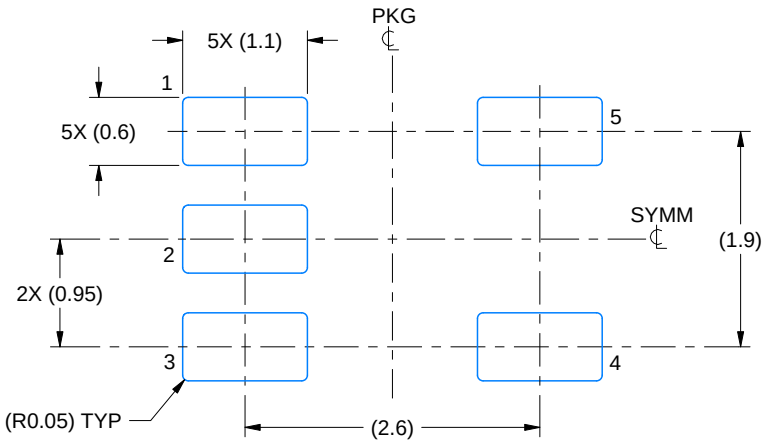
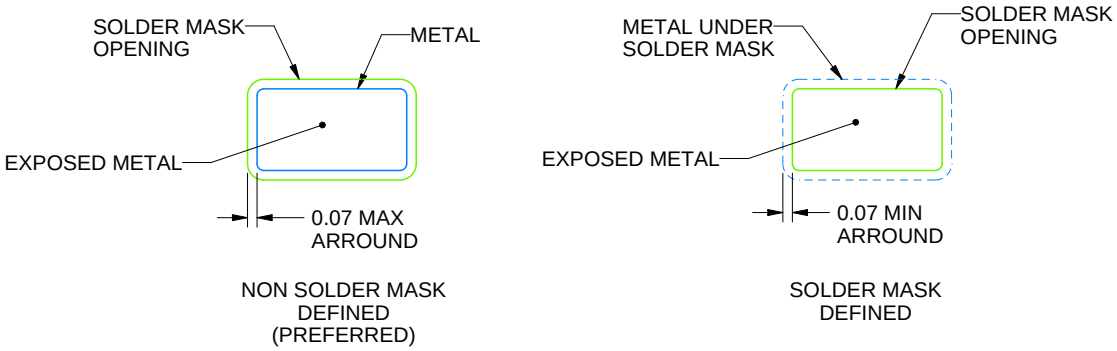
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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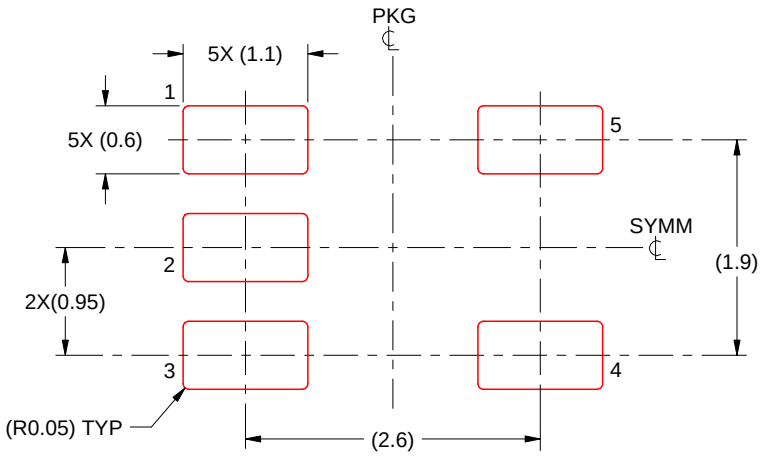
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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