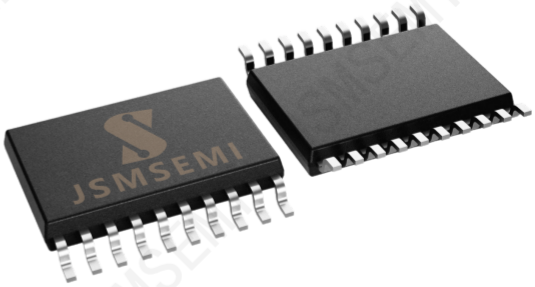
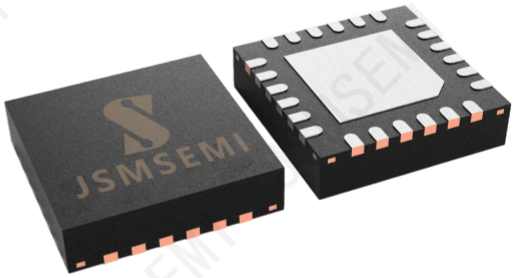
1 Description

The JSM6288 is a high voltage，high speed power MOSFET drivers with dependent high-side and low-side referenced output channels.Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.The logic input is compatible with standard CMOS or LSTTL output,down to 3.3 Vlogic.

The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction.The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 250V. The JSM6288T1 is TSSOP20 package and the JSM6288Q1 is QFN24 package can operate in the temperature range from -40℃ to 125℃.





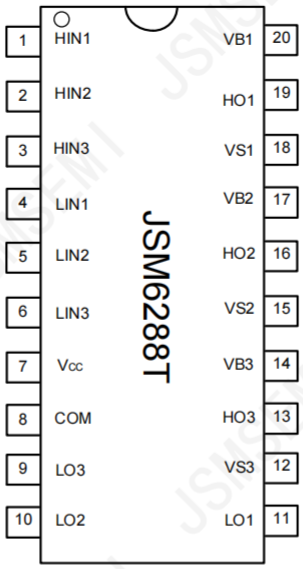
2 Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +250 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ±50 V/nsec
- Allowable negative Vs capability: -9V
- Gate drive supply range from 5 V to 20V
- High and low side undervoltage locking circuit
  -high side undervoltage locking forward threshold 4.5V
  -high side undervoltage locking negative threshold 4.3V
  -low side undervoltage locking forward threshold 4.5V
  -low side undervoltage locking negative threshold 4.3V
- Cross-conduction prevention logic
  - Deadtime:200ns
- Chip transmission delay characteristics
  -on / off transmission delay Ton / Toff = 150ns / 120ns
  -the delay matching time is less than 50 ns
- Matched propagation delay for both channels
- Wide operating temperature range -40°C ~125°C
- Typically output Source/Sink current capability: 1.5A/1.8A
- RoSH compatible

3 Application

- Motor Control
- Electric machine control
- General Purpose Inverters
- Power tool
- Electric vehicle/UAV
- Lawn mower/snow removal machine

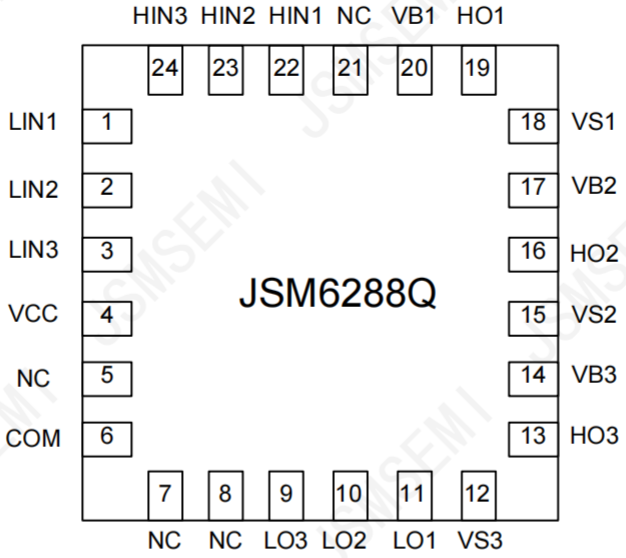
4 Function Pin Description



TSSOP-20 Top view

Lead Definitions

Number	Symbol	Description
1	HIN1	Logic inputs for high side gate driver output , in phase
2	HIN2	Logic inputs for high side gate driver output , in phase
3	HIN3	Logic inputs for high side gate driver output , in phase
4	LIN1	Logic inputs for low side gate driver output , in phase
5	LIN2	Logic inputs for low side gate driver output , in phase
6	LIN3	Logic inputs for low side gate driver output , in phase
7	VCC	Low side and logic fixed supply
8	COM	Low side gate drivers return
9	LO3	Low side gate driver output
10	LO2	Low side gate driver output
11	LO1	Low side gate driver output
12	VS3	High voltage floating supply return
13	HO3	High side gate driver output
14	VB3	High side floating supply
15	VS2	High voltage floating supply return
16	HO2	High side gate driver output
17	VB2	High side floating supply
18	VS1	High voltage floating supply return
19	HO1	High side gate driver output
20	VB1	High side floating supply



QFN-24 Top view

Lead Definitions

Number	Symbol	Description
1	LIN1	Logic inputs for low side gate driver output , in phase
2	LIN2	Logic inputs for low side gate driver output , in phase
3	LIN3	Logic inputs for low side gate driver output , in phase
4	V_{CC}	Low side and logic fixed supply
6	COM	Low side gate drivers return
9	LO3	Low side gate driver output
10	LO2	Low side gate driver output
11	LO1	Low side gate driver output
12	VS3	High voltage floating supply return
13	HO3	High side gate driver output
14	VB3	High side floating supply
15	VS2	High voltage floating supply return
16	HO2	High side gate driver output
17	VB2	High side floating supply
18	VS1	High voltage floating supply return
19	HO1	High side gate driver output
20	VB1	High side floating supply
22	HIN1	Logic inputs for high side gate driver output , in phase
23	HIN2	Logic inputs for high side gate driver output , in phase
24	HIN3	Logic inputs for high side gate driver output , in phase

5 Product specifications

Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	275	V
V_S	High side floating supply return	V_B – 25	V_B + 0.3	
V_{HO}	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	25	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN & LIN	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns

ESD rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	1500	—	V
	Machine Model	500	—	V

Rated power

Symbol	Definition	MIN.	MAX.	Units
P_D	Package Power Dissipation @ TA ≤25°C	—	1.25	W

Thermal information

Symbol	Definition	MIN.	MAX.	Units
Rth_{JA}	Thermal Resistance, Junction to Ambient	--	100	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	VS + 6	VS + 20	V
V_S	High side floating supply return	-9	250	
V_{HO}	High side gate drive output	V_S	V_B	
V_{CC}	Low side and main power supply	5	20	
V_{LO}	Low side gate drive output	0	V_{CC}	
V_{IN}	Logic input of HIN & LIN	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note1：Transient negative VS can be used for COM-50V with a pulse width of 50ns, guaranteed by design..

Note2：When the input pulse width is less than 1us, the input pulse cannot be transmitted normally .

Electrical Characteristics

Valid for temperature range at T_A= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

Dynamical electrical characteristics

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	150	250	ns	V_S=0V
t_{OFF}	Turn-off propagation delay	—	120	250	ns	V_S=250V
t_R	Turn-on rise time	—	30	—	ns	
t_F	Turn-off fall time	—	30	—	ns	
DT	Deadtime	100	200	300	ns	
MT	Matching delay ON and OFF	—	—	50	ns	

Static electrical characteristics

Valid for temperature range at T_A= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{CCUV+}	VCC supply UVLO threshold	—	4.5	—	V	
V_{CCUV-}		—	4.3	—	V	
$V_{CCUVHYS}$	VCC supply undervoltage lockout hysteresis	—	0.2	—	V	
V_{BSUV+}	VBS supply UVLO threshold	—	4.5	—	V	
V_{BSUV-}		—	4.3	—	V	
$V_{BSUVHYS}$	VBS supply undervoltage lockout hysteresis	—	0.2	—	V	
I_{LK}	High-side floating supply leakage current	—	—	90	μA	V_B=V_S=250V
I_{QBS}	Quiescent VB supply current	—	70	150	μA	V_{IN}=0V or 5V
I_{QCC}	Quiescent VCC supply current	—	230	350	μA	V_{IN}=0V or 5V
V_{IH}	Logic “1”(HIN & LIN) input voltage	2.5	—	—	V	
V_{IL}	Logic “0” (HIN &LIN) input voltage	—	—	0.8	V	
V_{OH}	High level output voltage, VBIAS - VO	—	—	0.2	V	I_O=0A
V_{OL}	Low level output voltage, VO	—	—	0.1	V	I_O=0A
I_{IN+}	Logic “1” Input bias current	—	25	50	μA	HIN=5V, LIN=0V
I_{IN-}	Logic “0” Input bias current	—	—	2	μA	HIN=0V, LIN=5V
Vs	VS negative surge	—	-9	—	V	
I_{O+}	Output high short circuit pulsed current	1.1	1.5	—	A	V_O=0V PW≤10us
I_{O-}	Output low short circuit pulsed current	1.3	1.8	—	A	V_O=15V PW≤10us

6 Function Description

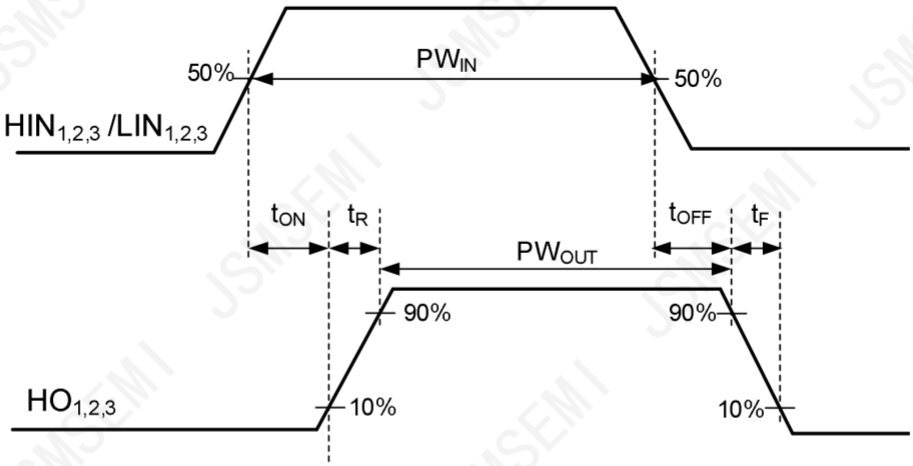


Figure 6-1 JSM6288 Input and output timing waveform

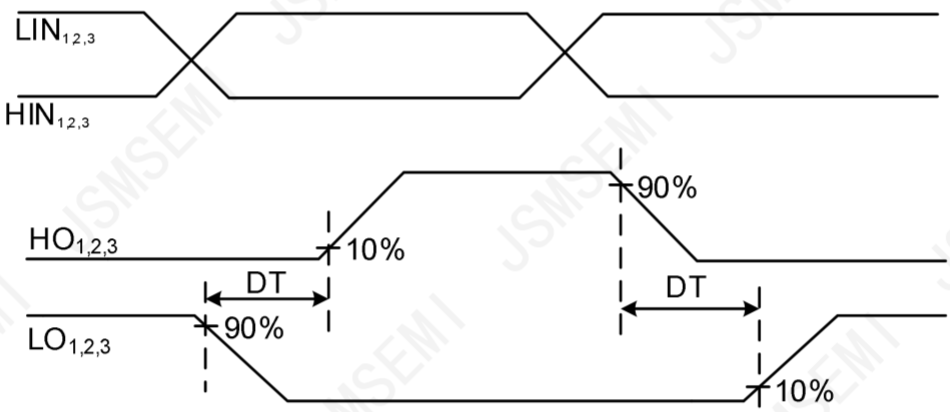


Figure 6-2 Propagation Time Waveform Definition

7 JSM6288 Description

Overview

The JSM6288 is a three-phase high-voltage, high-speed power MOSFET high-low driver chip with separate high-side and low-side reference output channels. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 Vlogic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 250 V, The floating channel requires additional bootstrap circuit support. In addition, both the high side and the low side of the JSM6288 include undervoltage protection.

Function Block Diagram

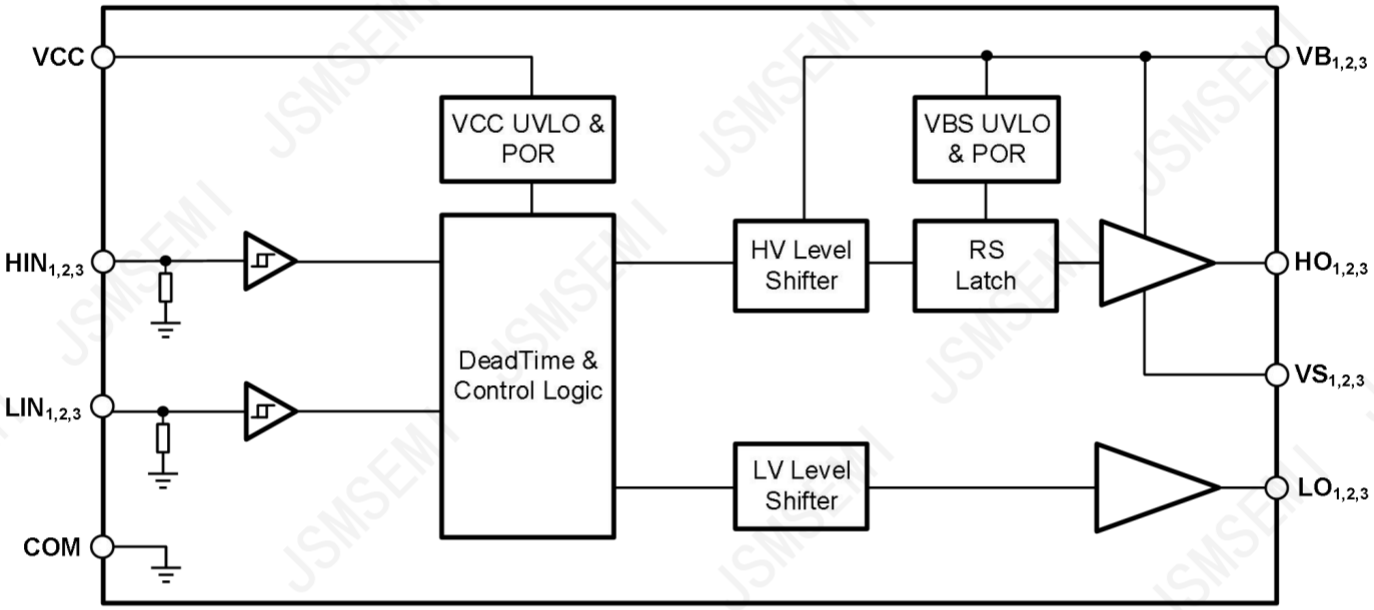


Figure7-1 Function Block Diagram of JSM6288

Chip operating logic

The signal input port of the JSM6288 adopts the level-triggered mode, that is, the voltage meets the logical requirements, and the chip can work normally, as shown in Table 7-1.

Table 7-1 I/O logical table

INPUT		OUTPUT	
HIN1,2,3	LIN1,2,3	HO1,2,3	LO1,2,3
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L
Note: H stands for high level; L stands for low level			

Signal input port

The JSM6288 includes three-phase high-side and low-side signal input ports for receiving control signals from the master.

There is an interlock function between the high side and the low side. When the input signal of the high side is high and the input signal of the low side is low, this function will be triggered, making the output signal of the high side and the low

side become low level signals. Moreover, there is a built-in dead time between the high side and the low side signals, which effectively avoids the overlapping of output signals. The HIN port is designed to have 800K resistance to VSS and the LIN port is designed to have 800K resistance to VCC. Therefore, the two ports can be floating when not in use.So they can be floating when not in use, but shorting with COM is recommended.

Output port

The internal push-pull structure of the output port is used to directly drive the power device MOSFET/IGBT. The reference ground of the output port on the low side is COM, and the reference ground of the output port on the high side is VS. When VS is high voltage, the voltage domain between VB-VS needs to be powered by the bootstrap circuit to work normally. The VS pin has a certain negative pulse resistance, which can ensure that no damage occurs under the pulse condition of -9V, 50ns.

Undervoltage protection function

The low-voltage driver of the JSM6288 includes an undervoltage protection circuit that monitors the supply voltage (VCC)and a UVLO circuit that will suppress all output until the voltage is sufficient to drive the external MOSFETs (up to acorresponding preset threshold). Therefore,

all output ports remain low until the voltage of the VCC pin rises above theUVLO threshold.

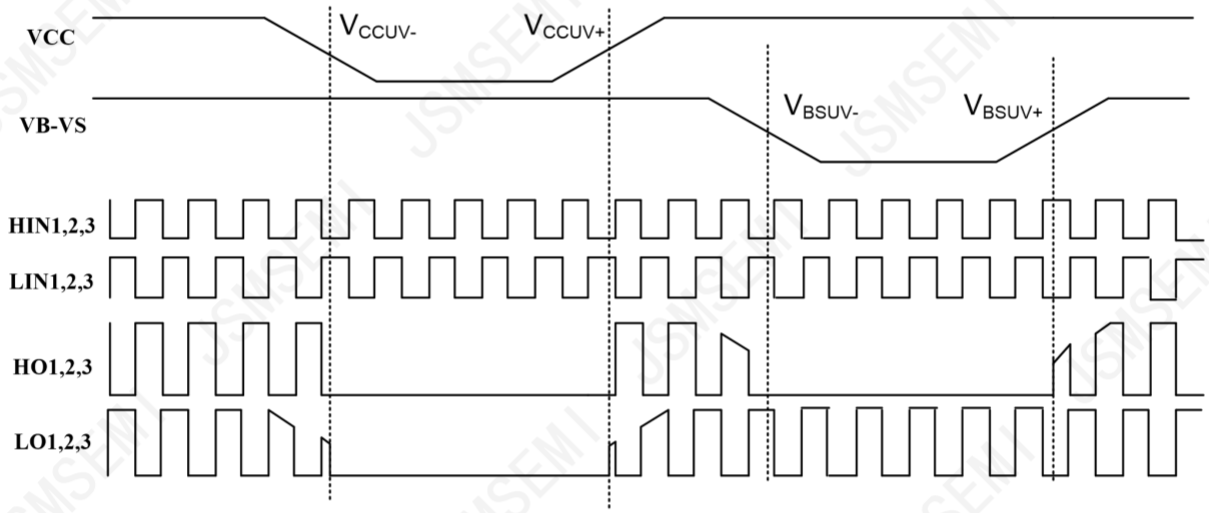


Figure7-2 Undervoltage function waveform definition

As shown in Figure 7-2, when the VCC undervoltage occurs, all output signals immediately become low. When the VCC voltage rises again and exceeds the undervoltage threshold, all output signals recover, and the LO voltage is the same as that of the current VCC. When the high-side bootstrap capacitor voltage (VB-VS) is reduced below the undervoltage threshold, the high-side output immediately becomes low, and the LO output signal is not affected. When the high-side bootstrap capacitor voltage (VB-VS) rises above the undervoltage threshold, the HO output signal recovers, and the HO voltage is consistent with the current high-side bootstrap capacitor voltage (VB-VS). In addition, the threshold hysteresis of UVLO is built into the JSM6288 .

There is a certain hysteresis between the threshold of the power supply voltage drop

triggering undervoltage and the threshold of the voltage rebound chip working normally, which can prevent abnormal output waveform when the power supply voltage fluctuates.

8 Application message

In most application environments, the PWM output voltage of the main control IC is usually only 3.3V or 5V, which is not enough to drive the MOSFET at the power end. Therefore, a high-power driver chip is needed between the main control IC and the MOSFET to drive the grid voltage of the MOSFET, so that the drive voltage rises to 12V-15V. This allows the MOSFET to be in a stable, fully open state. At the same time, the driver chip improves the switching speed of the power device and reduces the related switching power loss.

Typical application circuit

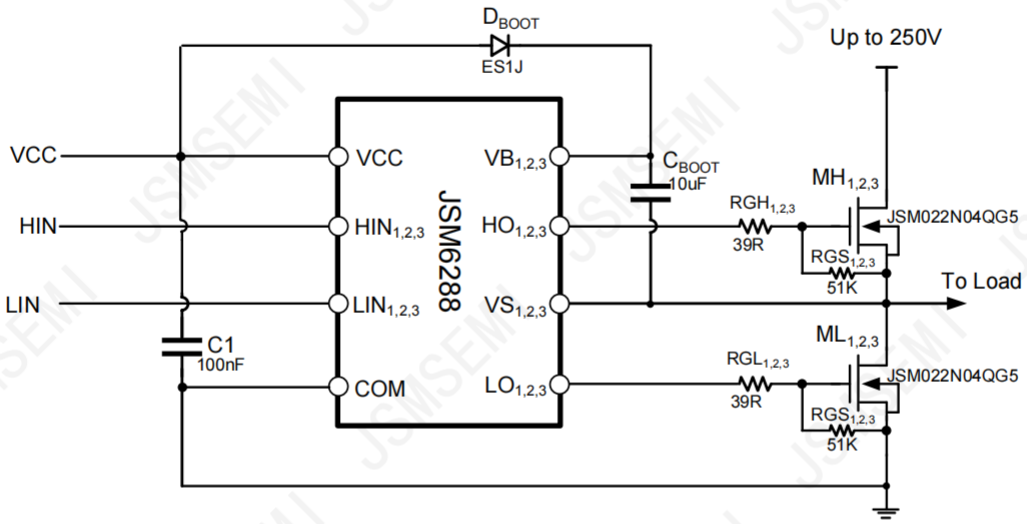


Figure8-1 Typical application circuit of JSM6288

Bootstrap Circuit Design Guide

The structure of a general half-bridge circuit is shown in Figure 8-2, including bootstrap resistance, bootstrap diode and bootstrap capacitor. This scheme is the most commonly used and cost-effective scheme in the current motor drive.

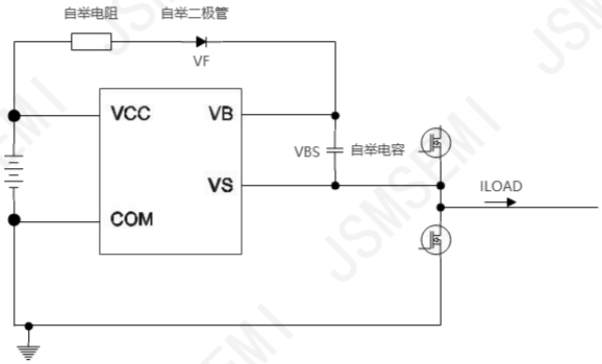


Figure 8-2 Basic structure of the bootstrap circuit

Bootstrap circuit capacitance selection

In order to determine the size of the bootstrap capacitance, we first need to evaluate the following points：

-The gate charge required for MOS to turn on: Q_g;

-GS leakage of MOS: I_{LK_GS};

-Static operating current of the drive: I_{QBS};

-Leakage of bootstrap diode: I_{LK_DIODE};

-Bootstrap capacitor leakage: I_{LK_CAP};

-Upper bridge height time: T_{HON}.

I_{LK_CAP} is included in the calculation only when the bootstrappable capacitor uses an electrolytic capacitor. Other types of capacitors do not need to be considered. It is recommended to use at least one low ESR ceramic capacitor. Parallel electrolytic capacitor and low ESR ceramic capacitor can achieve better circuit performance.

By calculation, we can find the loss of capacitance for a single turn on：

$$Q_{TOT} = Q_G + (I_{LK\_GS} + I_{QBS} + I_{LK\_DIODE} + I_{LK\_CAP}) \times T_{HON}$$

Specifies the range that VBS can drop during bootstrapping: $\triangle V_{BS}$

$$\Delta V_{BS} \leq V_{CC} - V_F - V_{GSmin} - V_{DSon}$$

In the process, you need assurance：

$$V_{GSmin} > V_{BSUV-}$$

V_F MOS reverse diode voltage drop

V_{GEmin} Maintain the minimum gate voltage for MOS tube conduction

V_{DSon} On-off pressure drop of the lower bridge MOS

And with that, you can calculate it：

$$C_{BOOTmin} = \frac{Q_{TOT}}{\triangle V_{BS}}$$

Note: In the process of calculating bootstrap capacitance here, only the charge required for a pulse process is calculated, without considering the duty ratio and frequency of PWM. If the signal is controlled by PWM wave, please get the actual required bootstrap capacitance size based on the above calculation method through a certain equivalent conversion.

Note on bootstrap circuit

A. Bootstrap resistance

Bootstrap resistors are used in some bootstrap circuits and are not required. HO and LO may have abnormal jump during startup. At this time, the increase of bootstrap resistance will limit the current passing through the bootstrap diode when the bootstrap circuit is started, which can effectively suppress some bad signals and protect the circuit.

B. Bootstrap capacitor

ESR must be considered in the design of the circuit with the upper bridge arm open for a long time when the electrolytic capacitor is used as the bootstrap capacitor. When the upper bridge arm is opened for a long time, a bootstrap capacitor with a large capacity is required, and electrolytic capacitors are generally used. But the electrolytic capacitor has a certain internal resistance, which will reduce the partial voltage of bootstrap resistance and can not realize its function. This situation can be effectively avoided by connecting a ceramic capacitor with a low ESR.

C. Bootstrap diode

The bootstrap diode is used to maintain the voltage stability of the bootstrap circuit. It is necessary to ensure that the reverse voltage resistance of the diode is greater than the voltage of the driving power supply. On this basis, fast recovery

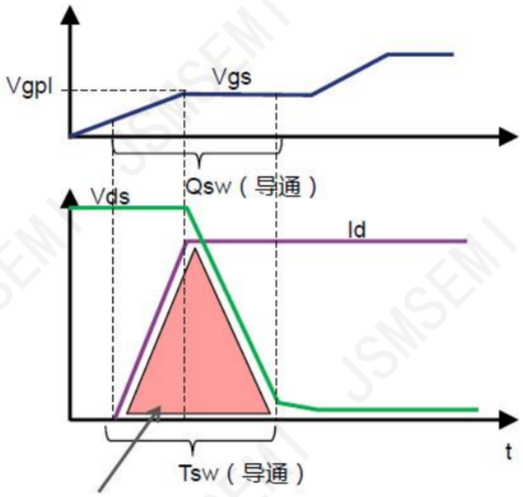
diodes such as Schottky diodes are selected as much as possible.

Bootstrap Circuit Design Guide

Gate resistance is used to control the switching speed of the driven MOS and the slope of the rising and falling edge, which will affect a number of application performance, such as loss, reliability and so on. This section describes how to select the driving resistance and discusses the impact of the driving resistance. The selection of grid resistance is closely related to the driver chip, MOSFET and even circuit design, and it needs to be re-selected according to the actual situation in different environments.

Common industrial brushless motors operate at a frequency of about 2kHz-10kHz. Based on this, grid resistors of 20-120 Ω are usually selected. This is determined by the following two factors：

（1） **Switching loss of MOS.** Part of the MOS loss is switching loss, and the other part is on-off loss, while the grid resistance mainly affects the loss of the switching process. The larger the resistance value, the slower the switching process, and the larger the overlap area of voltage and current, the greater the loss. The most direct impact of excessive loss is that the chip temperature will rise rapidly, and the device will face the risk of failure under the condition of higher than 150℃.



$$Psw(on) = \frac{1}{2} \times Id \times Vds \times Tsw(on)$$

Figure 8-3 MOS switch loss under resistive load

（2） **Reliability.** As opposed to loss, the smaller the resistance value of the gate resistance, the faster the MOSFET will switch. In practical applications, the power end current is larger, more sensitive to parasitic parameters, too high switching speed will increase the signal instability, light will make the motor EMI is too large, heavy will make the circuit damage. Some of the most common are:

1) Grid signal rings, causing MOS damage (as shown in Figure 8-4);

2) The dv/dt is too fast, and the VS port will bear too high or too low voltage signal, resulting in drive damage.。

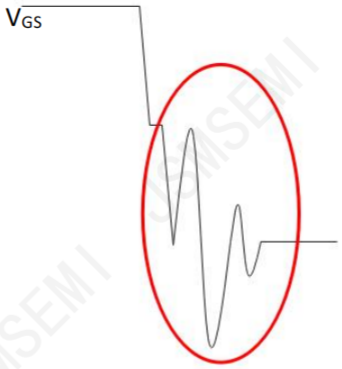


Figure 8-4 Grid ringing

PCB layout guide

To achieve the outstanding performance of half bridge grid driver chips, the following printed circuit board (PCB) layout routing guidelines should be followed.

• Low ESR/ESL capacitors should be placed near the driver chip between the VCC and COM pins, and between the VB and VS pins to provide peak current for the VCC and VB pins.

• To prevent large voltage transients from high-side MOSFET drains, a low ESR electrolytic capacitor and a ceramic capacitor must be connected between the high-side MOSFET drain and the ground (COM).

• To avoid excessive negative voltage transients on switch node (VS) pins, the parasitic inductance between the high-side MOSFET source and the low-side MOSFET (synchronous rectifier) source must be minimized.

• Overlap of the VS layer with the ground (COM) layer should be avoided as much as possible to minimize the coupling of switching noise from the VS layer to the ground layer.

• The heat dissipation pad of the driver chip should be connected to a large area of thick copper layer to improve the heat dissipation performance of the driver chip. The heat dissipation pad is usually connected to the ground that is equal to the COM of the chip. It is recommended to connect the heat dissipation pad to the COM pin only.

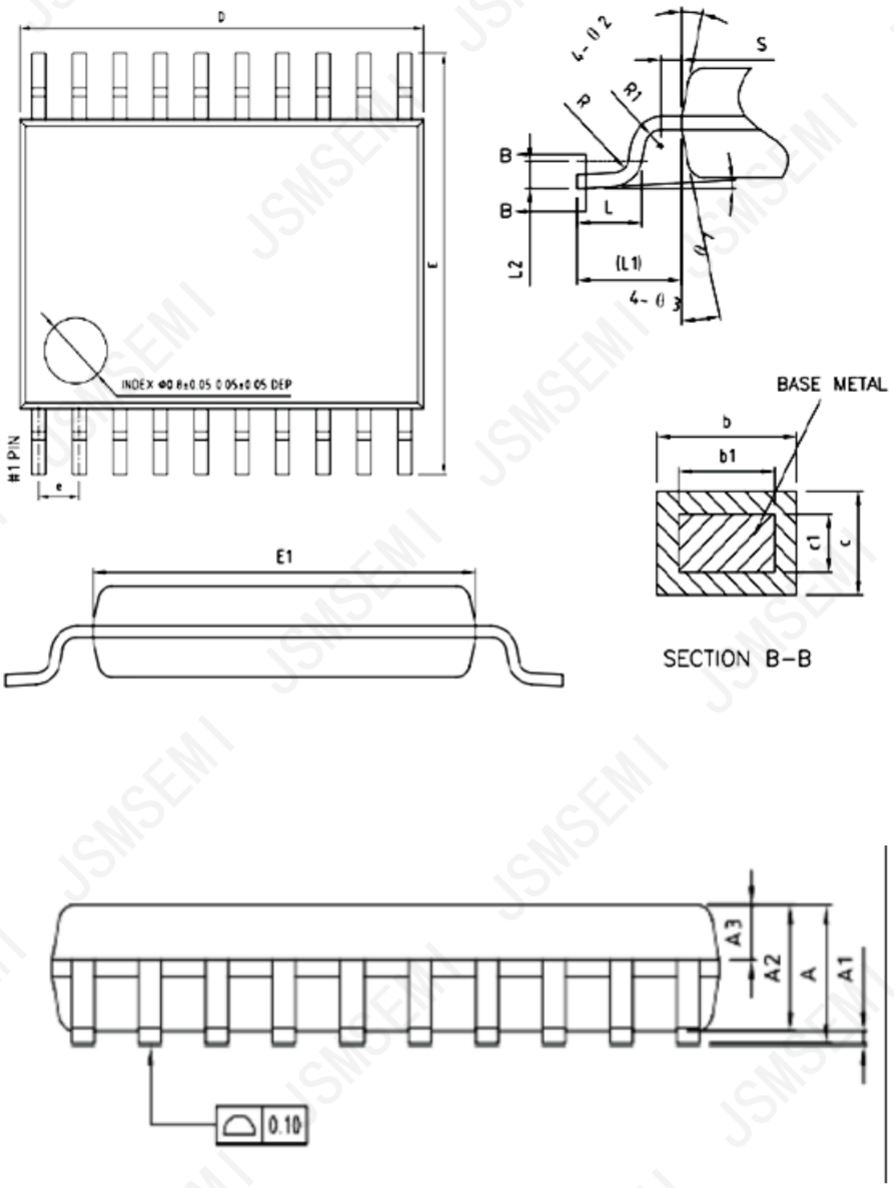
• Grounding precautions:

The primary goal of designing a ground connection is to limit the MOSFET gate charge and discharge loop to the smallest possible loop area. This method reduces the loop inductance and can effectively avoid the noise problem on the MOSFET gate. At the same time, the gate driver chip should be as close to the MOSFET as possible.

The second consideration is to ensure reasonable charging paths for bootstrap capacitors, including VCC bypass capacitors based on ground (COM), bootstrap diodes, bootstrap capacitors, and low-side MosFETs. Since the VCC bypass capacitor charges the bootstrap capacitor by cycle through the bootstrap diode, and each charge occurs in a very short period of time, this charge path passes through the peak current. Minimizing the loop length and area of the bootstrap circuit on PCB can make the bootstrap circuit work in a stable state, which is very important to ensure the reliable operation of the driver chip.

9 Package Information

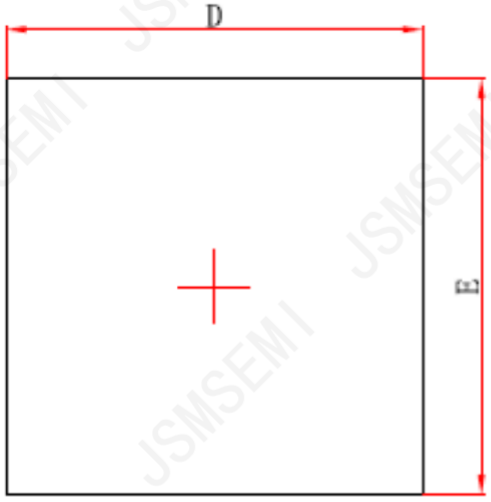
9.1 TSSOP20 Package Outlines



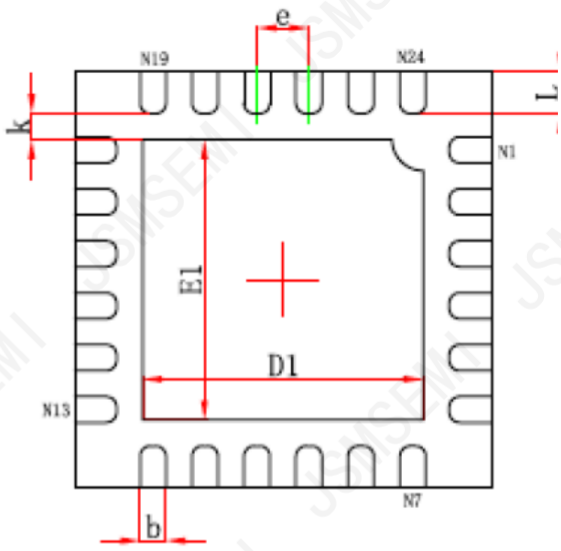
· TSSOP20 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.20	D	6.40	6.50	6.60
A1	0.05	-	0.15	E	6.20	6.40	6.60
A2	0.80	1.00	1.05	E1	4.30	4.40	4.50
b	0.19	-	0.30	e		0.65BSC	
b1	0.19	0.22	0.25	L	0.45	0.60	0.75
c	0.09	-	0.20	L1		1.00BSC	
c1	0.09	-	0.16				

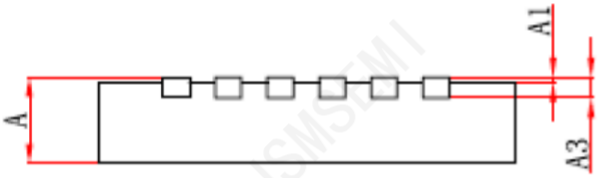
9.2 QFN24 Package Outlines



Top View



Bottom View



QFN24 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	0.700/0.800	-	0.800/0.900	E1	2.600	-	2.800
A1	0.000	-	0.050	K		0.200MN	
A3		0.203REF		B	0.200	-	0.300
D	3.924	-	4.076	e		0.500TYP	
E	3.924	-	4.076	L	0.324	-	0.476
D1	2.600	-	2.800				

Ordering Information

Orde rnumber	Package	Marking	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
JSM6288T1	TSSOP-20	JSM6288T1	-40 to 125°C	3	T&R,4000	Rohs
JSM6288Q1	QFN-24	JSM6288Q1	-40 to 125°C	3	T&R,5000	Rohs

Revision History

Rev.	Change	Date
V1.0	Initial version	2/23/2020
V1.1	Update applications and correct step errors	5/11/2021

Important Notice

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