TUSB211 USB 2.0 高速信号调节器

1 特性

- 与 USB 2.0、OTG 2.0 和 BC 1.2 兼容
- 支持低速 (LS)、全速 (FS) 和高速 (HS) 信号传输
- 3.3V 单电源供电运行时的功耗为 55mW（典型值）
- 可通过外部下拉电阻选择信号增益
- 不会损坏 DP 和 DM 走线
- 可扩展解决方案 - 用于高损耗应用的 菊花链器件
- 紧凑型 1.6mm x 1.6mm QFN 封装

2 应用

- 笔记本电脑
- 台式机
- 扩展坞
- 手机
- 有源电缆、电缆扩展器
- 背板
- 电视
- 平板电脑

3 说明

TUSB211 是一款 USB 高速 (HS) 信号调节器，专为补偿传输通道中的 ISI 信号损失而设计。

该器件采用了对 USB 低速 (LS) 和全速 (FS) 信号无感知的设计，该设计正在申请专利。LS 和 FS 信号特征不受 TUSB211 的影响。该器件只能对 HS 信号进行补偿。

该器件具有可编程的信号增益，可精调器件性能，从而对连接器上的高速信号进行优化。这对于通过 USB 高速电气兼容性测试很有帮助。

TUSB211 的封装不会损坏 DP/DM 信号路径的连续性。这样一来，便可以针对完整 USB 通道实现零风险系统设计。

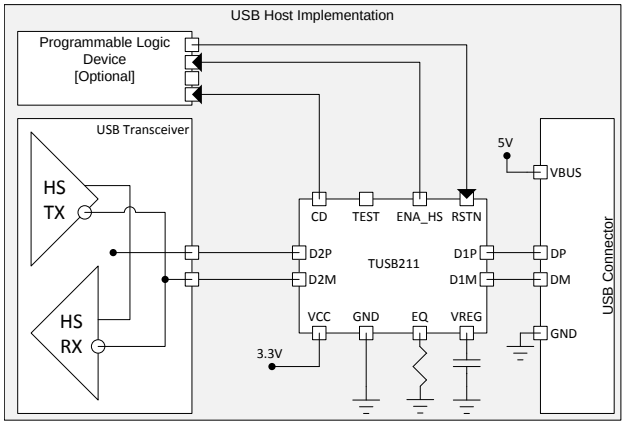
此外，TUSB211 符合 USB On-The-Go (OTG) 和电池充电 (BC) 协议。

器件信息 (1)

部件号	封装	封装尺寸（标称值）
TUSB211	X2QFN (12)	1.60mm x 1.60mm
TUSB211I		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化电路原理图



目录

4 修订历史记录

Changes from Revision C (June 2016) to Revision D **Page**

- 从产品说明书中删除了器件 TUSB211-Q1 ... 1
- 删除了*特性*：符合汽车应用 标准 ... 1
- 删除了*应用*：汽车信息娱乐系统 ... 1

Changes from Revision A (June 2015) to Revision B **Page**

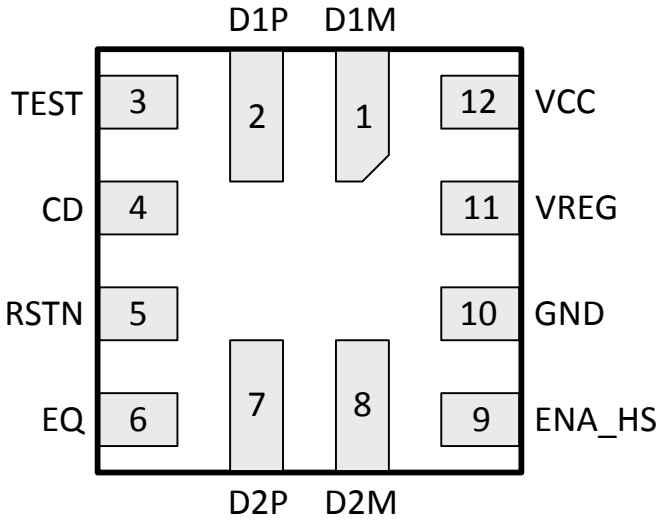
- 将 1 页产品说明书更改成了完整的产品说明书 ... 1
- 添加了*特性*：符合汽车应用 标准 ... 1
- 删除了*特性*：–40°C 至 85°C 工业温度范围 ... 1
- 添加了*应用*：汽车信息娱乐系统 ... 1
- 更改了*简化原理图* ... 1

Changes from Original (May 2015) to Revision A **Page**

- 将产品说明书从“产品预览”更改成了“生产” ... 1

5 Pin Configuration and Functions

RWB Package
12 Pin (X2QFN)
Top View



Pin Functions

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
VCC	12	P	N/A	3.3-V power
VREG	11	O	RSTN asserted: 30 kΩ PD FS, LS mode: 30 kΩ PD HS mode: N/A	1.8-V LDO output. Only enabled when operating in High Speed mode. Requires 0.1-µF external capacitor to GND to stabilize the core.
GND	10	P	N/A	Ground
RSTN	5	I	500 kΩ PU	Device disable/enable. Recommend 0.1-µF external capacitor to GND to ensure clean power on reset if not driven.
EQ	6	I	N/A	USB High Speed boost select via external pull down resistor. Sampled upon power up. Auto selects min EQ when left floating. Does not recognize real time adjustments.
D1P	2	I/O	N/A	USB High Speed positive port. Orientation independent – Can face either upstream or downstream.
D1M	1	I/O	N/A	USB High Speed negative port. Orientation independent – Can face either upstream or downstream.
D2P	7	I/O	N/A	USB High Speed positive port. Orientation independent – Can face either upstream or downstream.
D2M	8	I/O	N/A	USB High Speed negative port. Orientation independent – Can face either upstream or downstream.
TEST	3	I	RSTN asserted: 500 kΩ PD	No function. Leave floating.
ENA_HS	9	O	RSTN asserted: 500kΩ PD	Flag indicating that channel is in High Speed mode. Asserted upon: 1. Detection of USB-IF High Speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 µs – 128 µs] De-asserted upon detection of disconnect or suspend. Can be left floating if not needed.
CD	4	O	RSTN asserted: 500 kΩ PD	Flag indicating that a USB device is attached. Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect. Can be left floating if not needed.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage range	VCC	–0.3	3.8	V
Voltage range	D1P, D1M, D2P, D2M, RSTN, EQ	–0.3	3.8	V
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature [TUSB211]	0		70	°C
	Operating free-air temperature [TUSB211I]	–40		85	

6.4 Thermal Information

THERMAL METRIC (1)		RWB	UNIT
		12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	161.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
$I_{(ACTIVE\_HS)}$	High Speed Active Current	USB channel = HS mode. 480 Mbps traffic. V_{CC} supply stable		16	20	mA
$I_{(IDLE\_HS)}$	High Speed Idle Current	USB channel = HS mode. No traffic. V_{CC} supply stable		12	15	mA
$I_{(SUSPEND\_HS)}$	Suspend Current	USB channel = Suspend mode.		4.5	5.5	mA
$I_{(FS)}$	Full-Speed Current	USB channel = FS mode		4.5	5.5	mA
$I_{(LS)}$	Low-Speed Current	USB channel = LS mode		4.5	5.5	mA
$I_{(DISCONN)}$	Disconnect Power	Host side application. No device attachment.		4.5	5.5	mA
$I_{(RSTN)}$	Disable Power	RSTN driven low; V_{CC} supply stable; V_{CC} = 3.3 V		4.5	5.5	mA
RSTN						
V_{IH}	High level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
I_{IH}	High level input current	V_{IH} = 3.6 V, V_{CC} = 3 V, RPU enabled			±2	µA
I_{IL}	Low level input current	V_{IL} = 0V, V_{CC} = 3.6 V, RPU enabled			±11	µA
EQ						
$R_{(EQ)}$	External pulldown resistor	Level 0 EQ			0.32	kΩ
		Level 1 EQ	1.4		2.2	kΩ
		Level 2 EQ [MAX]	3.7		4.1	kΩ
		Level 3 EQ [MIN]	6			kΩ
CD, ENA_HS						
V_{OH}	High level output voltage	I_O = –50 µA	2.4			V
V_{OL}	Low level output voltage	I_O = 50 µA			0.4	V
DxP, DxM						
$T_{(SHRT\_GND)}$	DP, DM low voltage short circuit	DxP or DxM short circuited to GND continuously for 24 hours at T_A = 25°C only	0			V
$C_{IO(DXX)}$	Capacitance to GND	Measured with LCR meter and device powered down. 1 MHz sinusoid, 30 mVpp ripple		5		pF

(1) (1) All typical values are at V_{CC} = 3.3 V, and T_A = 25°C.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
DxP, DxM						
$F_{(BR\_DXX)}$	Bit Rate	USB channel = HS mode. 480 Mbps traffic. V_{CC} supply stable			480	Mbps
$t_{(R/F\_DXX)}$	Rise/Fall time		100			ps
CD, ENA_HS						
$t_{(EN)}$	Enable time			20		µs
$t_{(DIS)}$	Disable time			20		µs
VCC						
$t_{(STABLE)}$	V_{CC} stable before RSTN de-assertion		100			µs
$t_{(RAMP)}$	V_{CC} ramp time		0.2		100	ms

(1) (1) All typical values are at V_{CC} = 3.3 V, and T_A = 25°C.

7 Detailed Description

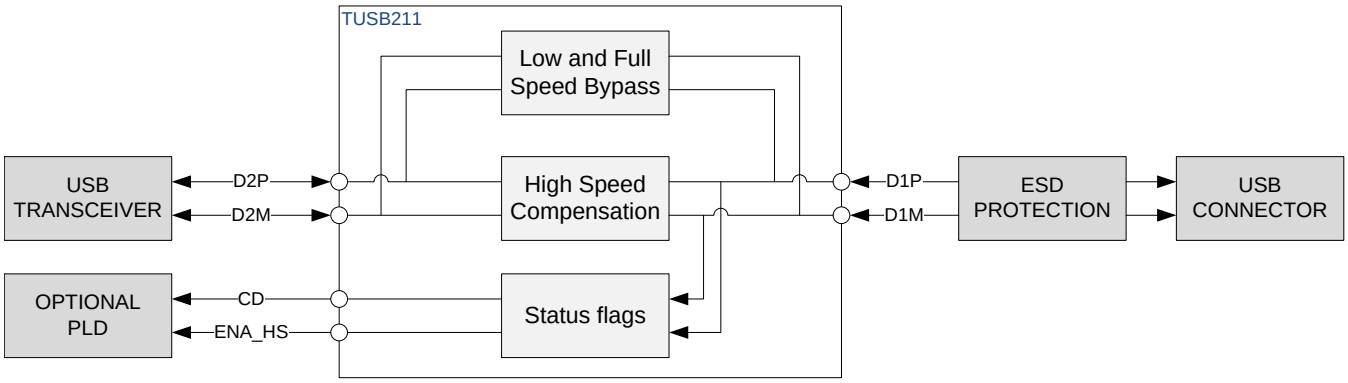
7.1 Overview

The TUSB211 is a USB High-Speed (HS) signal conditioner, designed to compensate for ISI signal loss in a transmission channel. TUSB211 has a patent-pending design which is agnostic to USB Low Speed (LS) and Full Speed (FS) signals and does not alter their signal characteristics, while HS signals are compensated. In addition, the design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals helping to pass USB HS electrical compliance tests at the connector.

The footprint of TUSB211 allows a board layout using this device such that it does not break the continuity of the DP/DM signal traces. This permits risk free system design of a complete USB channel with flexible use of one or multiple TUSB211 devices as needed for optimal signal integrity. This allows system designers to plan for this device and use it only if signal integrity analysis and/or lab measurements show a need. If such a need is not warranted, the device can be left unpopulated without any board rework.

7.2 Functional Block Diagram



7.3 Device Functional Modes

7.3.1 Low Speed (LS) Mode

TUSB211 automatically detects a LS connection and does not enable signal compensation. CD pin is asserted high.

7.3.2 Full Speed (FS) Mode

TUSB211 automatically detects a FS connection and does not enable signal compensation. CD pin is asserted high.

7.3.3 High Speed (HS) Mode

TUSB211 automatically detects a HS connection and enables signal compensation as determined by the configuration of the external pulldown resistance on its EQ pin. ENA_HS pin asserted high in addition to the CD pin.

7.3.4 Disable Mode

TUSB211 can be disabled when its RSTN pin is asserted low. The USB channel is still fully operational, but there is neither signal compensation, nor any indication from the CD pin or ENA_HS pin as to the status of the channel.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The primary purpose of the TUSB211 is to re-store the signal integrity of a USB High Speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB211 can help to pass this eye mask.

A secondary purpose is to use the CD pin and ENA_HS pin of the TUSB211 to control other blocks on the customer platform if so desired.

8.2 Typical Application

A typical application is shown below. In this setup, D1P and D1M face the USB connector while D2P and D2M face the USB transceiver. If desired, the orientation may be reversed [that is, D1 faces transceiver and D2 faces connector].

Note that CD and ENA_HS are connected to PLDs. This is for platforms where other circuit blocks must be modified based on the status of the USB channel. They could also be connected to LEDs to give a physical indication of current channel status for debug purposes. If neither use is desired, they can be left floating.

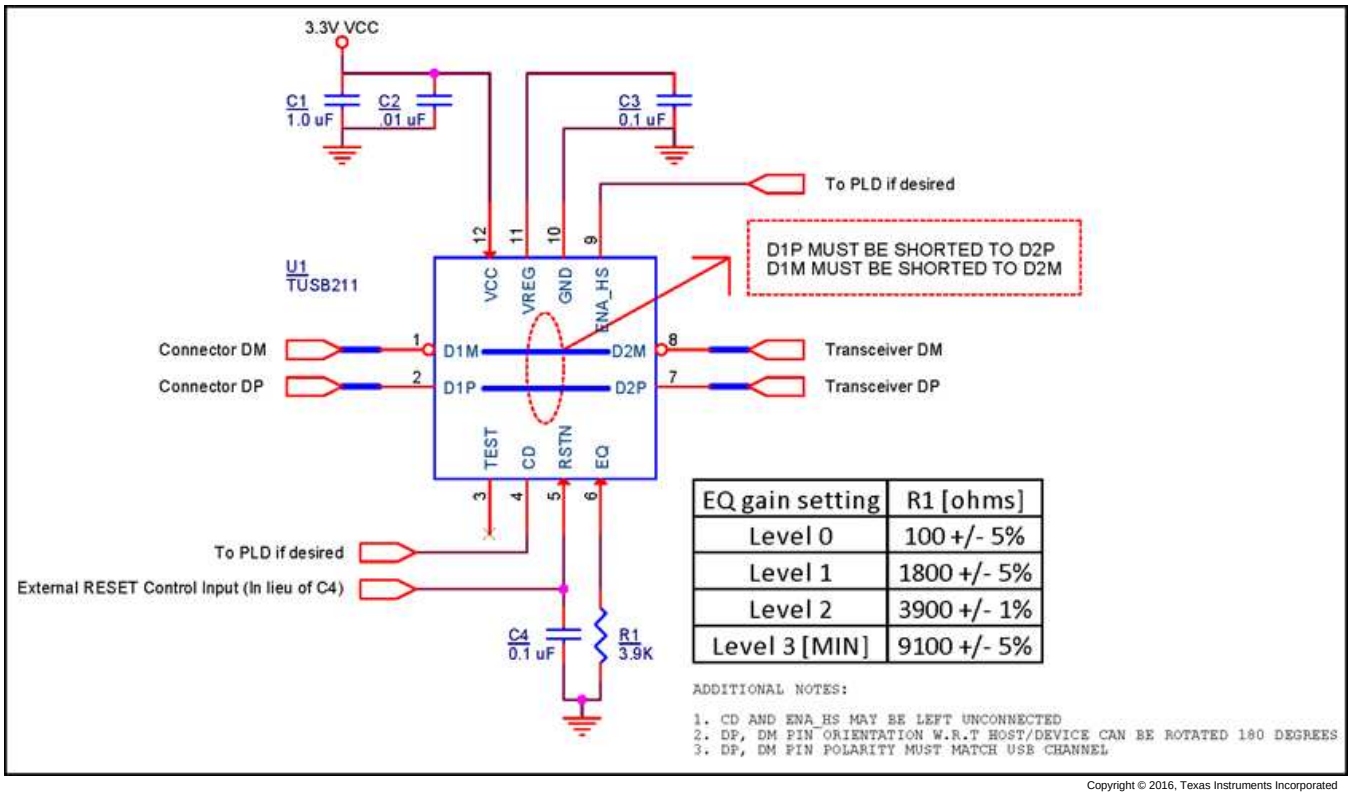


图 1. Reference Schematic

Typical Application (接下页)

8.2.1 Design Requirements

TUSB211 requires a valid reset signal as described in the power supply recommendations section. The capacitor C4 is not required if a microcontroller drives the RSTN pin according to recommendations.

Pin 11 VREG is an internal LDO output that requires a 0.1 μF external capacitor to GND to stabilize the core.

Pin 6 EQ requires an external pulldown resistor if EQ levels 0-2 are needed. If EQ level 3 is needed, then the EQ pin can be left floating.

8.2.2 Detailed Design Procedure

The ideal EQ setting is dependent upon the signal chain loss characteristics of the target platform. The general recommendation is to start with EQ level 0, and then increment to EQ level 1, and so on. if permissible.

In order for the TUSB211 to recognize any change to the EQ setting, the RSTN pin must be toggled. This is because the EQ pin is latched on power up and the pin is ignored thereafter.

In addition, TUSB211 does not compensate for any DC attenuation in the signal path. Therefore, minimizing DC loss (that is, resistance) in the system design, is suggested. As a consequence, this might lead to increased line capacitance. This is acceptable because the TUSB211 can compensate for the additional capacitive load.

Placement of the device is also dependent on the application goal. 表 1 summarizes the recommendations.

表 1. TUSB211 Platform Placement Guideline

PLATFORM GOAL	SUGGESTED TUSB211 PLACEMENT
Pass USB Near End Mask	Close to measurement point
Pass USB Far End Eye Mask	Close to USB PHY
Cascade multiple 211s to improve device enumeration	Midway between each USB interconnect

注

USB-IF certification tests for High Speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the 'Electricals' section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High Speed Eye Mask:

8.2.2.1 For a Host Side Application

1. Configure the TUSB211 to the desired EQ setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB211
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB211
4. Enable the host to transmit USB TEST_PACKET
5. Execute the oscilloscope's USB compliance software.
6. Repeat the above steps in order to re-test TUSB211 with a different EQ setting

8.2.2.2 For a Device Side Application

1. Configure the TUSB211 to the desired EQ setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB211
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB211. Ensure that the USB-IF device test fixture is configured to the 'INIT' position
4. Allow the host to enumerate the device
5. Enable the device to transmit USB TEST_PACKET
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the 'TEST' position.
7. Execute the oscilloscope's USB compliance software.
8. Repeat the above steps in order to re-test TUSB211 with a different EQ setting

8.2.3 Application Curves

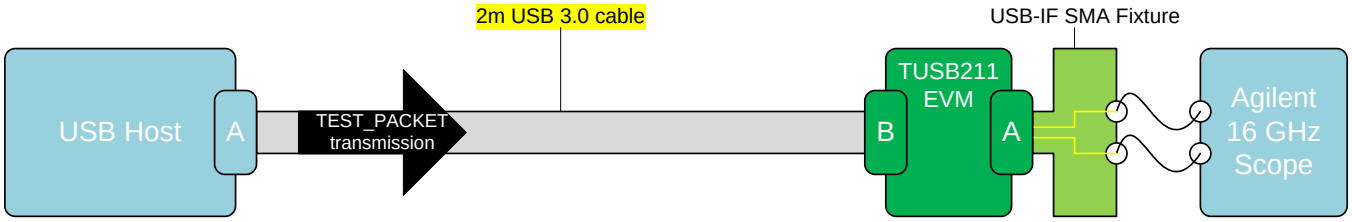


图 2. Eye Diagram Bench Setup

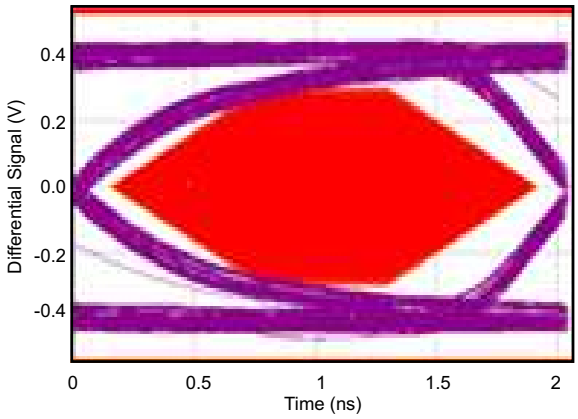


图 3. TUSB211 Disabled

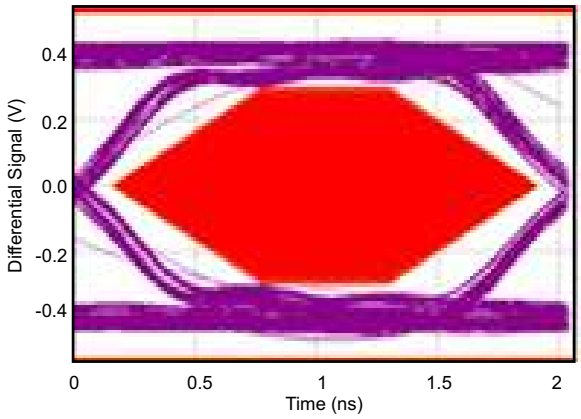


图 4. EQ Level 0

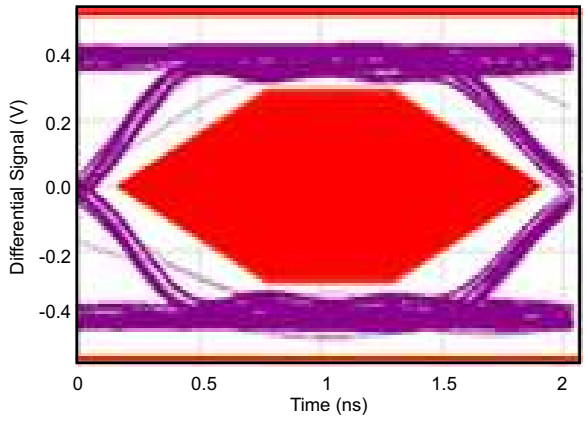


图 5. EQ Level 1

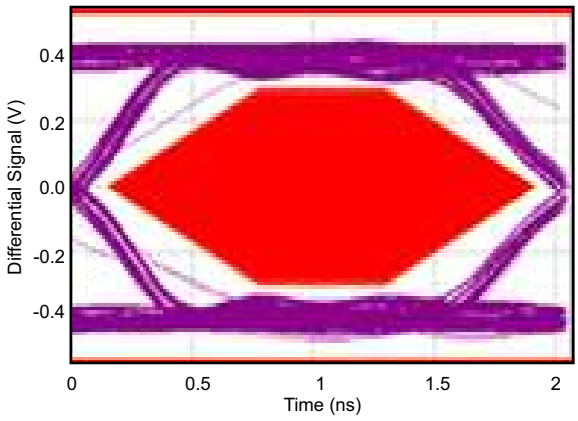


图 6. EQ Level 2

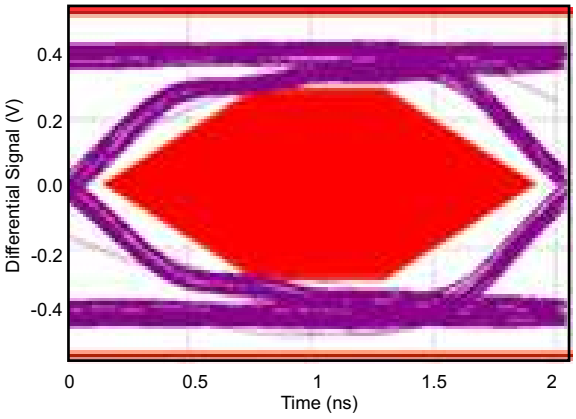


图 7. EQ Level 3

9 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to 3 V or higher to guarantee a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to V_{CC}). With a typical internal pullup resistance of 500 kΩ, the recommended minimum external capacitance is calculated as:

[Ramp Time x 5] ÷ [500 kΩ] (1)

10 Layout

10.1 Layout Guidelines

There is no need to break the USB signal trace. Thus, even with the TUSB211 powered down, or not populated, the USB link is still fully operational. To avoid the need for signal vias, routing the High Speed traces directly underneath the TUSB211 package, as illustrated in the PCB land pattern shown in 图 8, is recommended.

Although the land pattern shown below has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. It is recommended to maintain 90 Ω differential routing underneath the device.

All dimensions are in millimetres (mm).

10.2 Layout Example

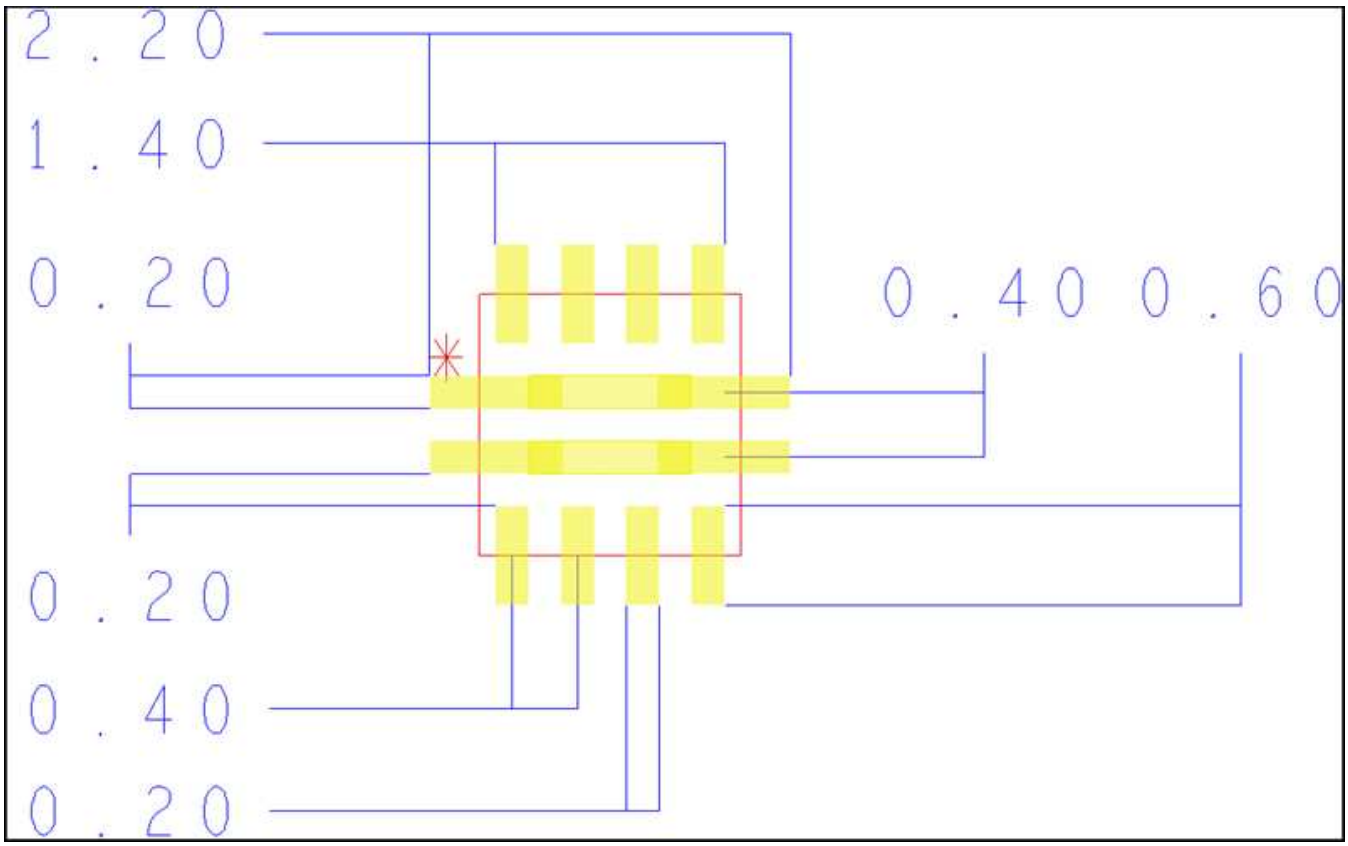


图 8. DP and DM Routing Underneath Device Package

11 器件和文档支持

11.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及立即订购快速访问。

表 2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TUSB211	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TUSB211I	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB211IRWBR	NRND	Production	X2QFN (RWB) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	I1
TUSB211RWBR	NRND	Production	X2QFN (RWB) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	C1

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

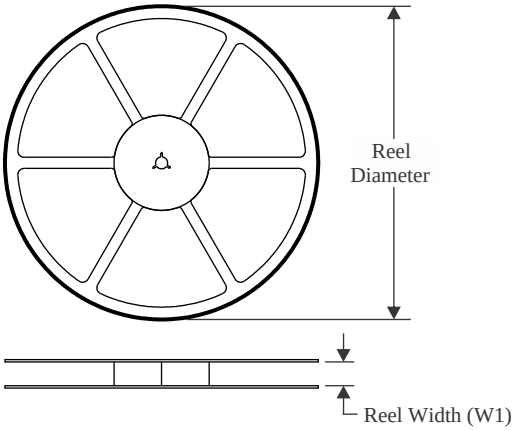
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

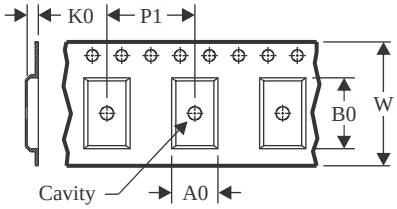
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

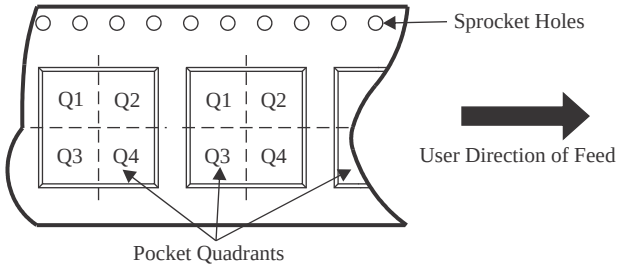


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

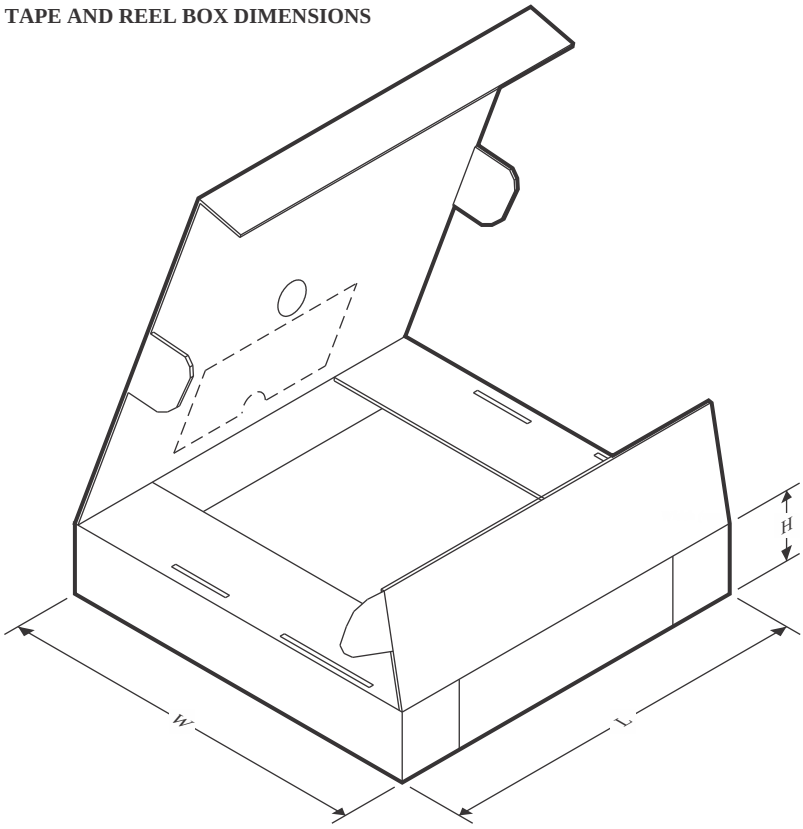
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB211IRWBR	X2QFN	RWB	12	3000	180.0	8.4	1.8	1.8	0.48	4.0	8.0	Q2
TUSB211RWBR	X2QFN	RWB	12	3000	180.0	8.4	1.8	1.8	0.61	4.0	8.0	Q2
TUSB211RWBR	X2QFN	RWB	12	3000	180.0	8.4	1.8	1.8	0.48	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

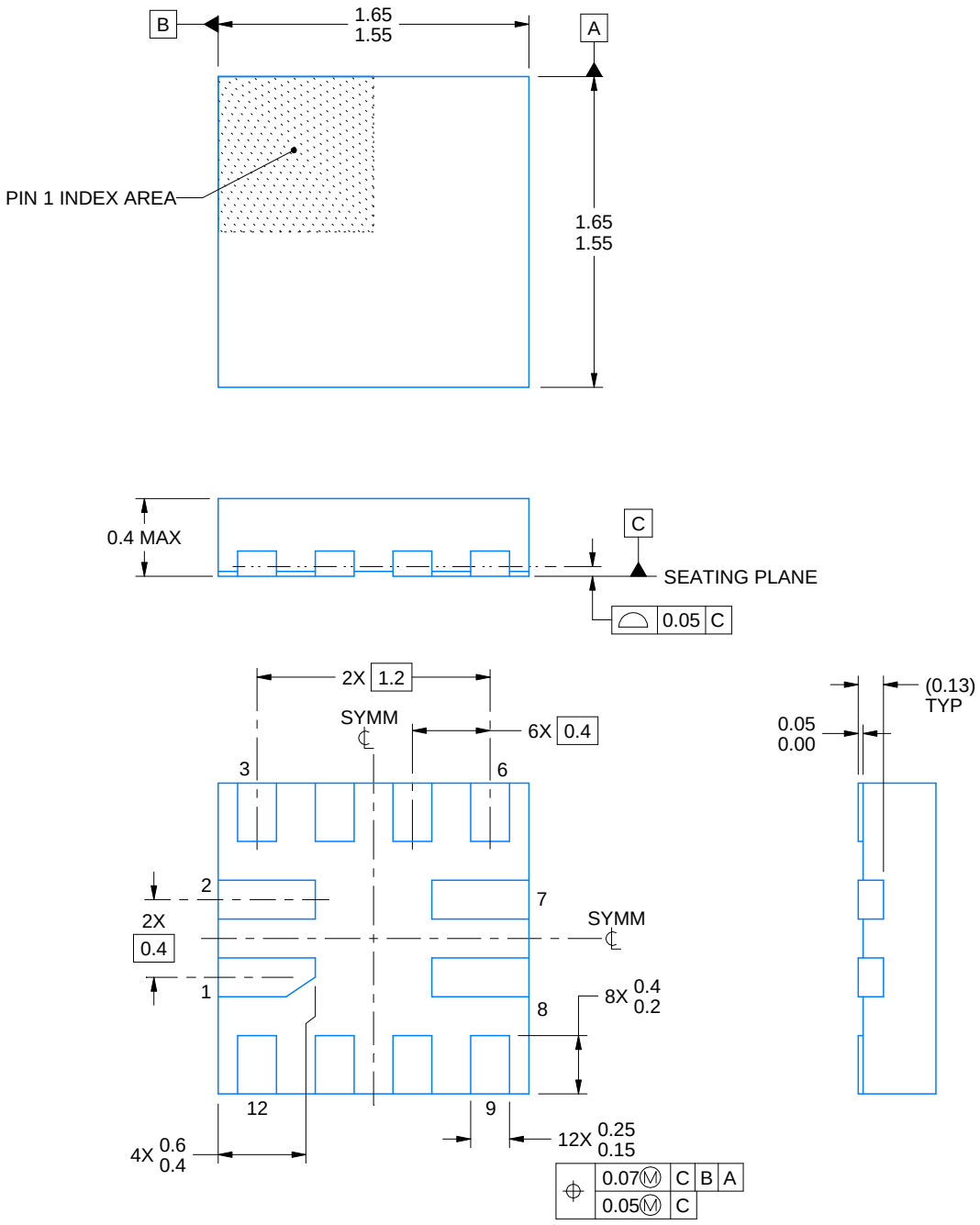
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB211IRWBR	X2QFN	RWB	12	3000	210.0	185.0	35.0
TUSB211RWBR	X2QFN	RWB	12	3000	213.0	191.0	35.0
TUSB211RWBR	X2QFN	RWB	12	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RWB0012A

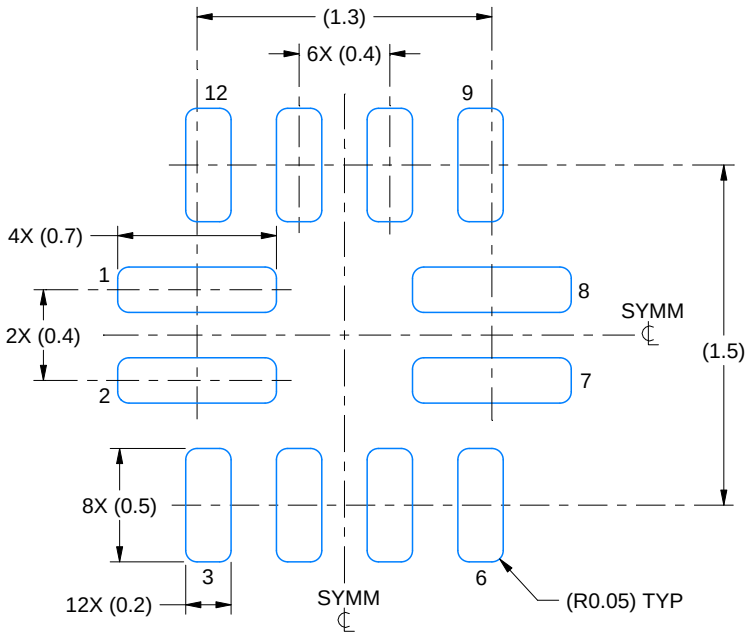
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

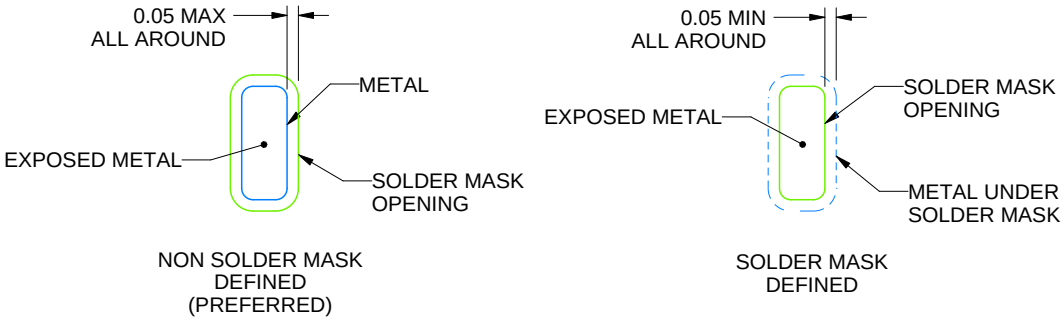


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

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NOTES: (continued)

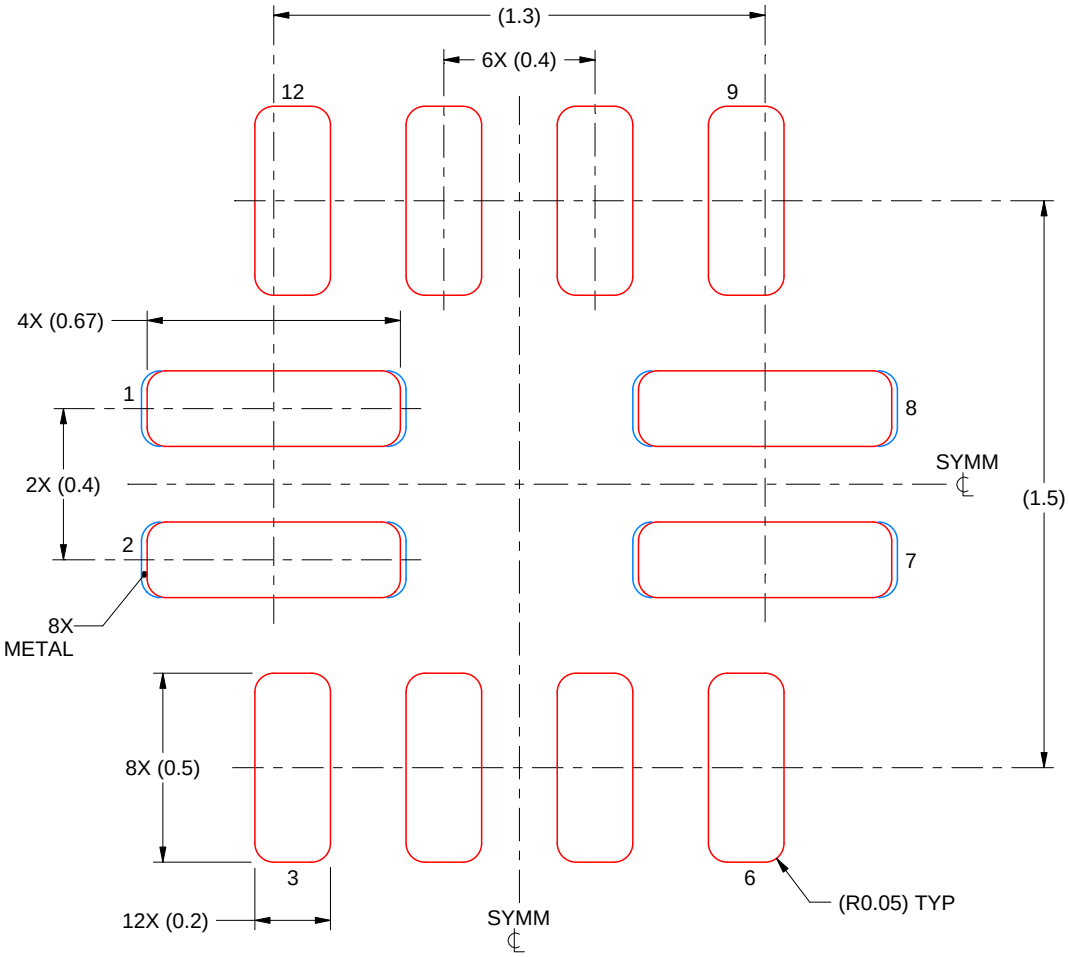
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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