

SNx4LV02A Quadruple 2-Input Positive-NOR Gates

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
 > 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^{\circ}\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Live insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 200-V Machine Model
 - 1000-V Charged-Device Model

2 Applications

- Handset: Smartphone
- Network Switch
- Health & Fitness / Wearables
- PDAs
- TV (LCD)
- Power Infrastructure

3 Description

The SNx4LV02A devices are quadruple 2-input positive-NOR gates designed for 2-V to 5.5-V V_{CC} operation.

The SNx4LV02A devices perform the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4LV02A	VQFN (14)	3.50 mm x 3.50 mm
	SOIC (14)	8.65 mm x 3.91 mm
	SOP (14)	10.30 mm x 5.30 mm
	SSOP (14)	6.20 mm x 5.30 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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5 Revision History

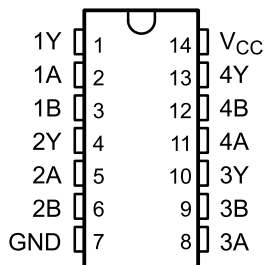
Changes from Revision I (April 2005) to Revision K

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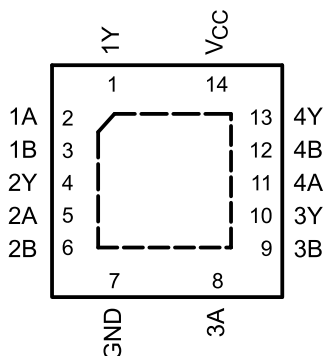
- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. **1**

6 Pin Configuration and Functions

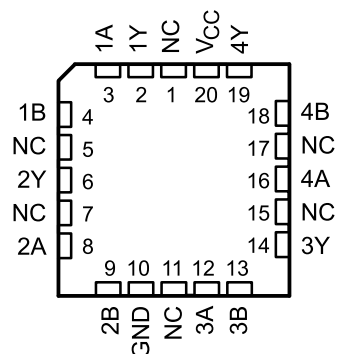
**SN54LV02A . . . J OR W PACKAGE
SN74LV02A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)**



**SN74LV02A . . . RGY PACKAGE
(TOP VIEW)**



**SN54LV02A . . . FK PACKAGE
(TOP VIEW)**



NC - No internal Connection

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	1Y	O	1Y output
2	1A	I	1A input
3	1B	I	1B input
4	2Y	O	2Y output
5	2A	I	2A input
6	2B	I	2B input
7	GND	—	GND
8	3A	I	3A input
9	3B	I	3B input
10	3Y	O	3Y output
11	4A	I	4A input
12	4B	I	4B input
13	4Y	O	4Y output
14	V _{CC}	—	V _{CC}

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	7	V
V_I	Input voltage range ⁽²⁾	–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	7	V
V_O	Output voltage range ⁽²⁾⁽³⁾	–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	–20	mA
I_{OK}	Output clamp current	$V_O < 0$	–50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	±25	mA
	Continuous current through V_{CC} or GND		±50	mA
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1500
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±2000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN54LV02A ⁽²⁾		SN74LV02A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	5.5	0	5.5	V
I _{OH}	High-level output current	V _{CC} = 2 V		–50		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2		–2	
		V _{CC} = 3 V to 3.6 V		–6		–6	
		V _{CC} = 4.5 V to 5.5 V		–12		–12	
I _{IH}	Low-level output current	V _{CC} = 2 V		50		50	mA
		V _{CC} = 2.3 V to 2.7 V		2		2	
		V _{CC} = 3 V to 3.6 V		6		6	
		V _{CC} = 4.5 V to 5.5 V		12		12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V _{CC} = 3 V to 3.6 V		100		100	
		V _{CC} = 4.5 V to 5.5 V		20		20	
T _A	Operating free-air temperature		–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

(2) Product Preview.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV02A						UNIT
		D	DB	DGV	NS	PW	RGY	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	97.5	109.5	133.3	92.2	125.1	59.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	58.7	62.1	55.6	49.8	53.7	72.5	
R _{θJB}	Junction-to-board thermal resistance	51.8	56.9	66.3	51.0	66.9	35.0	
ψ _{JT}	Junction-to-top characterization parameter	22.6	22.6	7.8	15.7	7.6	3.9	
ψ _{JB}	Junction-to-board characterization parameter	51.6	56.3	56.6	50.6	66.3	35.1	
R _{θJC(bot)}		–	–	–	–	–	15.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

SN54LV02A, SN74LV02A

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7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV02A ⁽¹⁾			–40°C to 85°C SN74LV02A		–40°C to 125°C SN74LV02A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OL} = –50 µA	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1		V _{CC} – 0.1		
	I _{OL} = –2 mA	2.3 V	2			2		2		
	I _{OL} = –6 mA	3 V	2.48			2.48		2.48		
	I _{OL} = –12 mA	4.5 V	3.8			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	2 V to 5.5 V			0.1		0.1		0.1	V
	I _{OL} = 2 mA	2.3 V			0.4		0.4		0.4	
	I _{OL} = 6 mA	3 V			0.44		0.44		0.44	
	I _{OL} = 12 mA	4.5 V			0.55		0.55		0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±1		±1		±1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5			20		20		20	µA
I _{off}	V _I or V _O = 0 to 5.5 V	0			5		5		5	µA
C _i	V _I = V _{CC} or GND	3.3 V		1.6			1.6		1.6	pF

(1) Product Preview.

7.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV02A		–40°C to 85°C SN74LV02A		–40°C to 125°C SN74LV02A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	C _L = 15 pF		8.3 ⁽¹⁾	12.4 ⁽¹⁾	1 ⁽¹⁾	15 ⁽¹⁾	1	15	1	17.5	ns
			C _L = 50 pF		11 ⁽¹⁾	16.1 ⁽¹⁾	1	19	1	19	1	21.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV02A		–40°C to 85°C SN74LV02A		–40°C to 125°C SN74LV02A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	C _L = 15 pF		5.6 ⁽¹⁾	7.9 ⁽¹⁾	1 ⁽¹⁾	9.5 ⁽¹⁾	1	9.5	1	11.5	ns
			C _L = 50 pF		7.6 ⁽¹⁾	11.4 ⁽¹⁾	1	13	1	13	1	15	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV02A		–40°C to 85°C SN74LV02A		–40°C to 125°C SN74LV02A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	C _L = 15 pF		3.9 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	1	8	ns
			C _L = 50 pF		5.3 ⁽¹⁾	7.5 ⁽¹⁾	1	8.5	1	8.5	1	10	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.9 Noise Characteristics⁽¹⁾

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	SN74LV02A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		–0.1	–0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		3.2		V
$V_{IH(D)}$ High-level dynamic input voltage	2.31			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

7.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	8.9	pF
		5 V	3	

7.11 Typical Characteristics

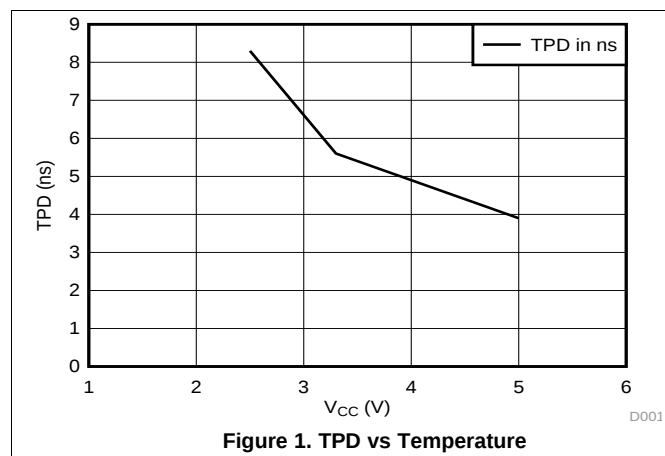


Figure 1. TPD vs Temperature

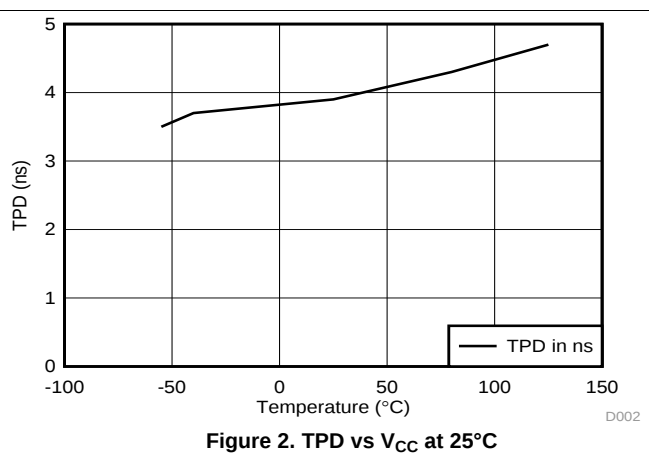
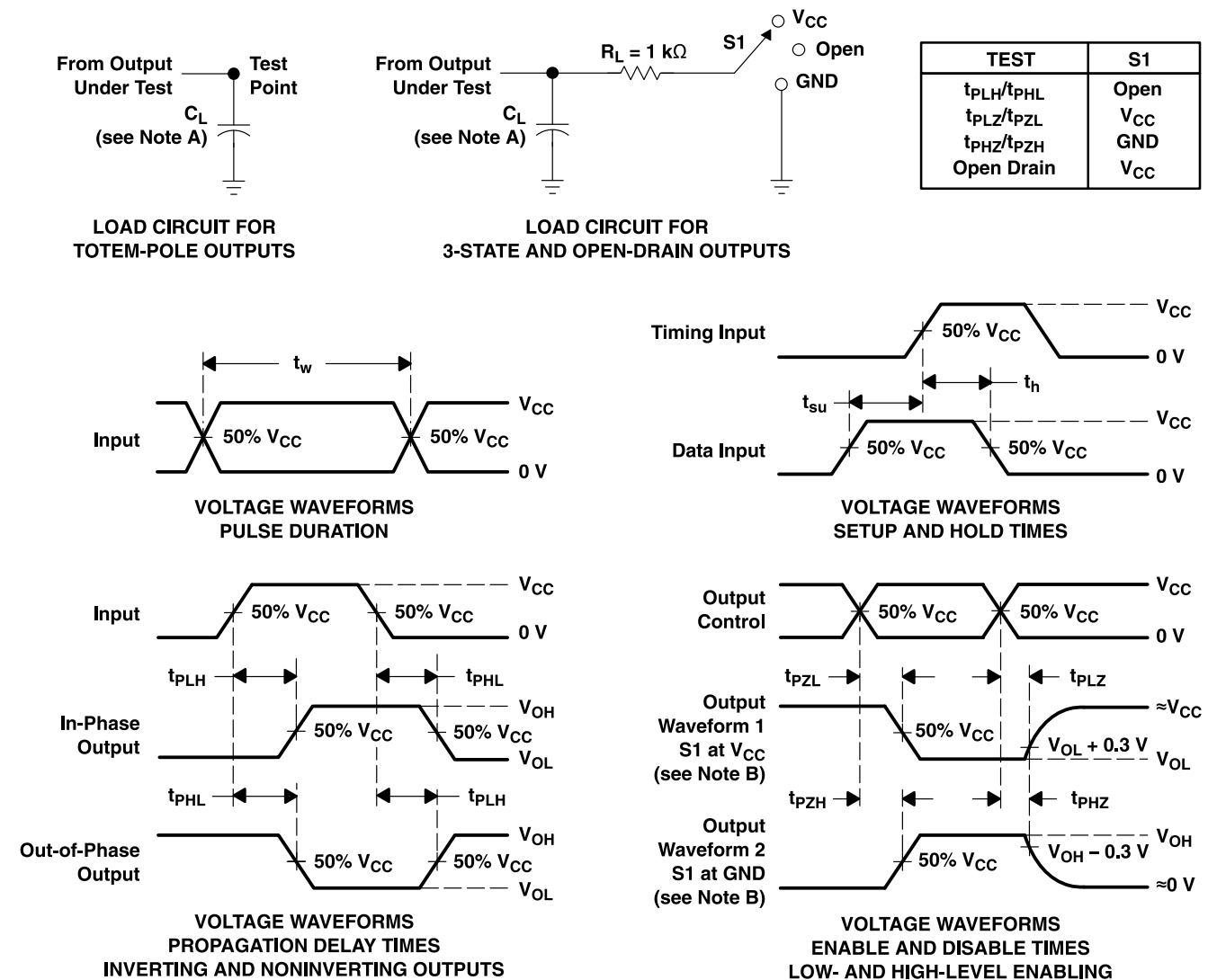


Figure 2. TPD vs V_{CC} at 25°C

8 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74LV02A devices are quadruple 2-input positive-NOR gates designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV02A devices perform the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

9.2 Functional Block Diagram



Figure 4. Logic Diagram (Positive Logic)

9.3 Feature Description

- Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down voltage translation
 - Inputs accept voltages to 5.5 V
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V

9.4 Device Functional Modes

**Table 1. Function Table
(Each Gate)**

INPUT		OUTPUT Y
A	B	
H	X	L
X	H	L
L	L	H

NOTE

Typical Application (continued)

10.2.3 Application Curves

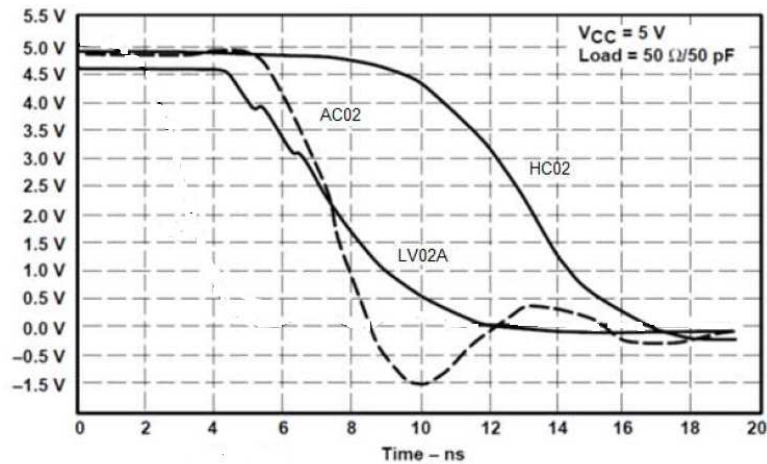


Figure 6. Typical Application Curve

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended and if there are multiple V_{CC} terminals then .01 μF or .022 μF capacitor is recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally OK to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

12.2 Layout Example

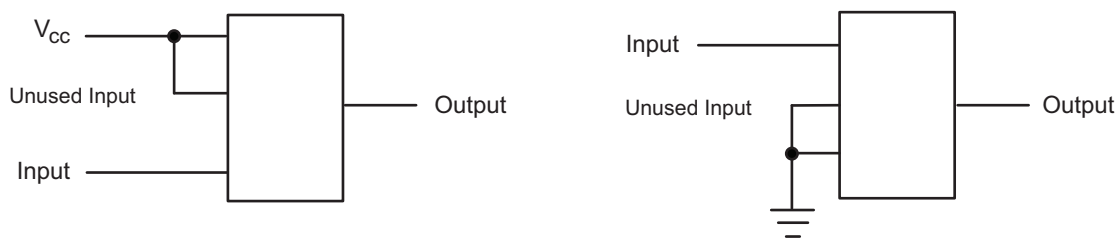


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV02A	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV02AD	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 125	LV02A
SN74LV02ADBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV02A
SN74LV02ADGVR	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV02A
SN74LV02ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV02A
SN74LV02ANSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV02A
SN74LV02APW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	LV02A
SN74LV02APWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV02A
SN74LV02APWT	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	LV02A
SN74LV02ARGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV02A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

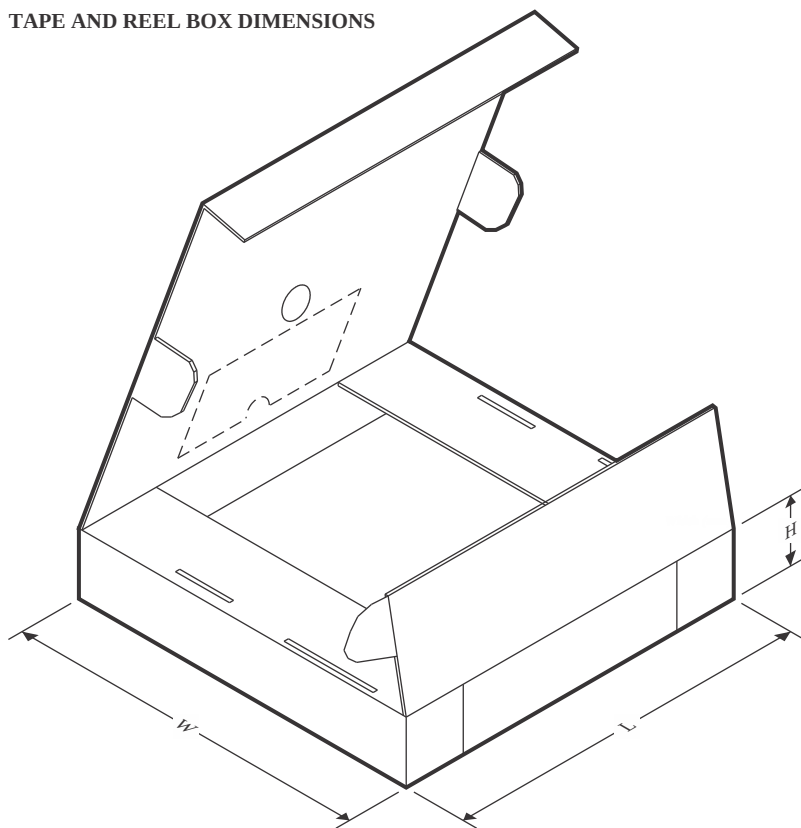
TAPE AND REEL INFORMATION



*All dimensions are nominal

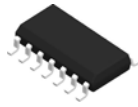
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV02ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV02ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV02ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV02ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV02APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV02ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

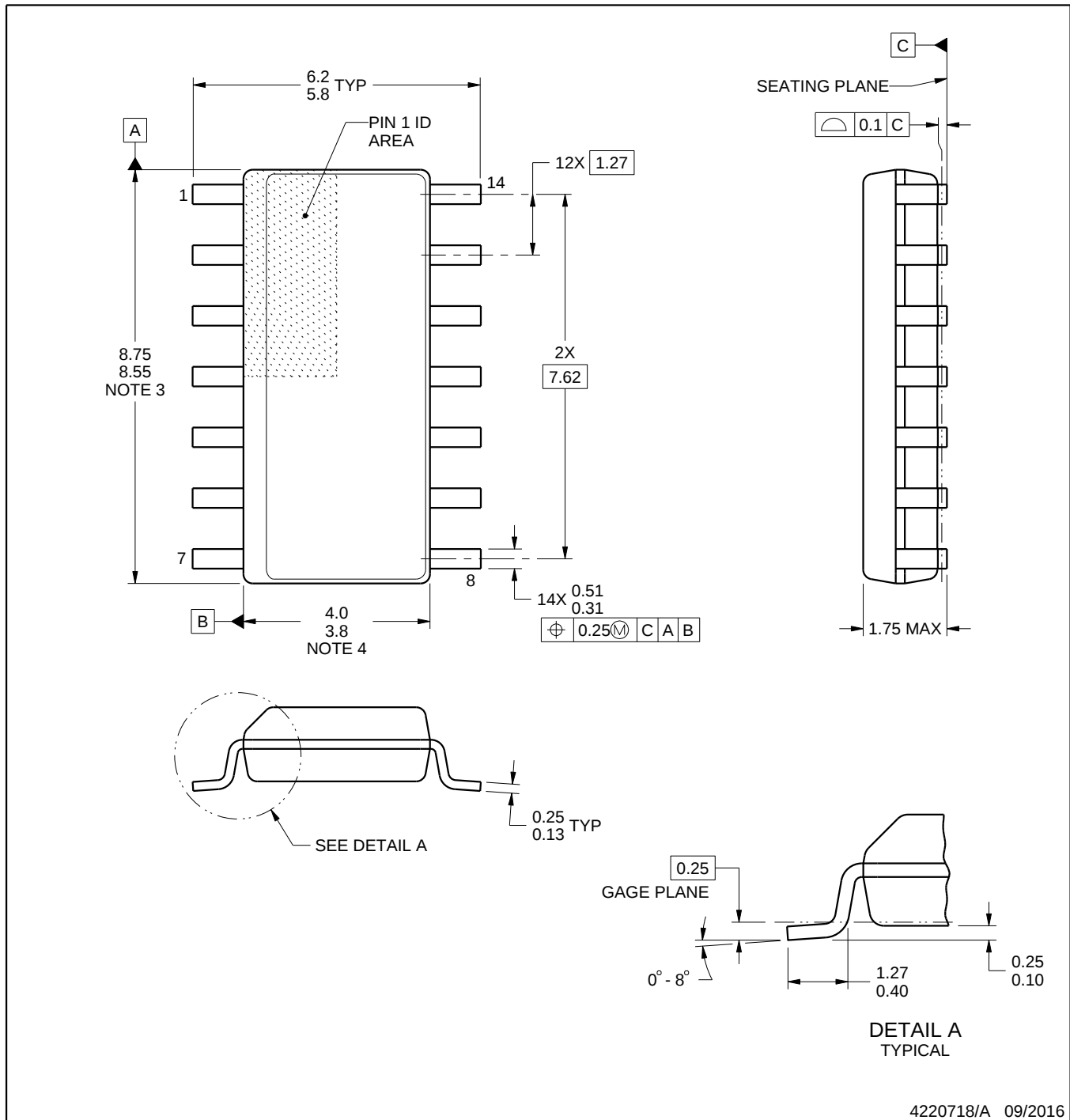


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV02ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV02ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV02ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV02ANSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74LV02APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV02ARGYR	VQFN	RGY	14	3000	360.0	360.0	36.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

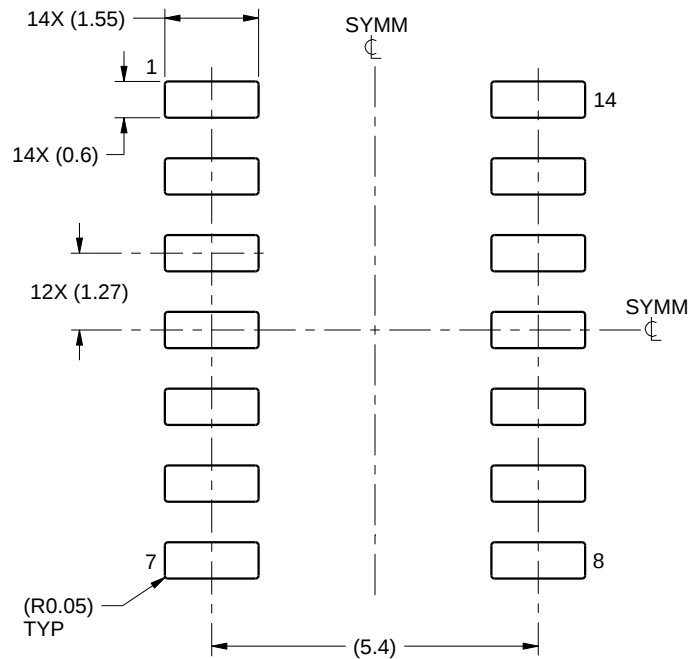
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

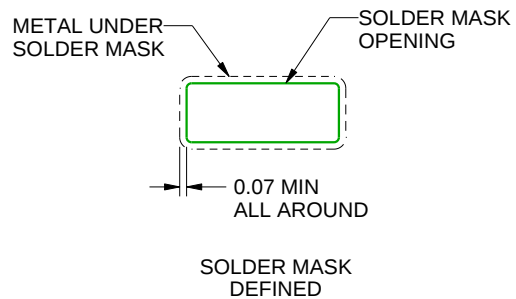
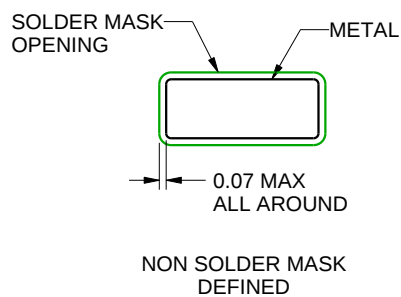
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

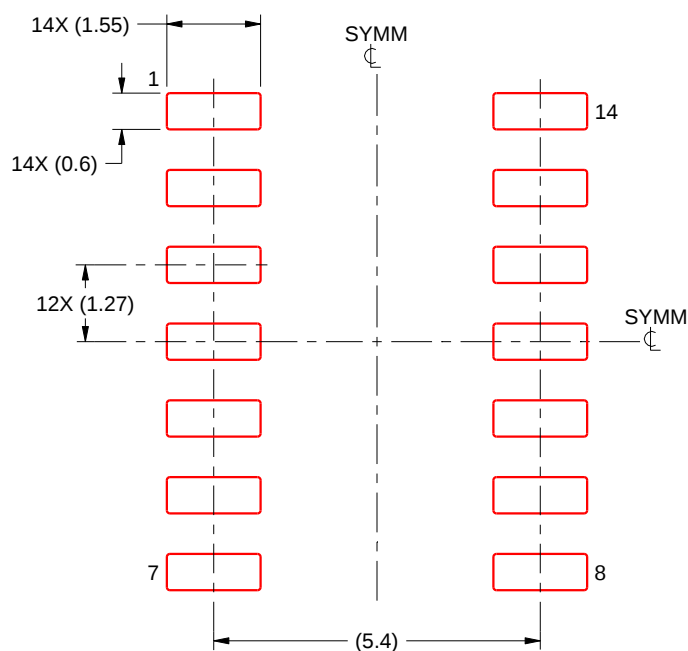
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

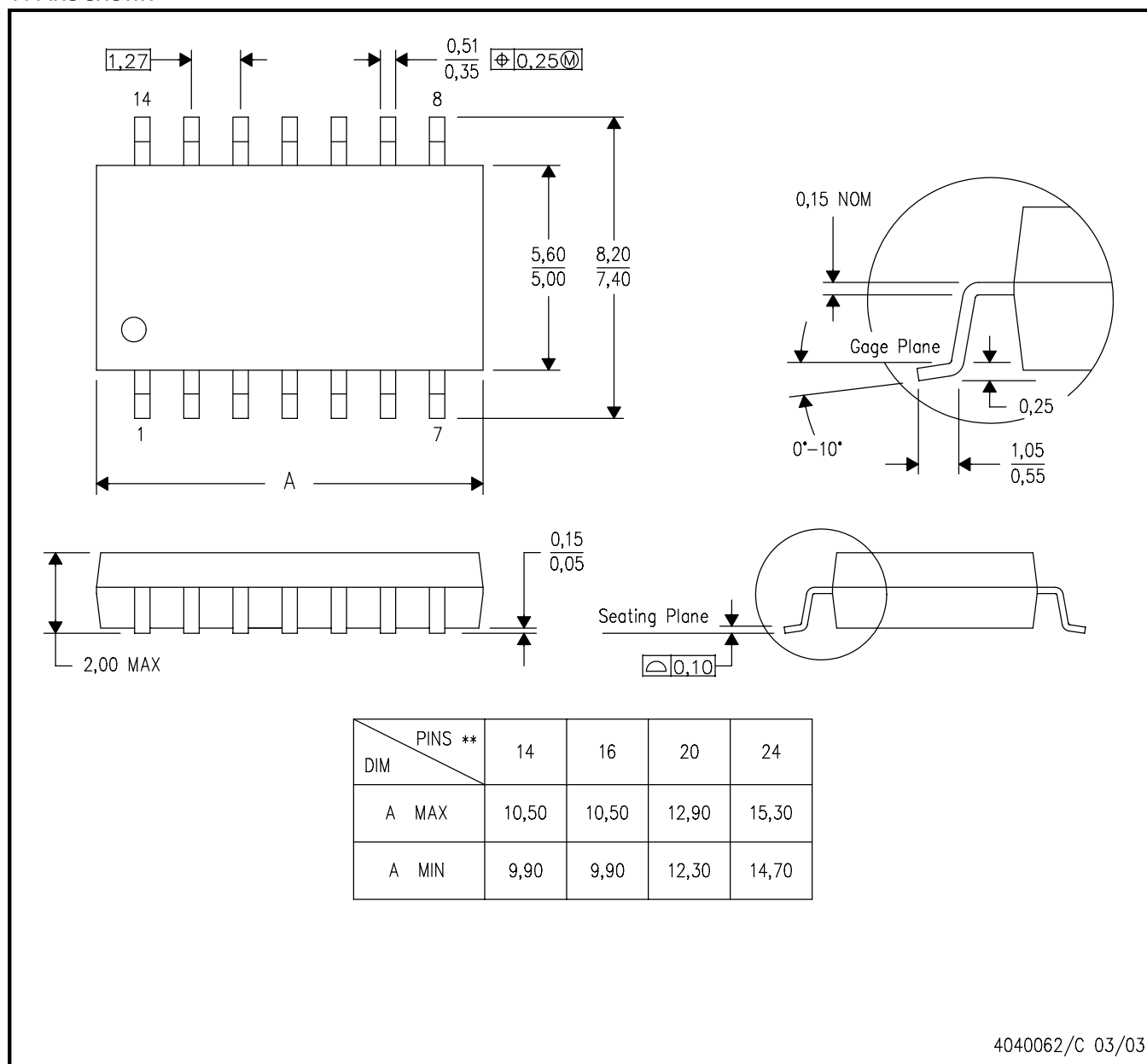
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

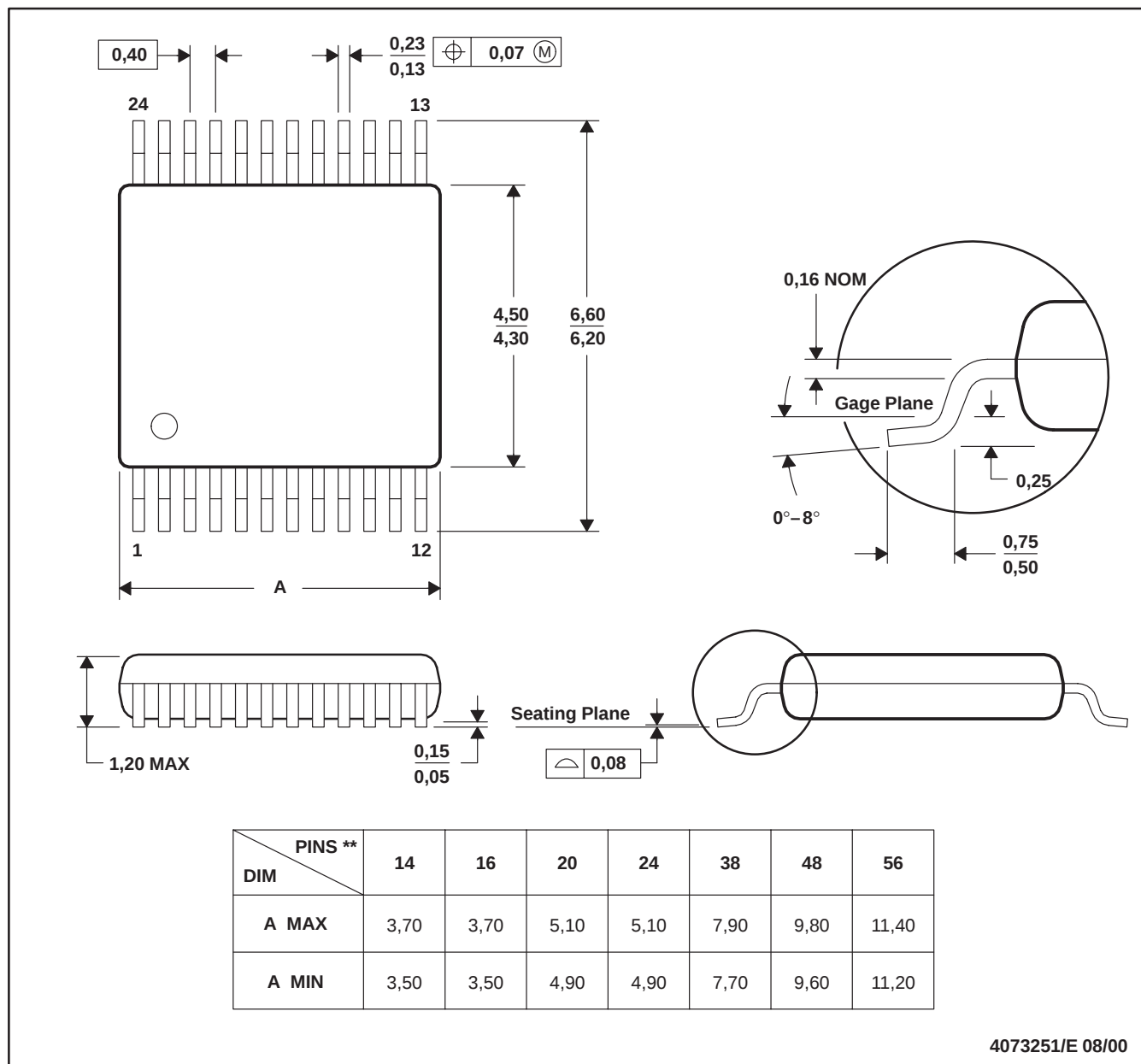


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

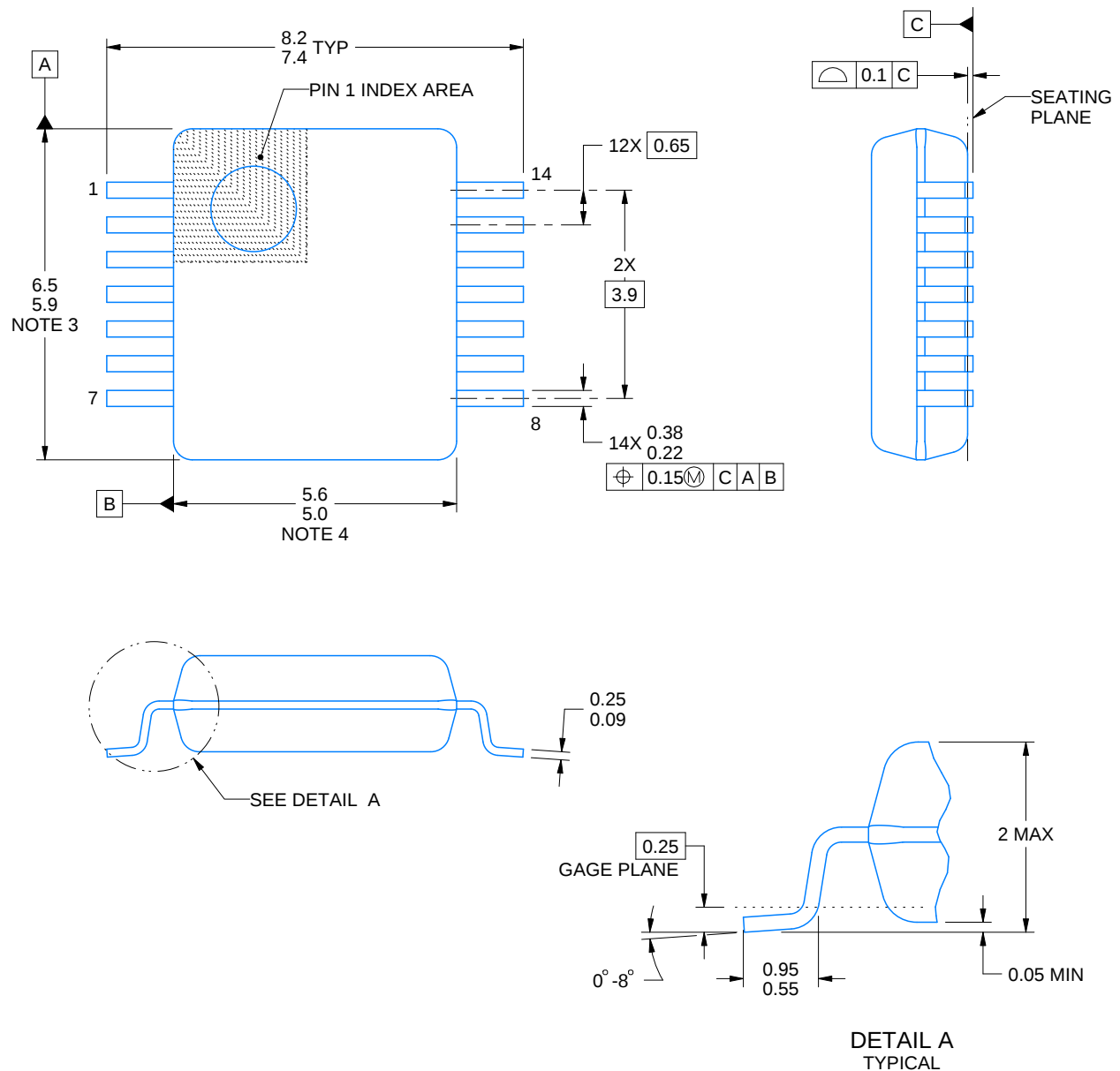
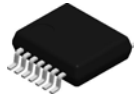
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4220762/A 05/2024

NOTES:

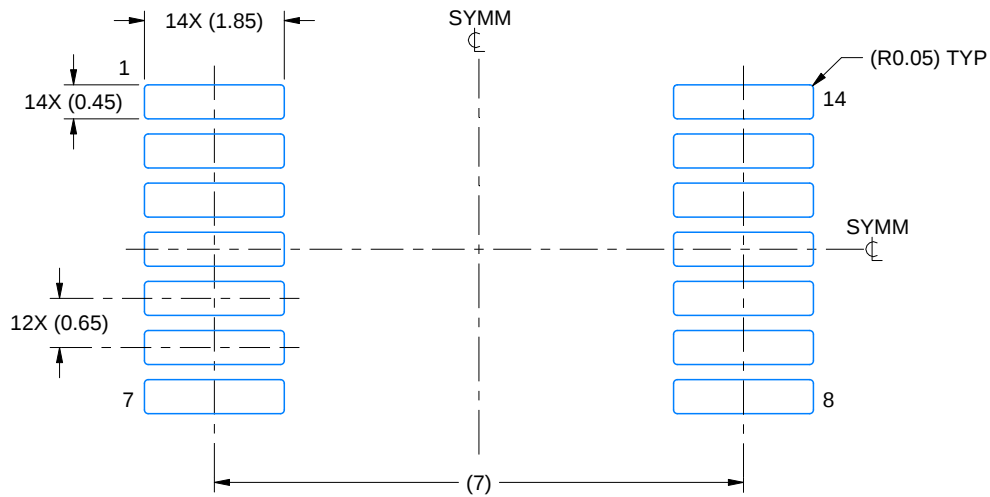
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

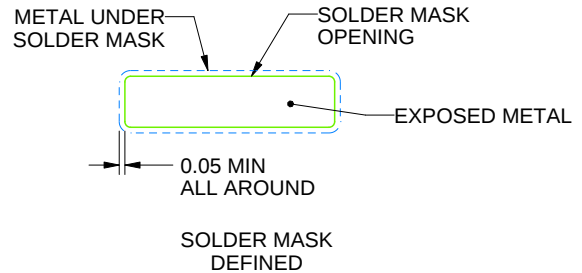
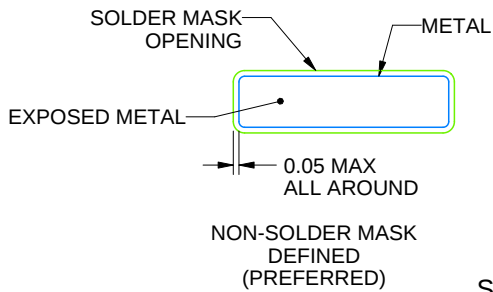
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



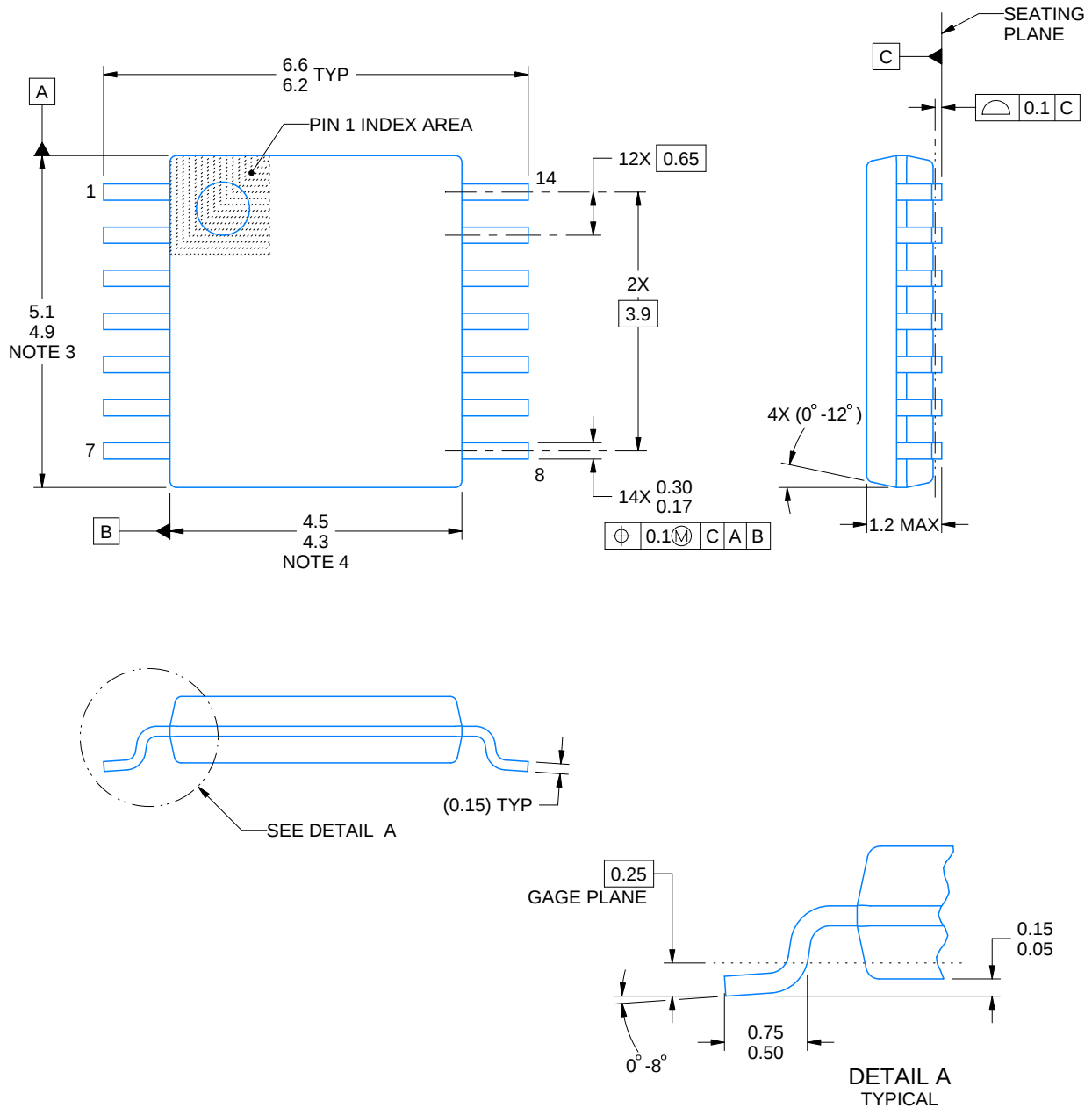
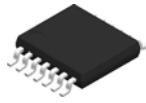
SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



4220202/B 12/2023

NOTES:

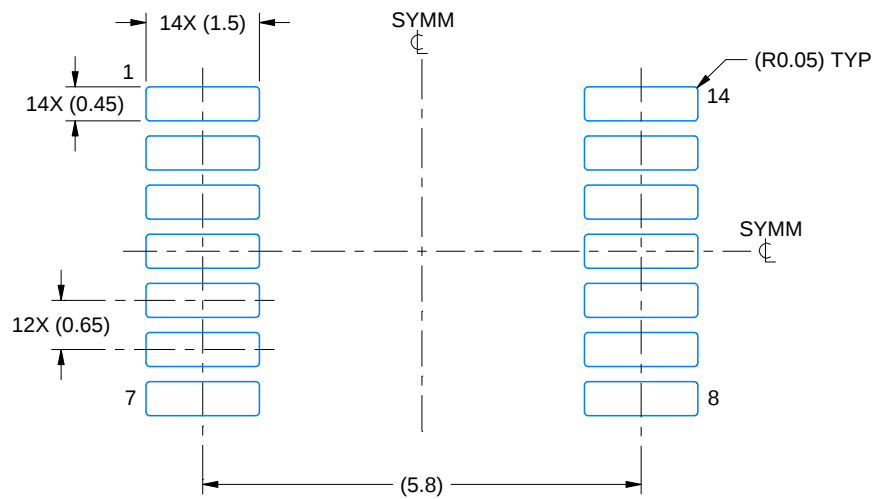
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

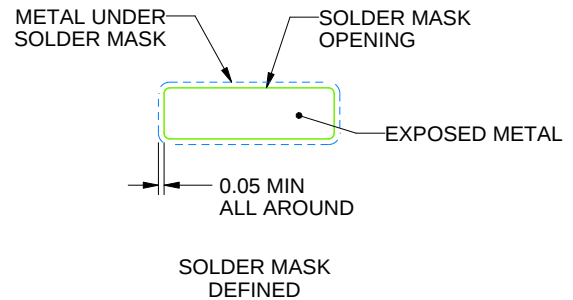
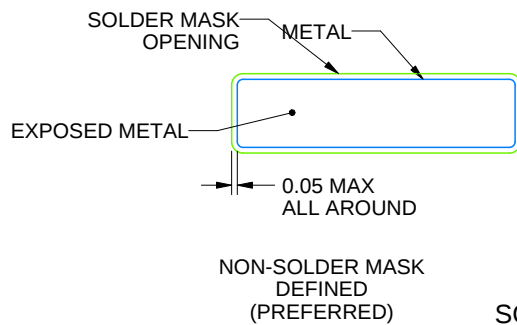
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

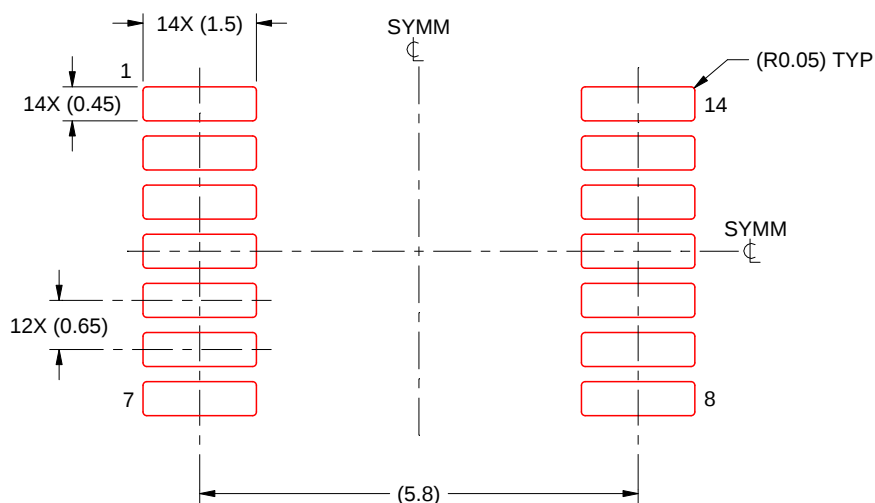
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

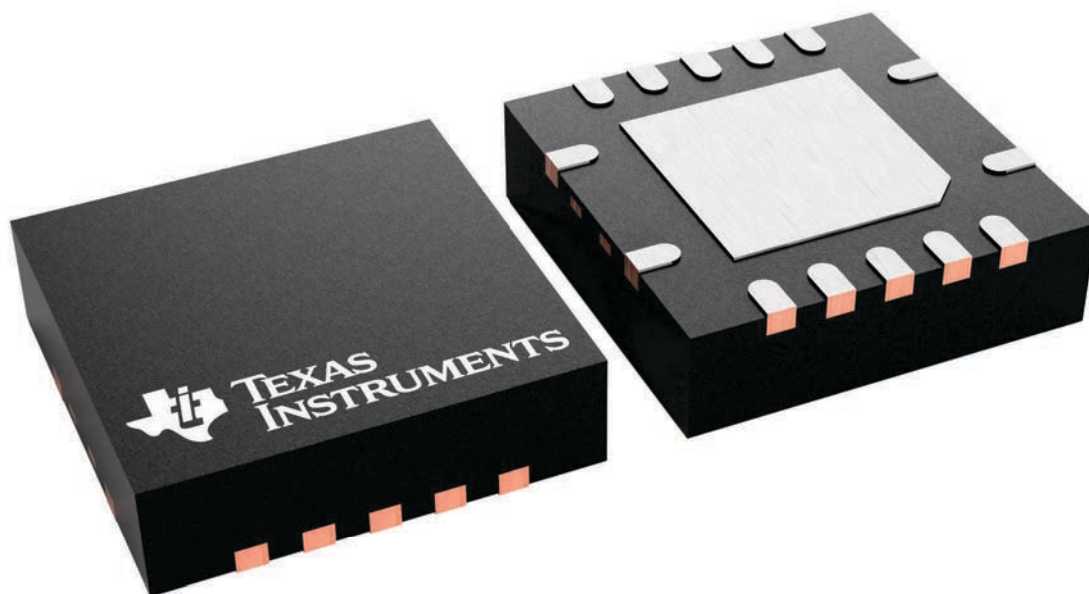
RGY 14

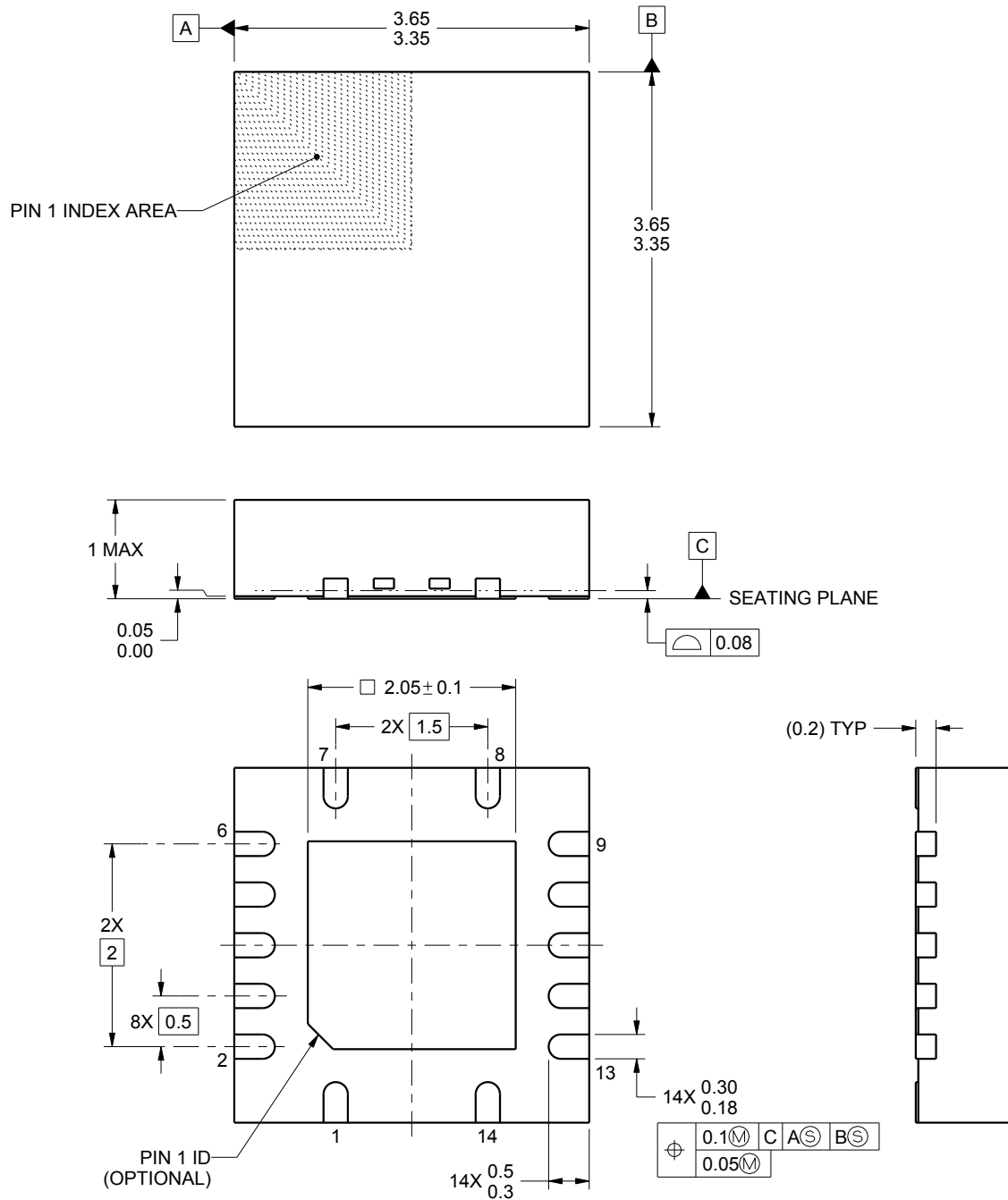
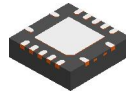
VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4219040/A 09/2015

NOTES:

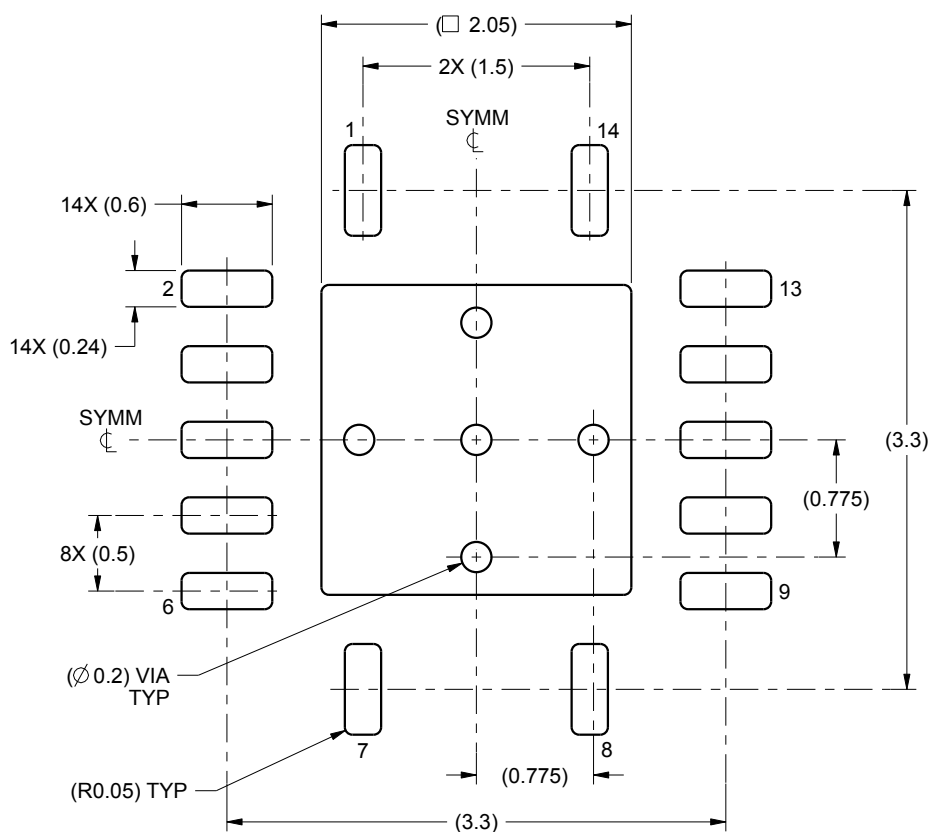
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

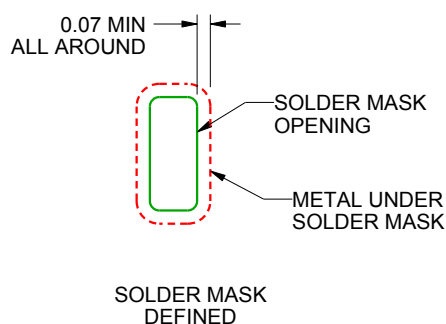
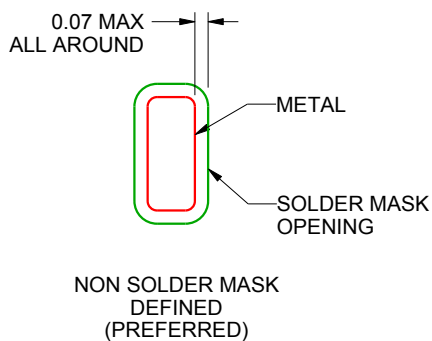
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

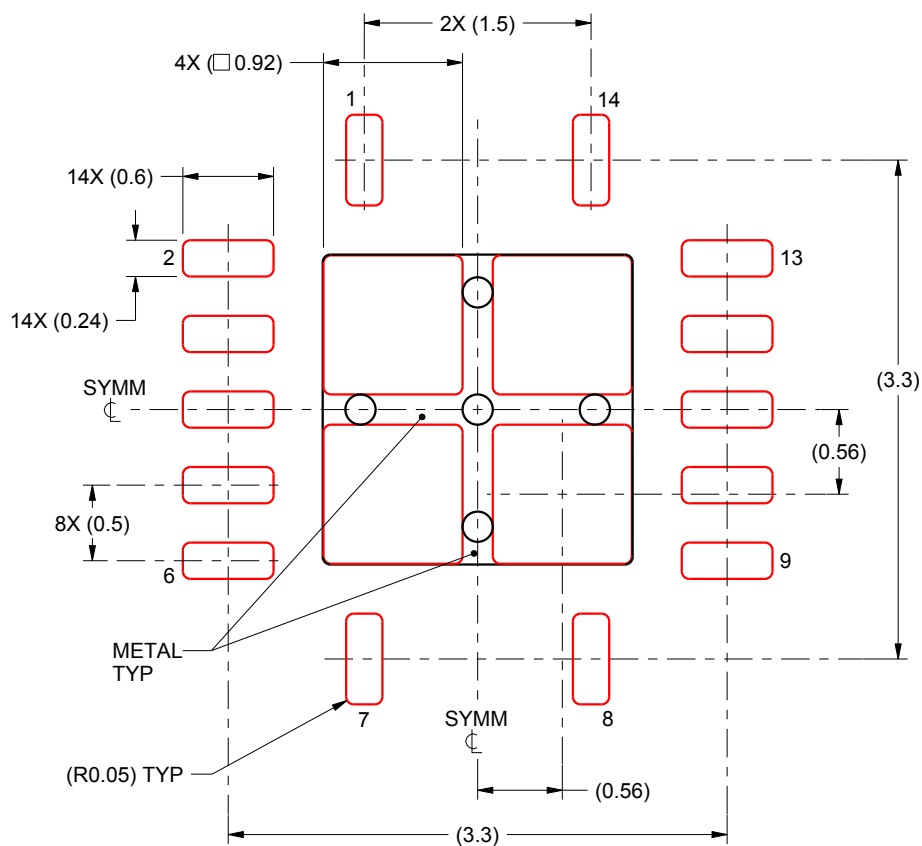
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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