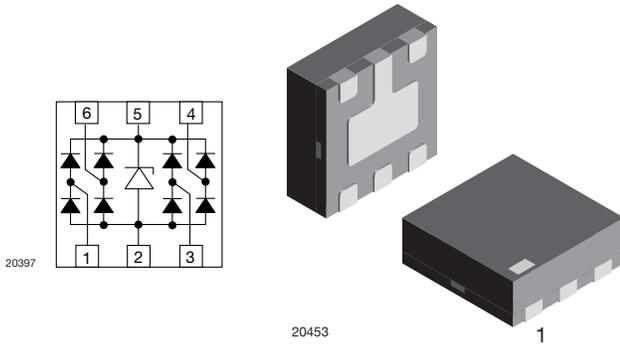


## 4-Line BUS-Port ESD Protection

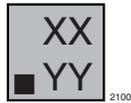


### FEATURES

- Ultra compact LLP75-6L package
- 4-line USB ESD protection
- Low leakage current
- Low load capacitance  $C_D = 1.2 \text{ pF}$
- ESD immunity acc. IEC 61000-4-2  $\pm 30 \text{ kV}$  contact discharge  $\pm 30 \text{ kV}$  air discharge
- High surge current acc. IEC 61000-4-5  $I_{pp} > 11 \text{ A}$
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu), (no Sn)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



### MARKING (example only)



Dot = pin 1 marking

XX = date code

YY = type code (see table below)

### DESIGN SUPPORT TOOLS

[click logo to get started](#)



ORDERING INFORMATION			
DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VBUS54CV-HSF	VBUS54CV-HSF-G4-08	3000	15 000

PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VBUS54CV-HSF	LLP75-6L	UC	4.2 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

ABSOLUTE MAXIMUM RATINGS VBUS54CV-HSF				
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Pin 1, 3, 4 or 6 to pin 2 acc. IEC 61000-4-5; $t_p = 8/20 \mu\text{s}$ /single shot	$I_{PPM}$	11	A
	Pin 5 to pin 2 acc. IEC 61000-4-5; $t_p = 8/20 \mu\text{s}$ ; single shot		13	
Peak pulse power	Pin 1, 3, 4 or 6 to pin 2 acc. IEC 61000-4-5; $t_p = 8/20 \mu\text{s}$ /single shot	$P_{PP}$	242	W
	Pin 5 to pin 2 acc. IEC 61000-4-5; $t_p = 8/20 \mu\text{s}$ ; single shot		246	
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	$V_{ESD}$	$\pm 30$	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		$\pm 30$	
Operating temperature	Junction temperature	$T_J$	-40 to +125	°C
Storage temperature		$T_{STG}$	-40 to +150	°C

**ELECTRICAL CHARACTERISTICS VBUS54CV-HSF** (pin 1, 3, 4, or 6 to pin 2)

 ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	4	lines
Reverse stand-off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	5.5	V
Reverse voltage	at $I_R = 0.1\text{ }\mu\text{A}$	$V_R$	5.5	-	-	V
Reverse current	at $V_{RWM} = 5.5\text{ V}$	$I_R$	-	0.01	0.1	$\mu\text{A}$
Reverse breakdown voltage	at $I_R = 1\text{ mA}$	$V_{BR}$	7	7.9	8.6	V
Reverse clamping voltage	at $I_{PP} = 11\text{ A}$	$V_C$	-	18	22	V
Forward clamping voltage	at $I_{PP} = 11\text{ A}$	$V_F$	-	6.5	8	V
Capacitance	$V_R$ (at I/O pin) = 0 V $V_R$ (at pin 5) = 5 V; $f = 1\text{ MHz}$	$C_D$	-	1.2	2.5	pF
Line symmetry	Difference of the line capacitances	$dC_D$	-	-	0.2	pF

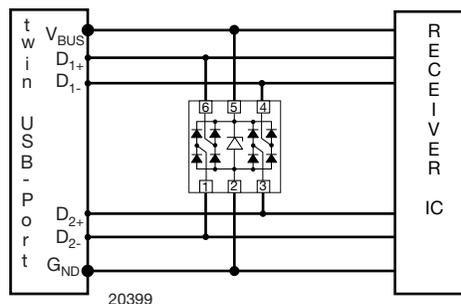
**ELECTRICAL CHARACTERISTICS** (pin 5 to pin 2)

 ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Reverse stand-off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	5.5	V
Reverse voltage	at $I_R = 0.1\text{ }\mu\text{A}$ ; pin 2 to pin 1	$V_R$	5.5	-	-	V
Reverse current	at $V_{RWM} = 5.5\text{ V}$	$I_R$	-	0.01	0.1	$\mu\text{A}$
Reverse breakdown voltage	at $I_R = 1\text{ mA}$	$V_{BR}$	6.3	7.1	8	V
Reverse clamping voltage	at $I_{PP} = 13\text{ A}$	$V_C$	-	18	22	V
Forward clamping voltage	at $I_{PP} = 13\text{ A}$	$V_F$	-	-	7	V
Capacitance	$V_R$ (at pin 5) = 0 V; $f = 1\text{ MHz}$	$C_D$	-	190	-	pF

**APPLICATION NOTE**

With the VBUS54CV-HSF a double, high speed USB-port can be protected against transient voltage signals. Negative transients will be clamped close below the ground level while positive transients will be clamped close above the working range. An avalanche diode clamps the supply line ( $V_{BUS}$  at pin 5) to ground (pin 2). The high speed data lines,  $D_{1+}$ ,  $D_{2+}$ ,  $D_{1-}$  and  $D_{2-}$ , are connected to pin 1, 3, 4 and 6. As long as the signal voltage on the data lines is between the ground- and the  $V_{BUS}$ -level, the low capacitance PN-diodes offer a very high isolation to  $V_{BUS}$ , ground and to the other data lines. But as soon as any transient signal exceeds this working range, one of the PN-diodes gets in the forward mode and clamps the transient to ground or the avalanche break through voltage level.





TYPICAL CHARACTERISTICS (T<sub>amb</sub> = 25 °C, unless otherwise specified)

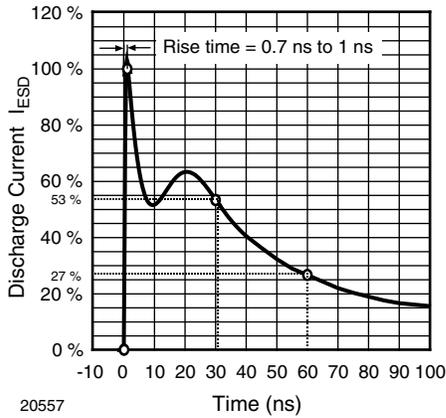


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

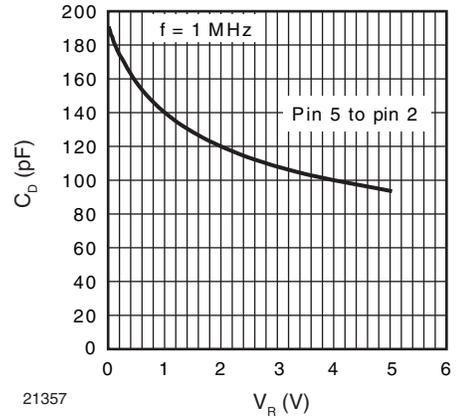


Fig. 4 - Typical Capacitance C<sub>D</sub> vs. Reverse Voltage V<sub>R</sub>

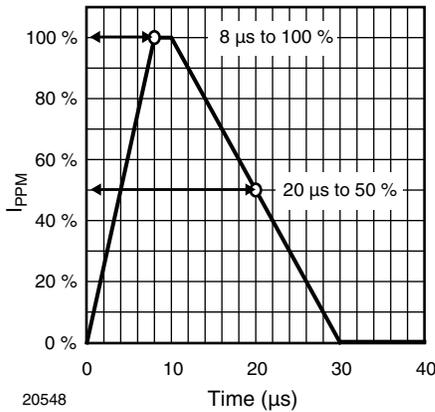


Fig. 2 - 8/20 μs Peak Pulse Current Wave Form acc. IEC 61000-4-5

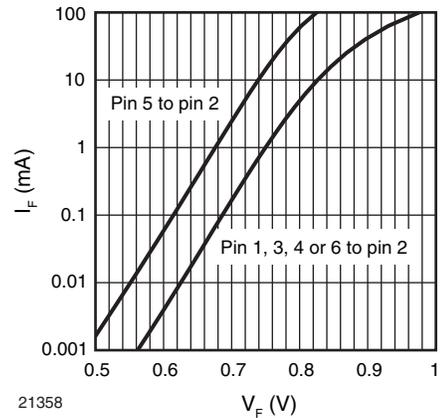


Fig. 5 - Typical Forward Current I<sub>F</sub> vs. Forward current I<sub>R</sub>

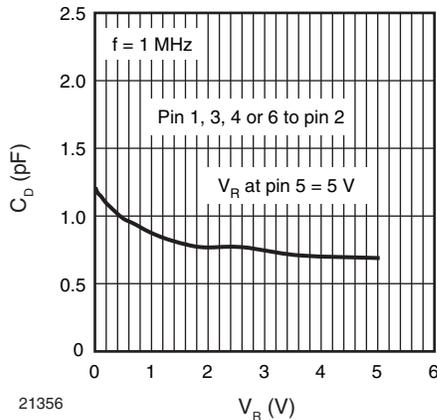


Fig. 3 - Typical Capacitance C<sub>D</sub> vs. Reverse Voltage V<sub>R</sub>

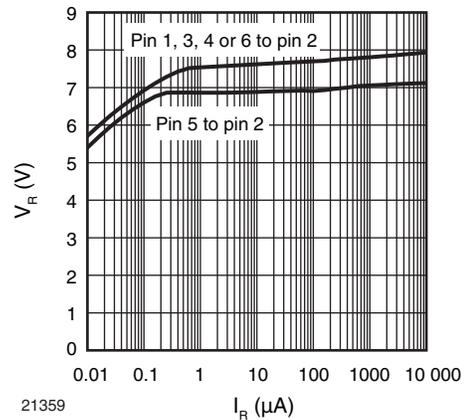


Fig. 6 - Typical Reverse Voltage V<sub>R</sub> vs. Reverse Current I<sub>R</sub>

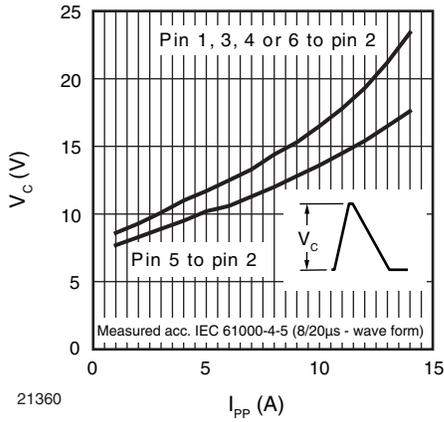


Fig. 7 - Typical Peak Clamping Voltage vs. Peak Pulse Current  $I_{PP}$

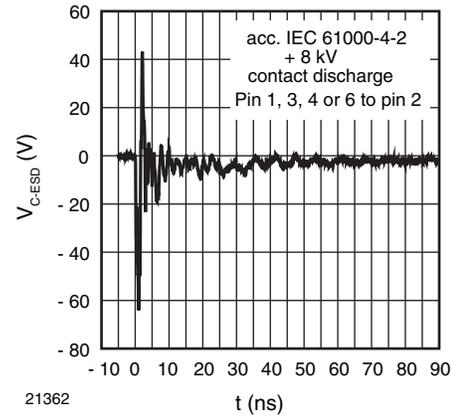


Fig. 9 - Typical Clamping Performance at 8 kV Contact Discharge (acc. IEC 61000-4-2)

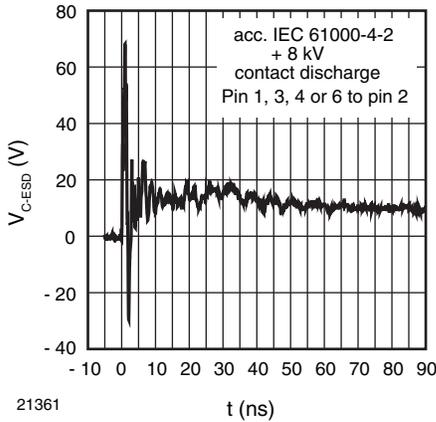


Fig. 8 - Typical Clamping Performance at 8 kV Contact Discharge (acc. IEC 61000-4-2)

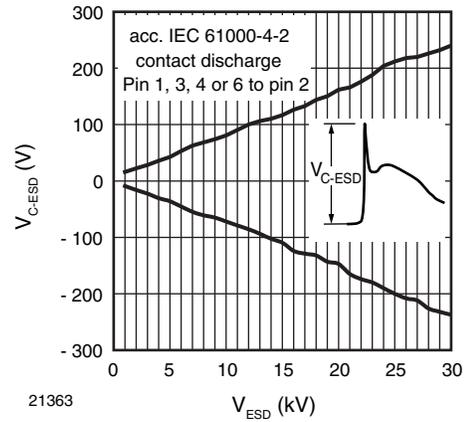
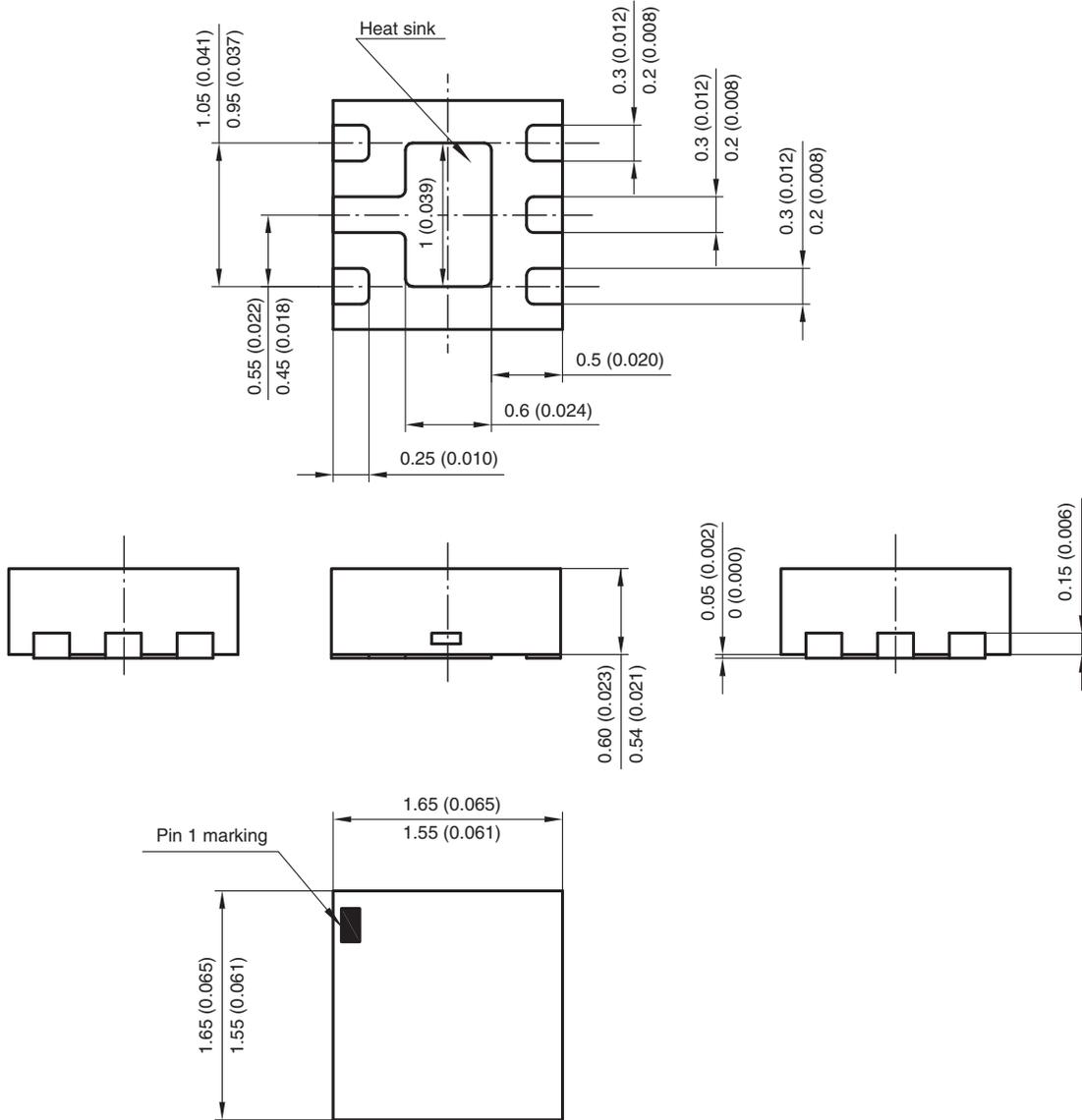


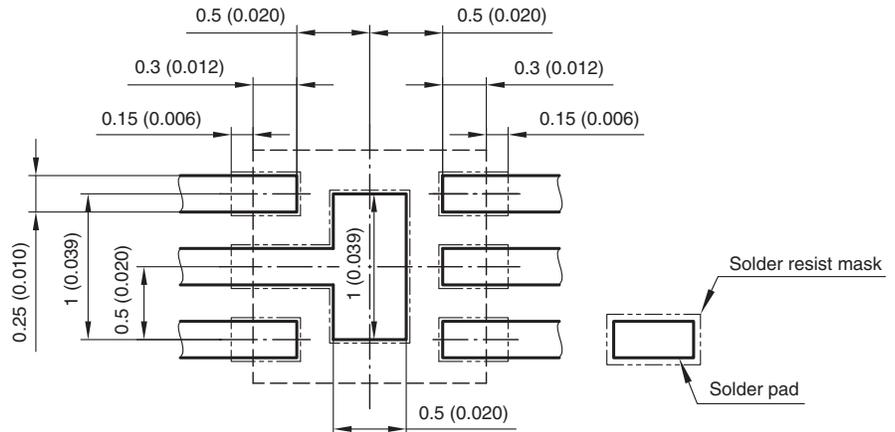
Fig. 10 - Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)



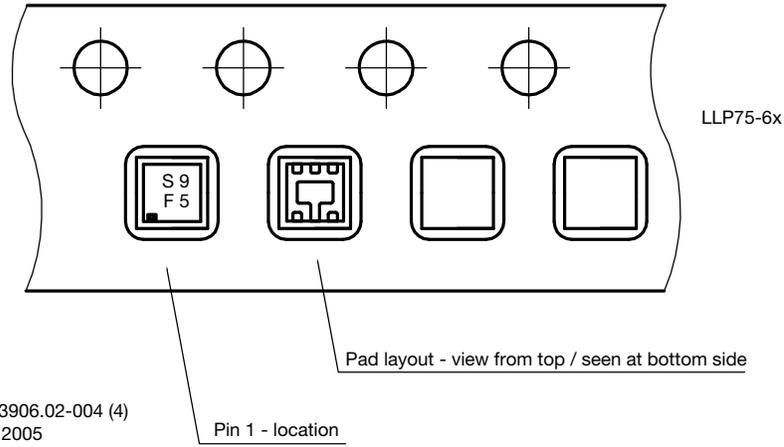
PACKAGE DIMENSIONS in millimeters (inches): **LLP75-6L**



Foot print recommendation:



Document no.:S8-V-3906.02-010 (4)  
 Created - Date: 04. MAY 2005  
 Rev. 4 - Date: 21. March 2006  
 20454



S8-V-3906.02-004 (4)  
10.01.2005

Pin 1 - location

Pad layout - view from top / seen at bottom side



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