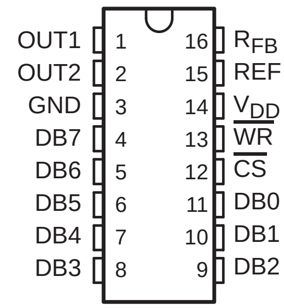
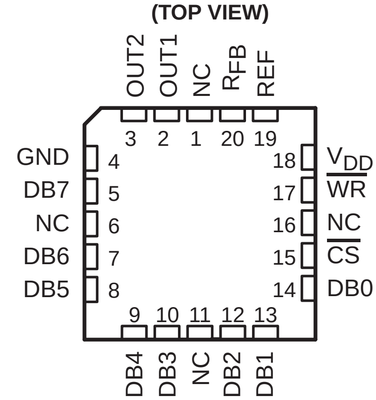
- **Easily Interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonic Over the Entire A/D Conversion Range**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Interchangeable With Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal-Processor Applications Including Interface With TMS320**
- **CMOS Technology**

D, N, OR PW PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC−No internal connection

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	1/2LSB Max
Power dissipation at V_{DD} = 5V	5mW Max
Setting time	100ns Max
Propagation delay time	80ns Max

description

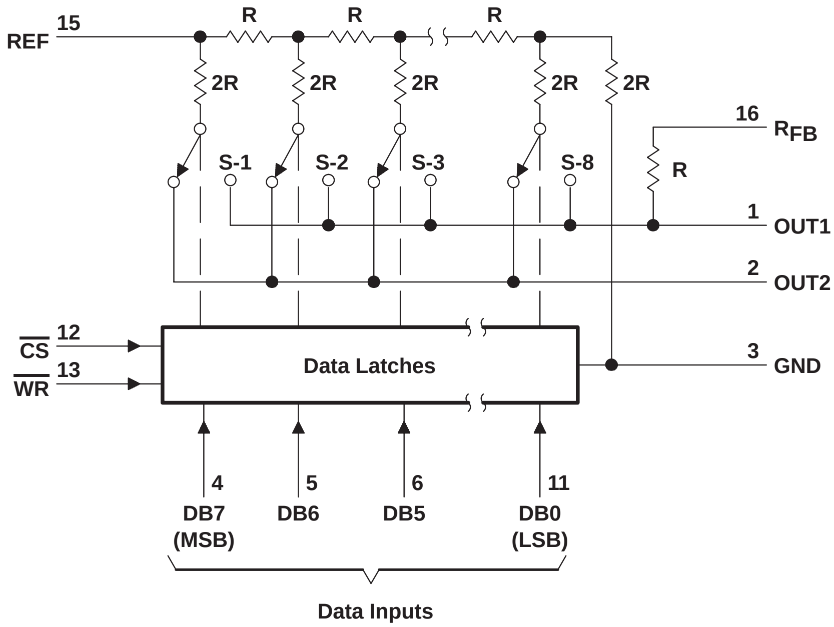
The TLC7524C, TLC7524E, and TLC7524I are CMOS, 8-bit, digital-to-analog converters (DACs) designed for easy interface to most popular microprocessors.

The devices are 8-bit, multiplying DACs with input latches and load cycles similar to the write cycles of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, which produce the highest glitch impulse. The devices provide accuracy to 1/2LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5mW typically.

Featuring operation from a 5V to 15V single supply, these devices interface easily to most microprocessor buses or output ports. The 2- or 4-quadrant multiplying makes these devices an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7524C is characterized for operation from 0°C to 70°C. The TLC7524I is characterized for operation from −25°C to +85°C. The TLC7524E is characterized for operation from −40°C to +85°C.

functional block diagram



Terminal numbers shown are for the D or N package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD}		−0.3V to 16.5V
Digital input voltage range, V_I		−0.3V to V_{DD} + 0.3V
Reference voltage, V_{ref}		±25V
Peak digital input current, I_I		10μA
Operating free-air temperature range, T_A:	TLC7524C	0°C to +70°C
	TLC7524I	−25°C to +85°C
	TLC7524E	−40°C to +85°C
Storage temperature range, T_{stg}		−65°C to +150°C
Case temperature for 10 seconds, T_C: FN package		+260°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds: D, N, or PW package		+260°C

package/ordering information

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

recommended operating conditions

		V_{DD} = 5V			V_{DD} = 15V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input voltage, V_{IL}				0.8			1.5	V
CS setup time, $t_{su(CS)}$		40			40			ns
CS hold time, $t_{h(CS)}$		0			0			ns
Data bus input setup time, $t_{su(D)}$		25			25			ns
Data bus input hold time, $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	TLC7524C	0		+70	0		+70	°C
	TLC7524I	−25		+85	−25		+85	
	TLC7524E	−40		+85	−40		+85	

electrical characteristics over recommended operating free-air temperature range, V_{ref} = ±10V, OUT1 and OUT2 at GND (unless otherwise noted)

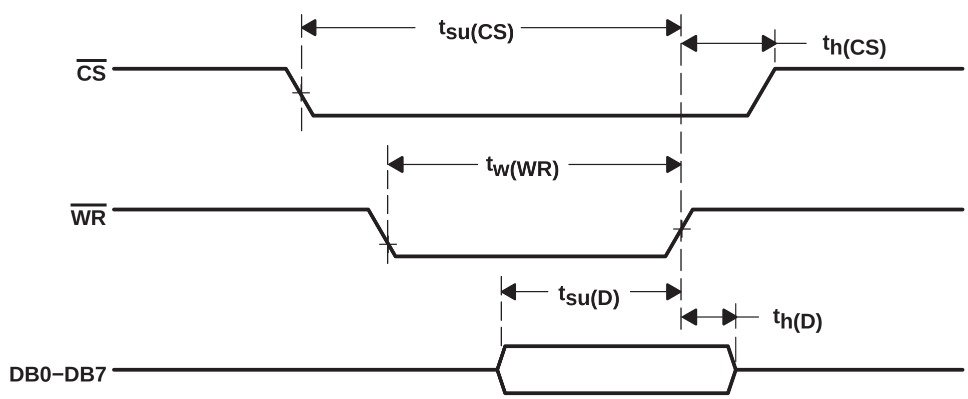
PARAMETER			TEST CONDITIONS	V_{DD} = 5V			V_{DD} = 15V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High-level input current		$V_I = V_{DD}$			10			10	µA
I_{IL}	Low-level input current		V_I = 0			−10			−10	µA
I_{lkg}	Output leakage current	OUT1	DB0−DB7 at 0V, $\overline{WR}$, $\overline{CS}$ at 0V, V_{ref} = ±10V			±400			±200	nA
		OUT2	DB0−DB7 at V_{DD}, $\overline{WR}$, $\overline{CS}$ at 0V, V_{ref} = ±10V			±400			±200	
I_{DD}	Supply current	Quiescent	DB0−DB7 at V_{IH}min or V_{IL}max			1			2	mA
		Standby	DB0−DB7 at 0V or V_{DD}			500			500	µA
k_{SVS}	Supply voltage sensitivity, Δgain/ΔV_{DD}		ΔV_{DD} = ±10%		0.01	0.16		0.005	0.04	%FSR/%
C_i	Input capacitance, DB0−DB7, $\overline{WR}$, $\overline{CS}$		V_I = 0			5			5	pF
C_o	Output capacitance	OUT1	DB0−DB7 at 0V, $\overline{WR}$, $\overline{CS}$ at 0V			30			30	pF
		OUT2				120			120	
		OUT1	DB0−DB7 at V_{DD}, $\overline{WR}$, $\overline{CS}$ at 0V			120			120	
		OUT2				30			30	
	Reference input impedance (REF to GND)			5		20	5		20	kΩ

operating characteristics over recommended operating free-air temperature range, V_{ref} = ±10V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{DD} = 5V			V_{DD} = 15V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error				±0.5			±0.5	LSB
Gain error	See Note 1			±2.5			±2.5	LSB
Settling time (to 1/2 LSB)	See Note 2			100			100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80			80	ns
Feedthrough at OUT1 or OUT2	Vref = ±10V (100kHz sinewave) $\overline{WR}$ and $\overline{CS}$ at 0V, DB0−DB7 at 0V			0.5			0.5	%FSR
Temperature coefficient of gain	T_A = +25°C to MAX		±0.004			±0.001		%FSR/°C

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal full-scale range (FSR) = V_{ref} − 1LSB.
2. OUT1 load = 100Ω, C_{ext} = 13pF, $\overline{WR}$ at 0V, $\overline{CS}$ at 0V, DB0 − DB7 at 0V to V_{DD} or V_{DD} to 0V.

operating sequence



PRINCIPLES OF OPERATION

voltage-mode operation

It is possible to operate the current-multiplying DAC in these devices in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. Figure 1 is an example of a current-multiplying DAC, which is operated in voltage mode.

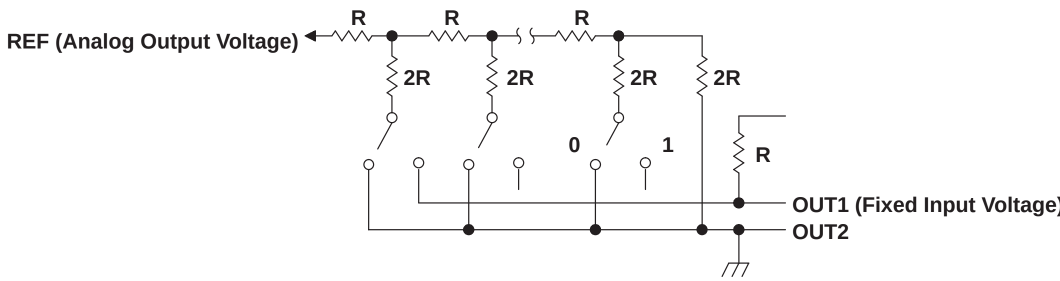


Figure 1. Voltage Mode Operation

The relationship between the fixed-input voltage and the analog-output voltage is given by the following equation:

$$V_O = V_I\ (D/256)$$

where

V_O = analog output voltage
V_I = fixed input voltage
D = digital input code converted to decimal

In voltage-mode operation, these devices meet the following specification:

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at REF	V_{DD} = 5V, OUT1 = 2.5V, OUT2 at GND, T_A = +25°C		1	LSB

PRINCIPLES OF OPERATION

The TLC7524C, TLC7524E, and TLC7524I are 8-bit multiplying DACs consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary-weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded. These decoded bits, through a modification in the R-2R ladder, control three equally-weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 2. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source I/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30pF maximum) appears at OUT2 and the on-state switch capacitance (120pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 2. Analysis of the circuit for all digital inputs high is similar to Figure 2; however, in this case, I_{ref} would be switched to OUT1.

The DAC on these devices interfaces to a microprocessor through the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, analog output on these devices responds to the data activity on the DB0−DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0−DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figure 3 and Figure 4. Table 1 and Table 2 summarize input coding for unipolar and bipolar operation respectively.

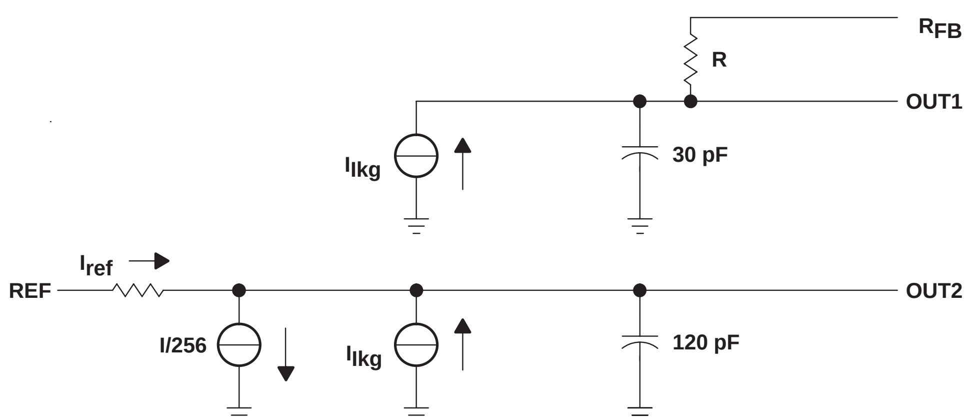
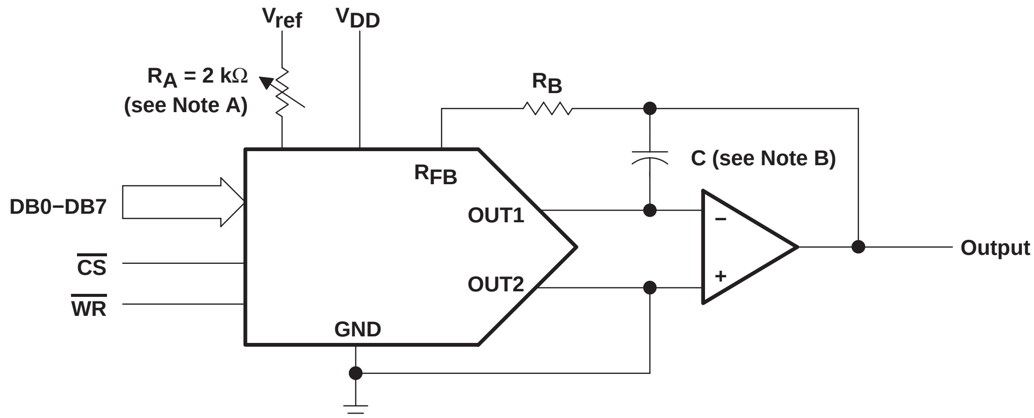


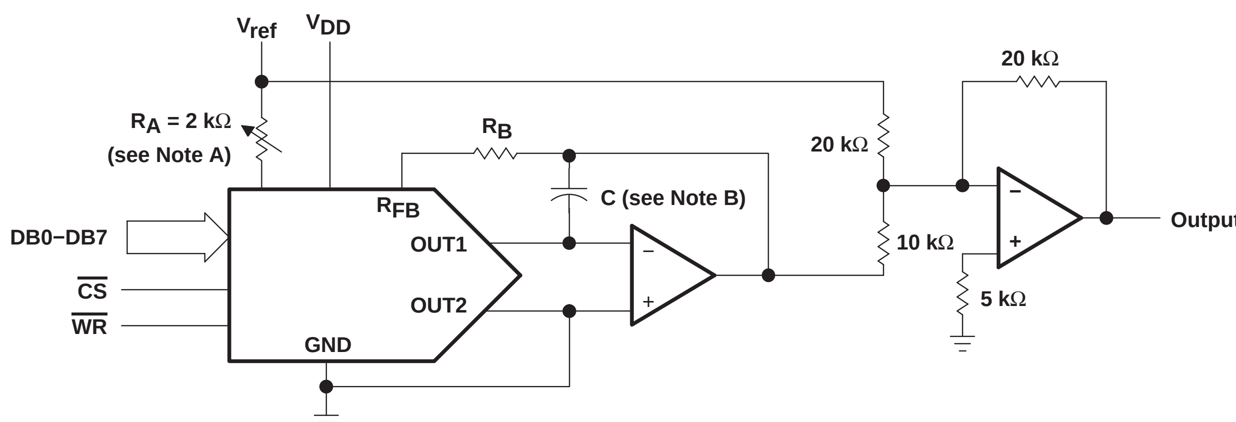
Figure 2. TLC7524 Equivalent Circuit With All Digital Inputs Low

PRINCIPLES OF OPERATION



NOTES: A. R_A and R_B used only if gain adjustment is required.
B. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 3. Unipolar Operation (2-Quadrant Multiplication)



NOTES: A. R_A and R_B used only if gain adjustment is required.
B. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 4. Bipolar Operation (4-Quadrant Operation)

Table 1. Unipolar Binary Code

DIGITAL INPUT (see Note 3) MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_{ref}$ (255/256)
1 0 0 0 0 0 0 1	$-V_{ref}$ (129/256)
1 0 0 0 0 0 0 0	$-V_{ref}$ (128/256) = $-V_{ref}/2$
0 1 1 1 1 1 1 1	$-V_{ref}$ (127/256)
0 0 0 0 0 0 0 1	$-V_{ref}$ (1/256)
0 0 0 0 0 0 0 0	0

NOTE 3: LSB = 1/256 (V_{ref})

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (see Note 4) MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	V_{ref} (127/128)
1 0 0 0 0 0 0 1	V_{ref} (1/128)
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{ref}$ (1/128)
0 0 0 0 0 0 0 1	$-V_{ref}$ (127/128)
0 0 0 0 0 0 0 0	$-V_{ref}$

NOTE 4: LSB = 1/128 (V_{ref})

PRINCIPLES OF OPERATION

microprocessor interfaces

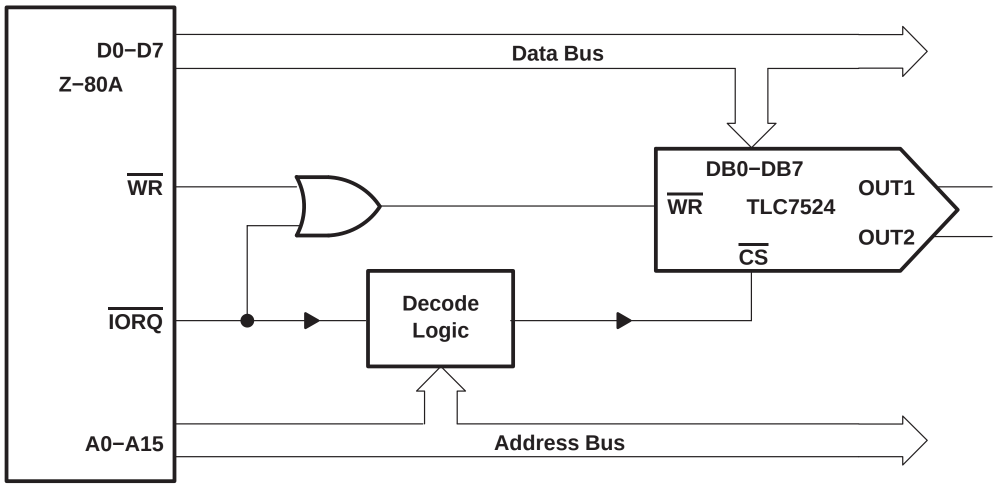


Figure 5. TLC7524: Z-80A Interface

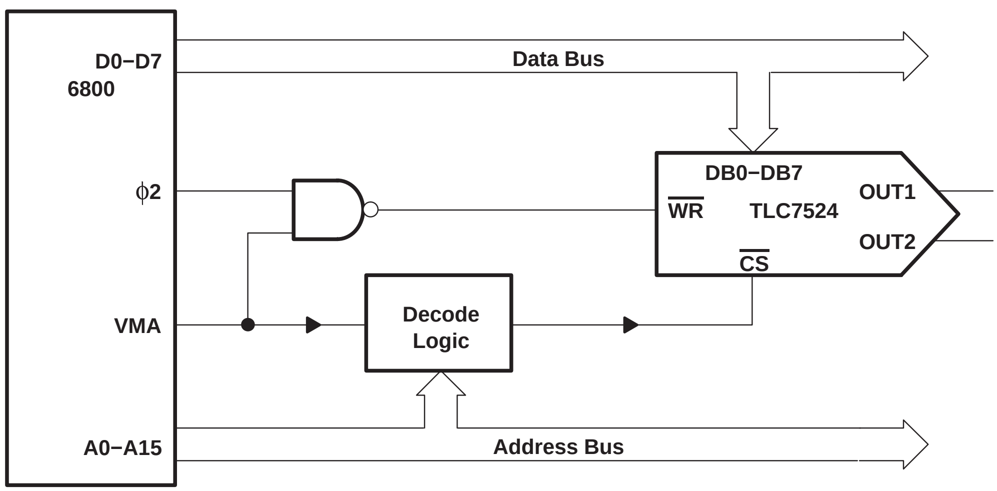


Figure 6. TLC7524: 6800 Interface

PRINCIPLES OF OPERATION

microprocessor interfaces (continued)

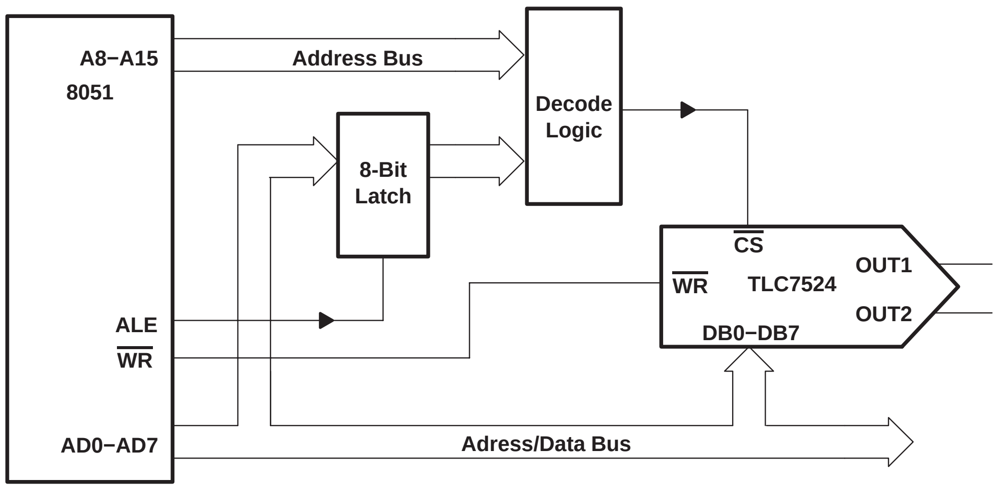


Figure 7. TLC7524: 8051 Interface

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
6/07	D	Front Page	—	Deleted Available Options table.
		2	—	Inserted Package/Ordering information.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC7524CD	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7524C
TLC7524CDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7524C
TLC7524CFNR	Obsolete	Production	PLCC (FN) | 20	-	-	Call TI	Call TI	0 to 70	TLC7524C
TLC7524CN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC7524CN
TLC7524CNS	Active	Production	SOP (NS) | 16	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7524
TLC7524CNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7524
TLC7524CPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P7524
TLC7524CPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P7524
TLC7524ED	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC7524E
TLC7524EDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC7524E
TLC7524EN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC7524EN
TLC7524ID	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	TLC7524I
TLC7524IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	TLC7524I
TLC7524IFN	Obsolete	Production	PLCC (FN) | 20	-	-	Call TI	Call TI	-25 to 85	TLC7524I
TLC7524IN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	TLC7524IN
TLC7524IPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	Y7524
TLC7524IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	Y7524

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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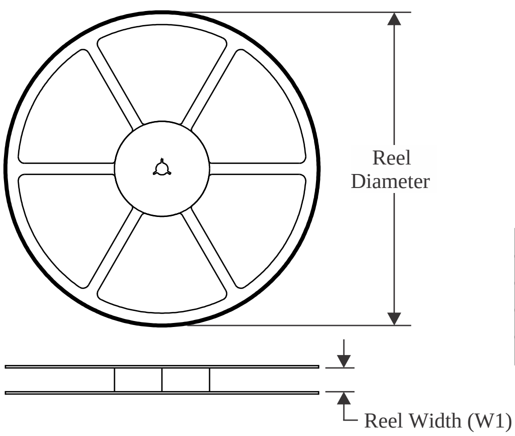
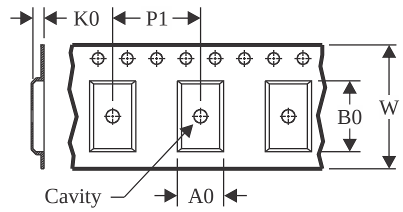
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

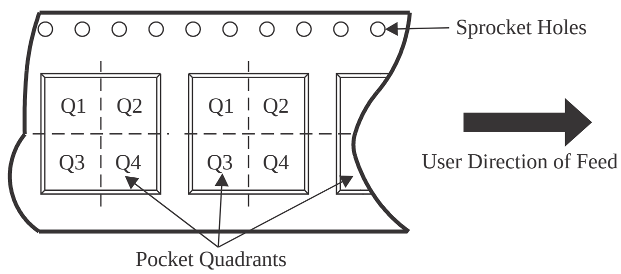


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

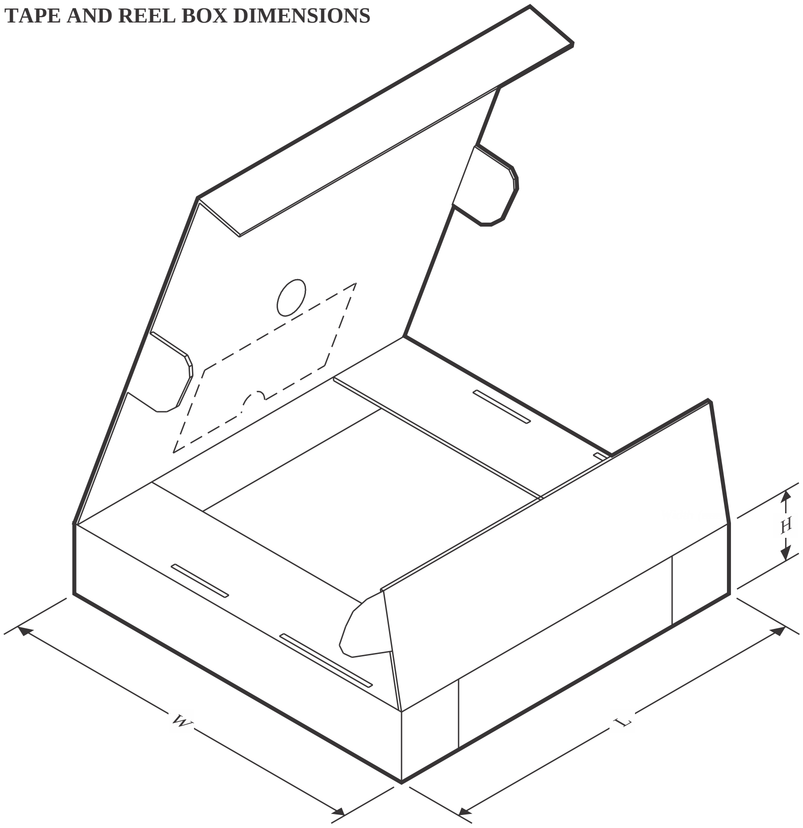
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7524CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLC7524CNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TLC7524CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC7524EDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLC7524IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLC7524IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

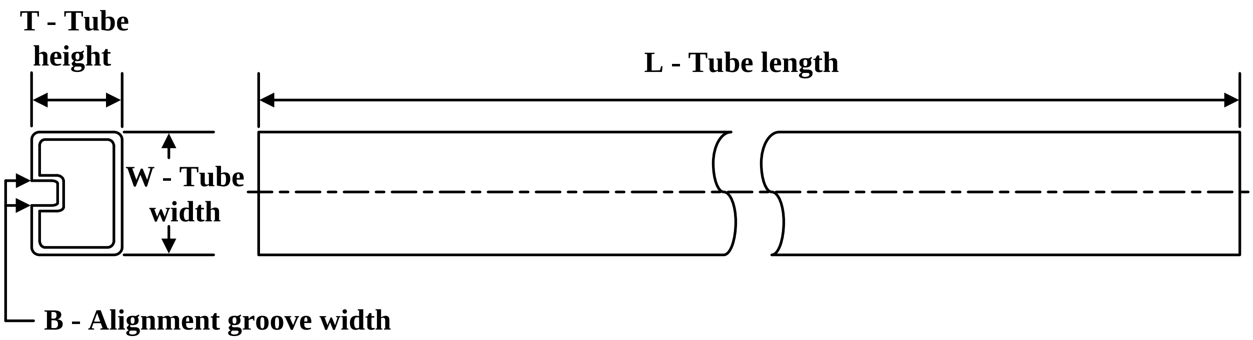
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7524CDR	SOIC	D	16	2500	350.0	350.0	43.0
TLC7524CNSR	SOP	NS	16	2000	356.0	356.0	35.0
TLC7524CPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TLC7524EDR	SOIC	D	16	2500	350.0	350.0	43.0
TLC7524IDR	SOIC	D	16	2500	350.0	350.0	43.0
TLC7524IPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

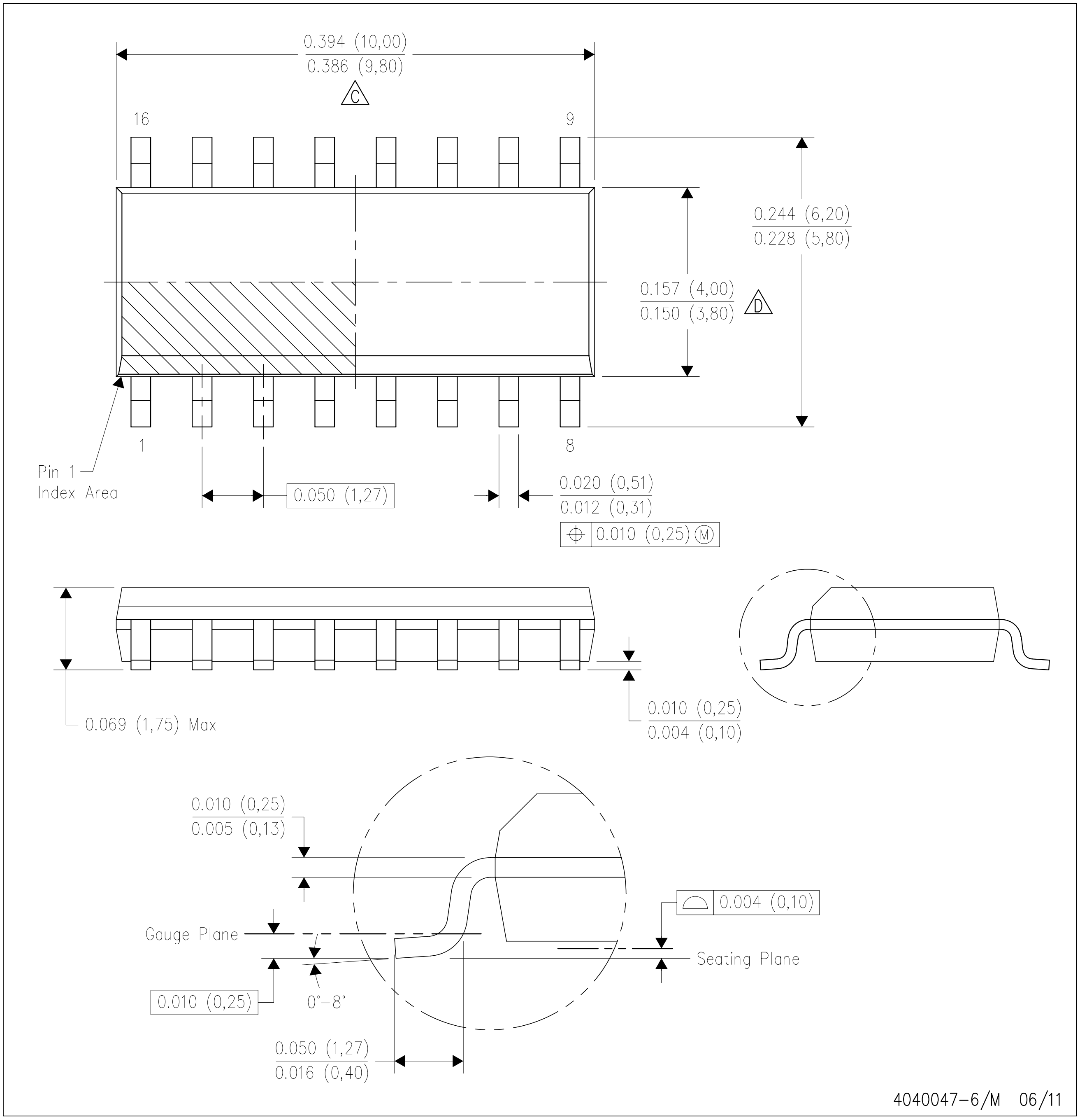
TUBE



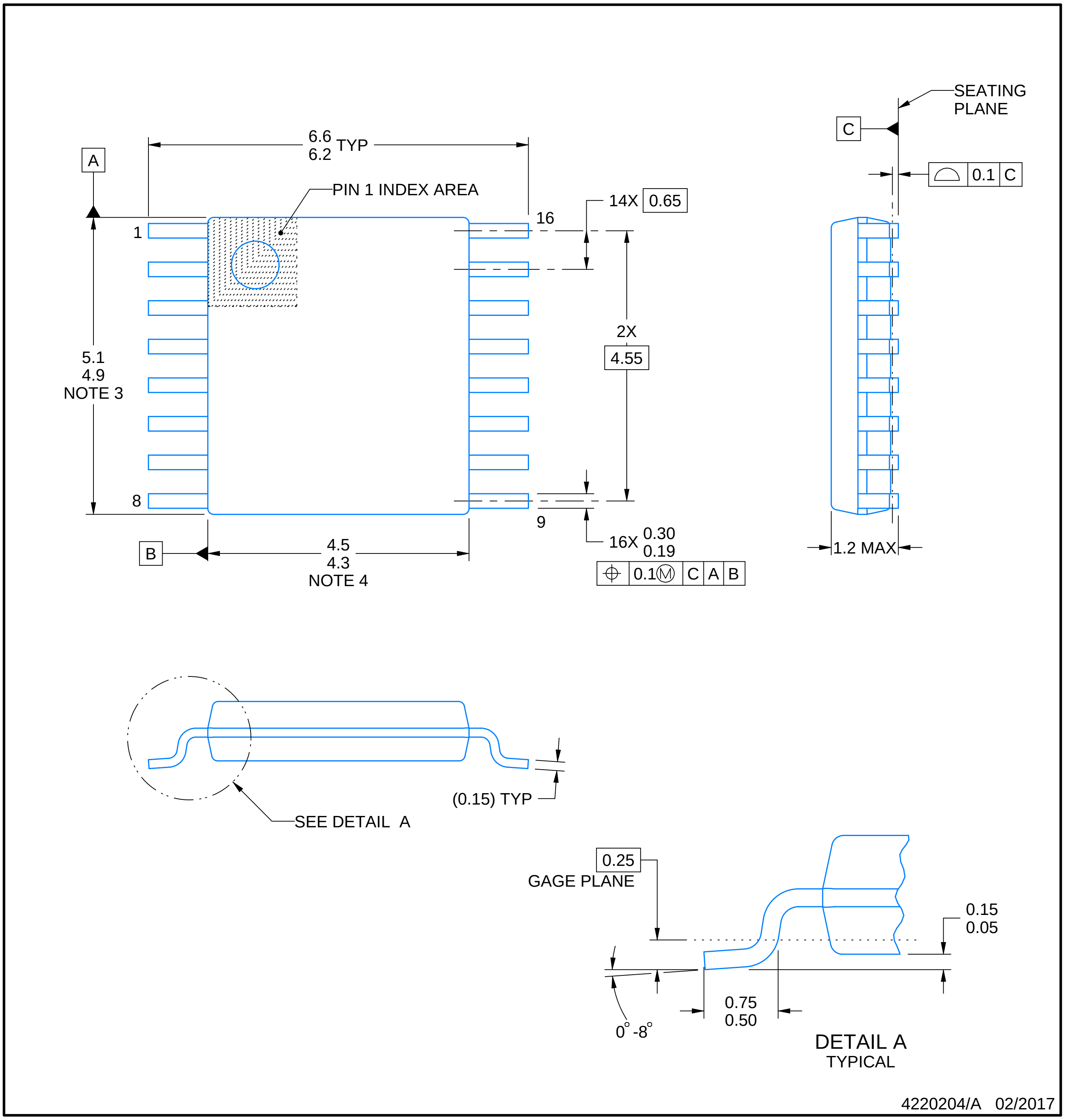
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC7524CD	D	SOIC	16	40	505.46	6.76	3810	4
TLC7524CDG4	D	SOIC	16	40	505.46	6.76	3810	4
TLC7524CN	N	PDIP	16	25	506	13.97	11230	4.32
TLC7524CNE4	N	PDIP	16	25	506	13.97	11230	4.32
TLC7524CNS	NS	SOP	16	50	530	10.5	4000	4.1
TLC7524CPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TLC7524ED	D	SOIC	16	40	505.46	6.76	3810	4
TLC7524EN	N	PDIP	16	25	506	13.97	11230	4.32
TLC7524ID	D	SOIC	16	40	505.46	6.76	3810	4
TLC7524IN	N	PDIP	16	25	506	13.97	11230	4.32
TLC7524IPW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

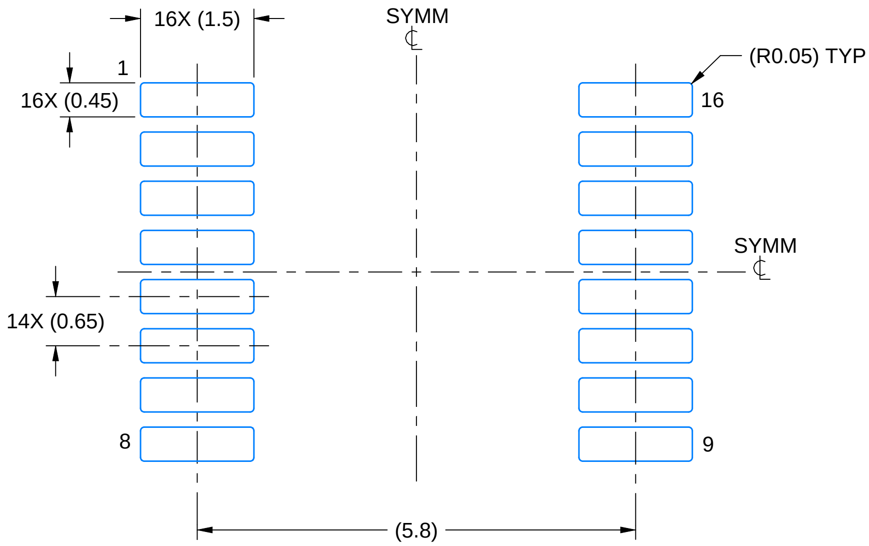


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

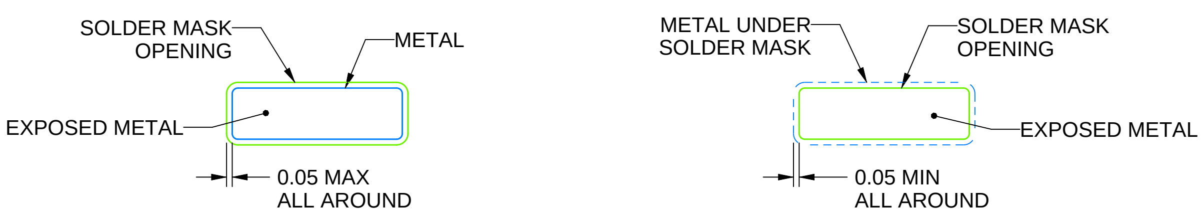


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

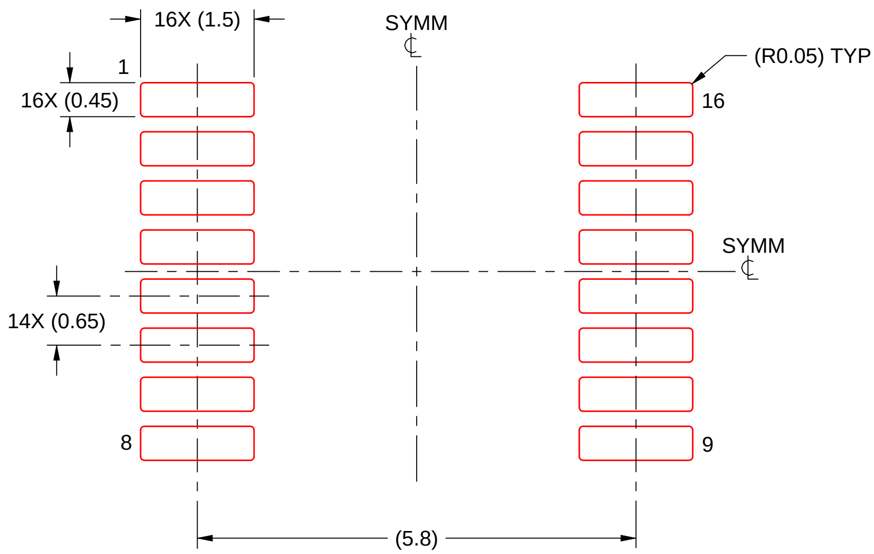
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

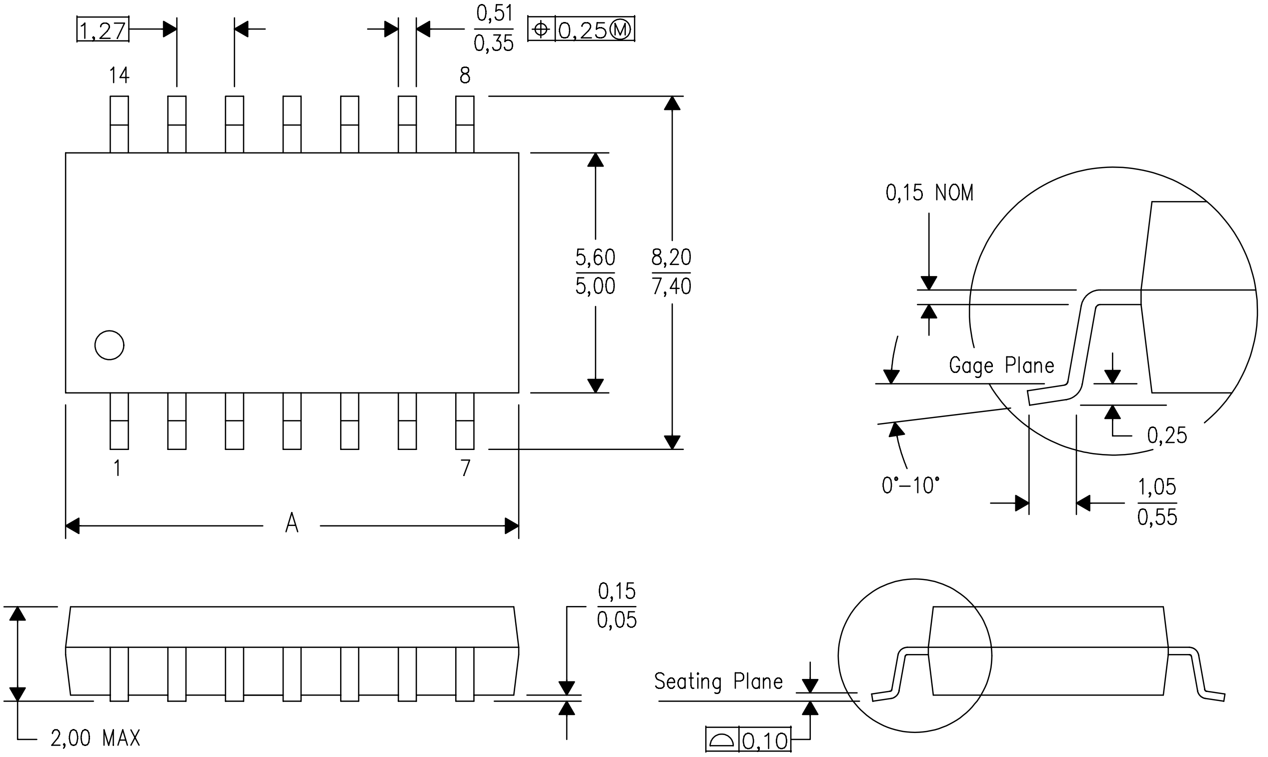
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



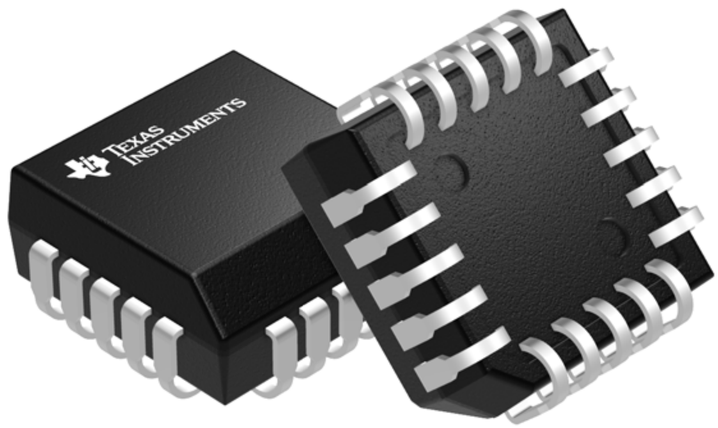
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

FN 20 PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

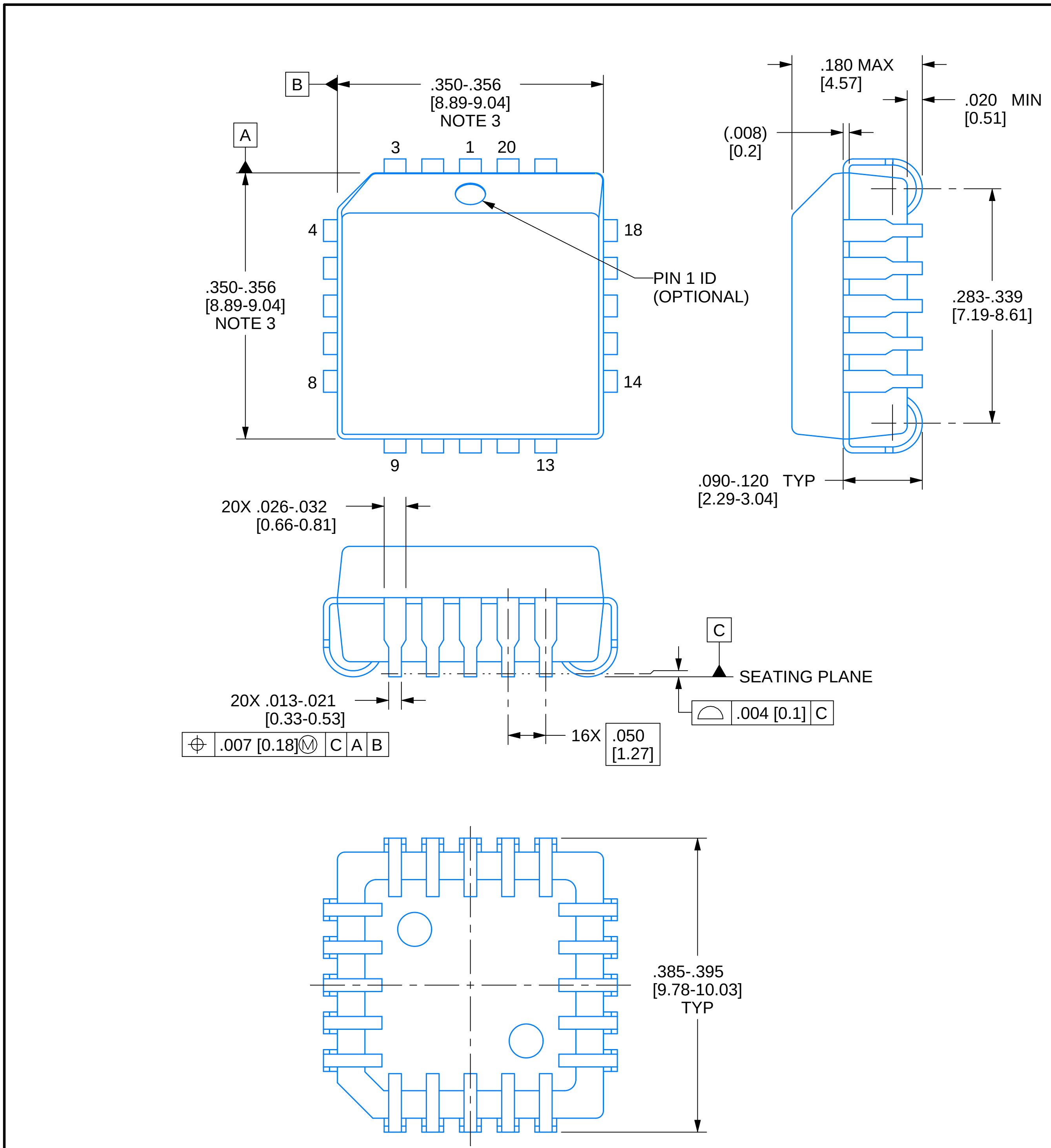
4040005-2/C

PACKAGE OUTLINE

FN0020A

PLCC - 4.57 mm max height

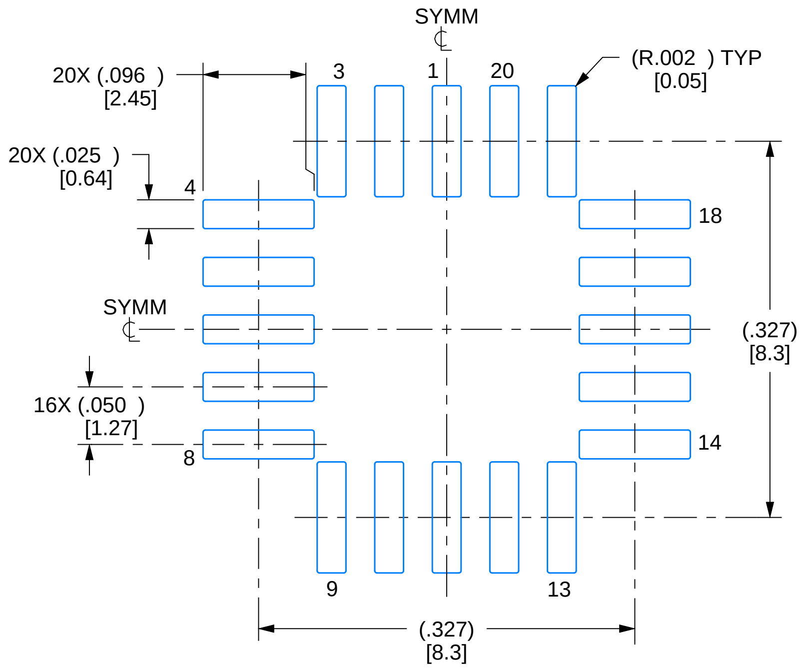
PLASTIC CHIP CARRIER



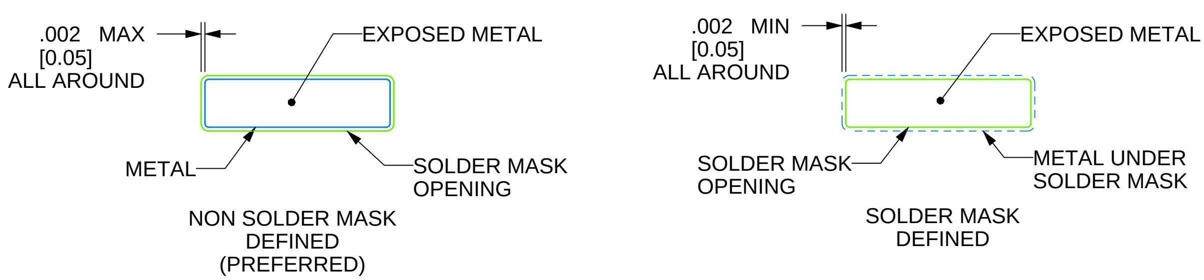
4215152/B 04/2017

NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

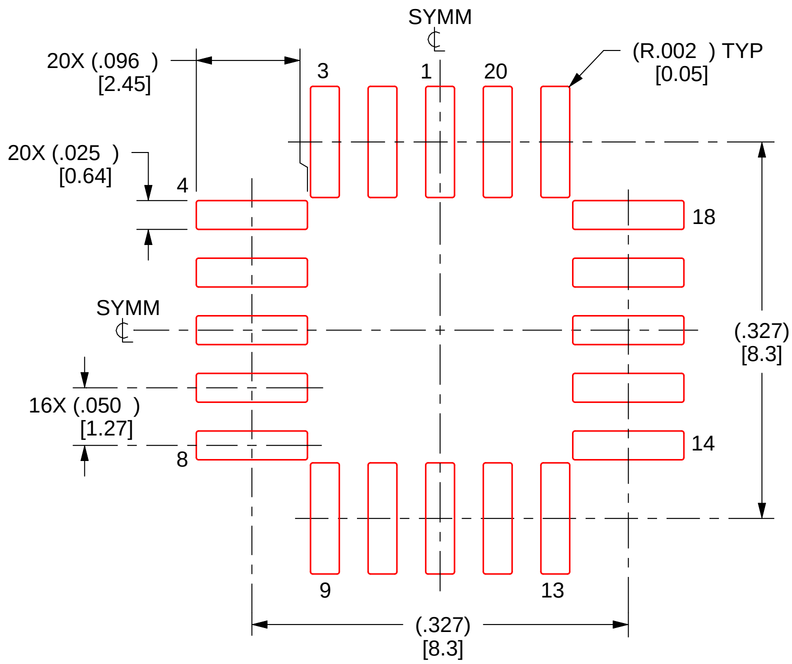


SOLDER MASK DETAILS

4215152/B 04/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

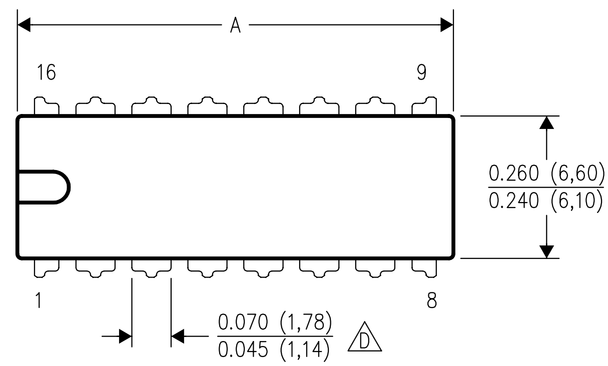
4215152/B 04/2017

NOTES: (continued)

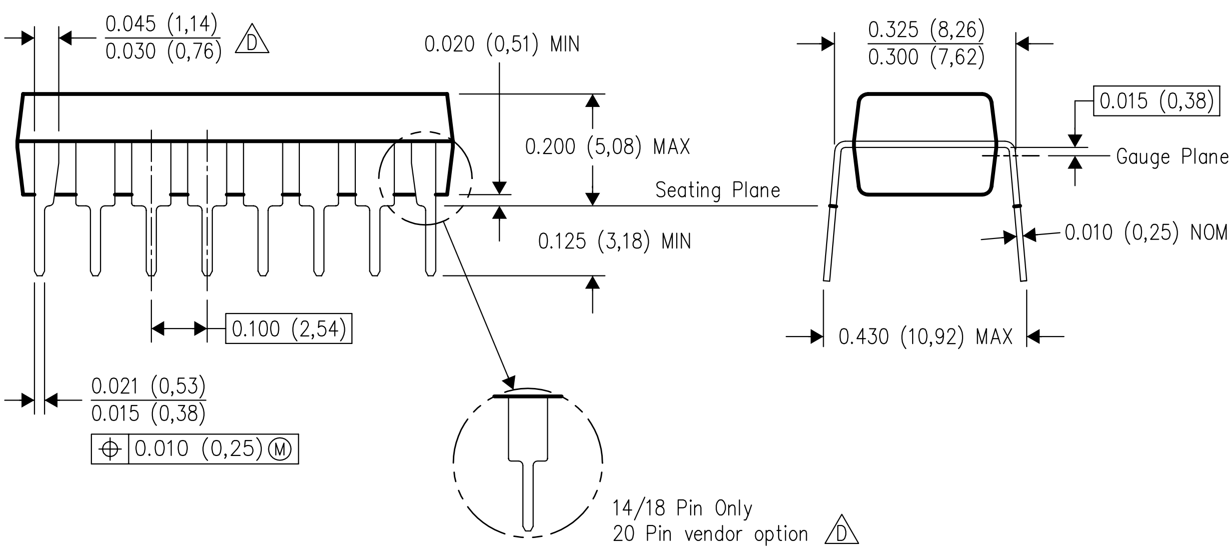
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

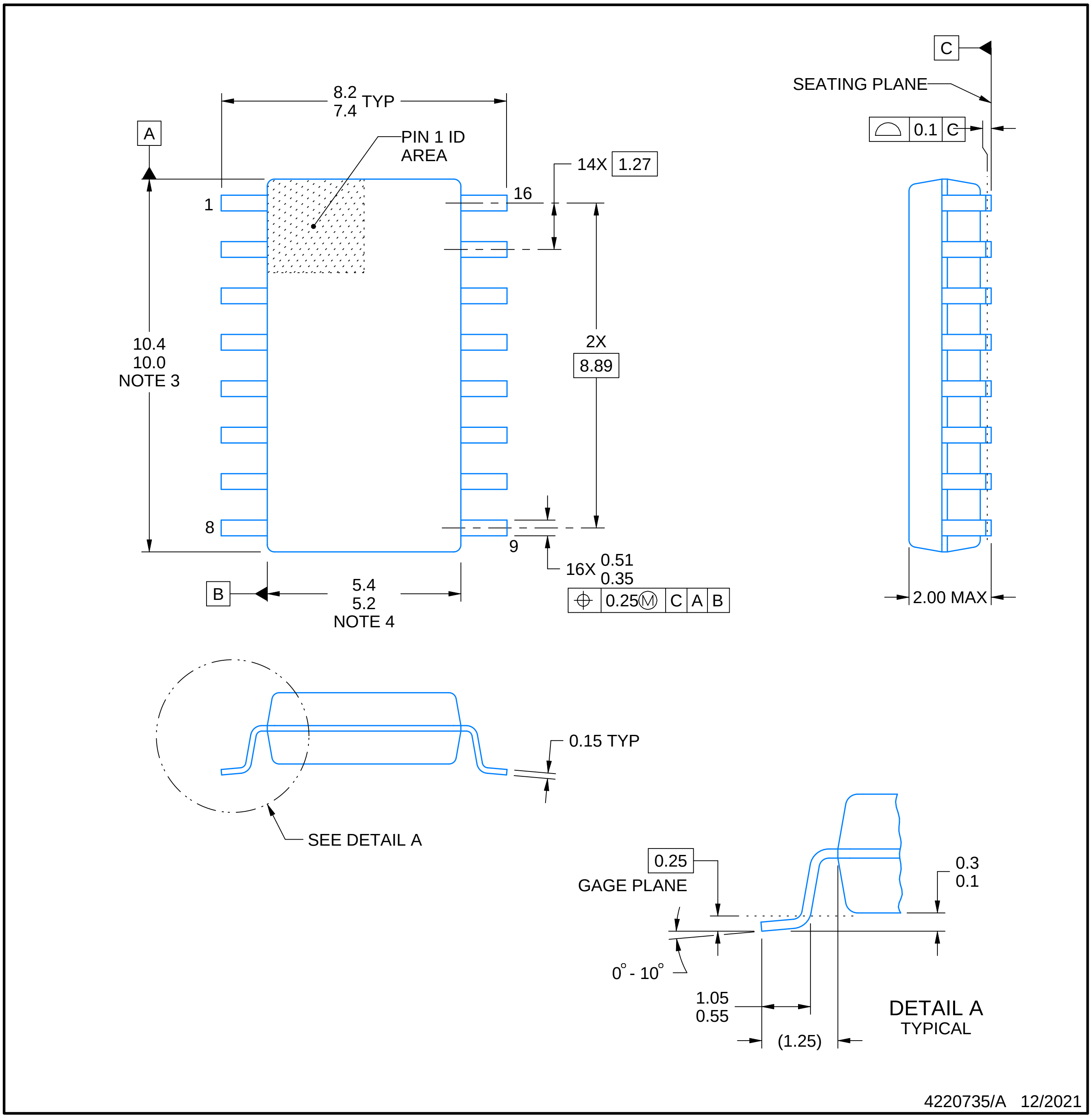


PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



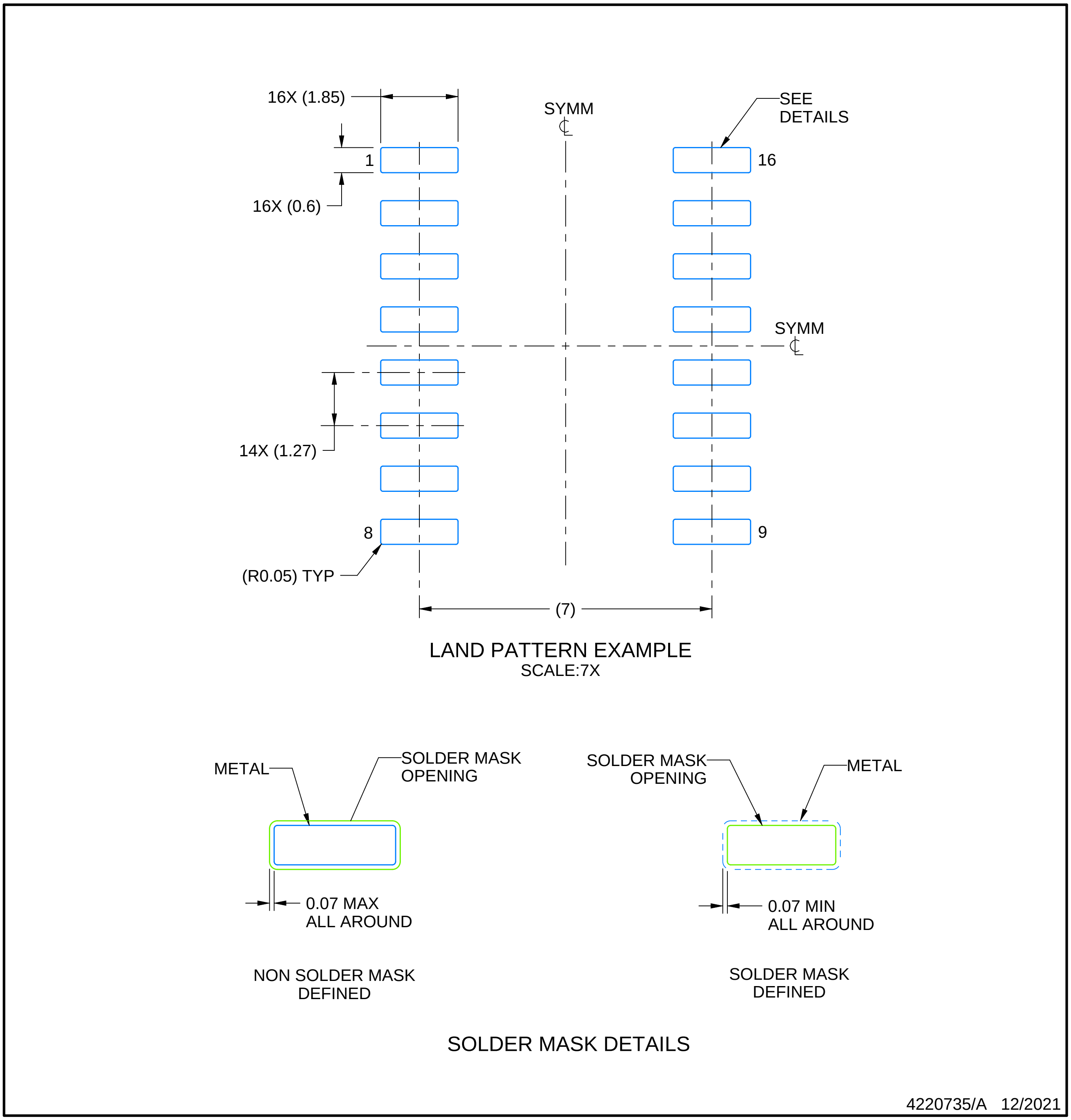
4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.



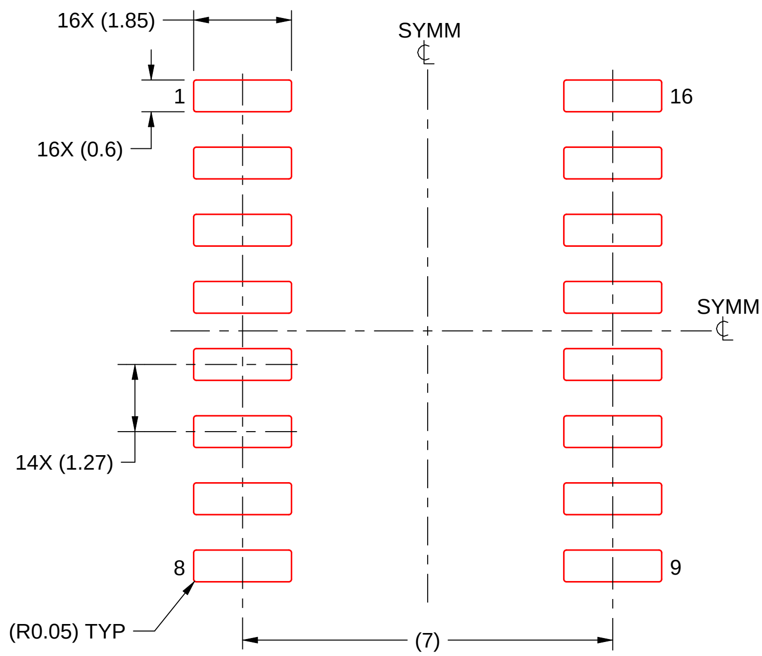
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.